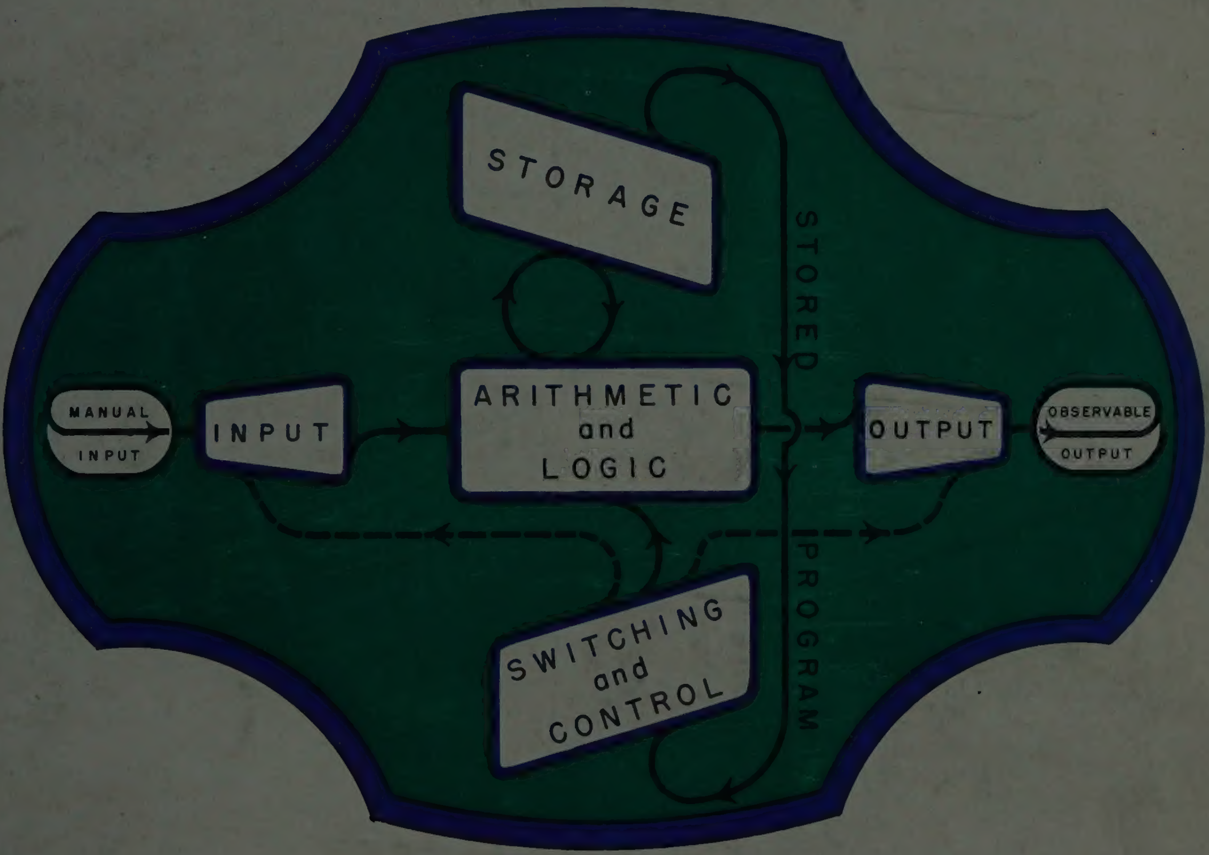
Vol. 41 OCTOBER · 1953 No. 10

Proceedings of the I·R·E

COMPUTER ISSUE


STORAGE
STORED PROGRAM
MANUAL INPUT
INPUT
ARITHMETIC and LOGIC
OUTPUT
OBSERVABLE OUTPUT
SWITCHING and CONTROL

IN THIS ISSUE

Forty-One Papers Covering the Computer Field
Selected with the Collaboration of the IRE Professional Group
on Electronic Computers

Table of Contents, Pages 1217-1218

The Institute of Radio Engineers

UTC

for Military Components

UTC was the largest supplier of transformer components in World War II. Present UTC production is on a similar basis. Illustrated below are a few of the thousand military types in UTC 1953 production.

Carrier frequency filter.........Aircraft low frequency filter.........Plate transformer.

Typical hermetically sealed power transformers for 60 cycle service.

Hermetically sealed audio and pulse transformers.

60 cycle and 400 cycle components hermetically sealed and fosterized.

Miniaturized audio units, magnetic amplifiers, etc.

United Transformer Co.

150 VARICK STREET • NEW YORK 13, N. Y.

EXPORT DIVISION: 13 EAST 40th STREET, NEW YORK 16, N. Y. CABLES: "ARLAB"

...Another Crucible Service for Magnet Users

160,000

ampere turn, impulse magnetizer now available

Magnet users are reducing manufacturing costs and improving their products through the use of this new, capacitor discharge-type, impulse magnetizer — another example of Crucible's leadership in serving industry.

This Crucible development has an improved firing circuit . . . is more compact . . . requires less maintenance . . . and results in more efficient magnetization.

For further information on the availability and operation of the Crucible Impulse Magnetizer, write to Crucible Steel Company of America, General Sales Offices, Oliver Building, Pittsburgh, Pa.

CRUCIBLE first name in special purpose steels

53 *years of Fine steelmaking*

ALNICO PERMANENT MAGNETS

CRUCIBLE STEEL COMPANY OF AMERICA, GENERAL SALES OFFICES, OLIVER BUILDING, PITTSBURGH, PA.

STAINLESS • REX HIGH SPEED • TOOL • ALLOY • MACHINERY • SPECIAL PURPOSE STEELS

NEWS and NEW PRODUCTS

October 1953

RF-AF-Crystal Marker-TV Bar Generator

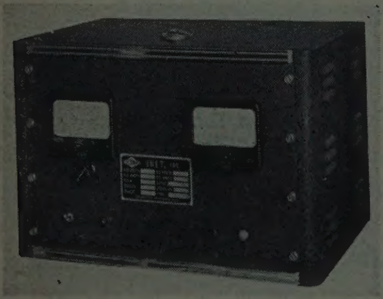
Electronic Measurements Corp., 280 Lafayette St., New York, N. Y., has announced a new RF-AF-Crystal Marker-TV Bar Generator.

RF-AF-CRYSTAL MARKER
TV BAR GENERATOR

EMC Model 700 gives complete coverage from 18 cps to 108 mc on fundamentals. It provides a bar generator for TV adjustment with a variable number of bars available for horizontal or vertical alignment, plus a square-wave generator to 20 kc. It contains a Wienbridge af oscillator with sine wave output from 18 cps to 300 kc and crystal marker and amplitude control. Other features include individually tuned coils, constant rf output impedance, stepped rf attenuator, electro-statically shielded transformer, thorough shielding, Colpitts rf oscillator from 300 kc to 108 mc on fundamentals—up to 216 mc on second harmonic and variable percentage of modulation. EMC Model 700 is priced at $55.90.

Low-Cost Rectifier Unit

Designated "MagniVolt," a new type high-performance ac-to-dc regulated selenium rectifier with magnitic amplifier control, which provides closely regulated dc power in a dependable, compact, low cost unit is available from **Inet, Inc.,** 8655 S. Main St., Los Angeles 3, Calif.



Regulation is better than ±0.1 per cent from no load to full load with ±10 per cent ac line variation. Response is faster than 0.2 second under extreme load conditions. Ripple is less than 0.1 per cent R.M.S. (to 0.1 per cent at extra cost). DC output ratings are 1.2 to 30.0 volts dc, and 2.5 to 40.0 amperes full loads. AC input is 115 volts, single phase, 60 cps.

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

Oscilloscope

The Colorscope, a new triple-channel ocsilloscope which permit simultaneous viewing of three color signals, was announced today by the **Electronic Tube Corp.,** 1200 E. Mermaid Lane, Philadelphia 18, Pa. This oscilloscope was designed to monitor color television broadcasting in the studio or at the transmitter site.

The recent adoption of the RCA-NBC system of color TV transmission by the National Television System Committee (as well as by CBS, Sylvania, and Philco) as a recommended standard has made widespread color telecasting virtually assured in the near future. Since the system provides for breakdown of colors into three separate color signals, red, blue, and yellow, it will be essential that transmitting stations maintain the necessary balance between these signals during transmission. For this reason, present and prospective color TV stations are faced with quickly developing new techniques and with obtaining suitable indicating equipment to meet the exacting commercial color transmission requirements. This instrument presents the three NTSC color signals on the face of a single cathode-ray tube, facilitating instantaneous comparison at a single glance.

Heart of the Colorscope is a special 5-inch flat-faced cathode-ray tube. In addition to supplying three in individual traces, the tube's design insures that the sweep time-base of the three color signals will be the same. Since accurate comparison of the signals can only be made under identical sweep conditions, this feature eliminates constant rechecking of the three sweeps and considerably simplifies color TV transmission monitoring.

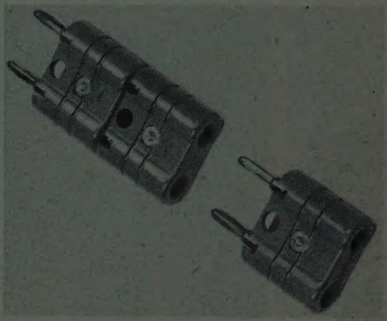
The Colorscope employs independent wide-range vertical amplifiers and a common horizontal amplifier. Vertical amplifiers have a frequency range from 10 cps to 4 mc±db with a deflection sensitivity of 0.1 volts per inch. The horizontal amplifier has a response from 0 to 500 kc±db. Deflection sensitivity is 4 volts dc per inch, and input coupling is direct.

The linear sweep generator is continuously variable from 0.02 seconds per inch to 2 microseconds per inch with a sweep leg of but 0.1 microseconds maximum. Trigger requirements are 0.5 to 50 volts peak for outside triggering; signal under deflection producing a 0.2 inch minimum deflection for internal.

A 60 cps square wave calibrator is integral in the Colorscope. Supplying 0 to 0.5 volts peak to peak, it may be switched to the inputs of all three vertical amplifiers.

Banana Plugs

The National Co., Inc., Components Div., 61 Sherman St., Malden, Mass., has announced production of a new type of Banana Plug.

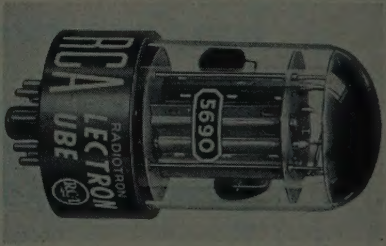


This plug, the FWT, has many advantages over previous types. Molded of mica filled bakelite in accordance with JAN specifications, it is styled for easy gripping. Leads can be brought directly from the base of the prongs or through a hole at the bottom of the plug. The top of the plug has been designed to accept additional plugs. All contacts and screws are nickel-plated brass.

Drawings, specifications and prices may be obtained by writing to the manufacturer.

Full-Wave Vacuum Rectifier

Tube Dept., Radio Corp. of America, Harrison, N. J., has developed the 5690, a "Special Red" vacuum rectifier tube, designed for industrial and aircraft application.



Model 5690 has two separate diode units of the indirectly heated cathode type. It is conservatively rated to withstand a maximum peak inverse plate voltage of 1120 volts, a maximum peak current-per-plate of 375 milliamperes, and a maximum dc output current-per-plate of 75 milliamperes.

When operated within maximum ratings, tube life should be 10,000 hours.

The structural design of this new tube makes it capable of withstanding continuous vibration of 2.5 g at a frequency of approximately 25 cps for hundreds of hours at maximum rated voltage. It is also capable of withstanding impact shocks of 500 g for short time periods at maximum rated voltages.

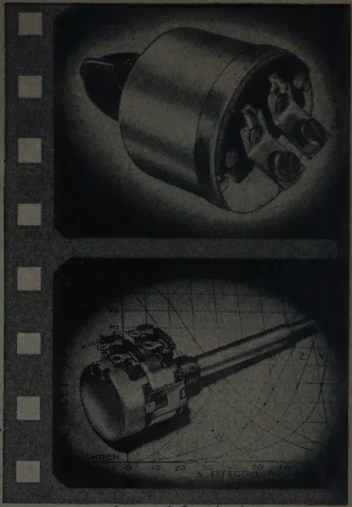
(Continued on page 52A)

when the circuit reads

come to

WIRE-WOUND and CARBON

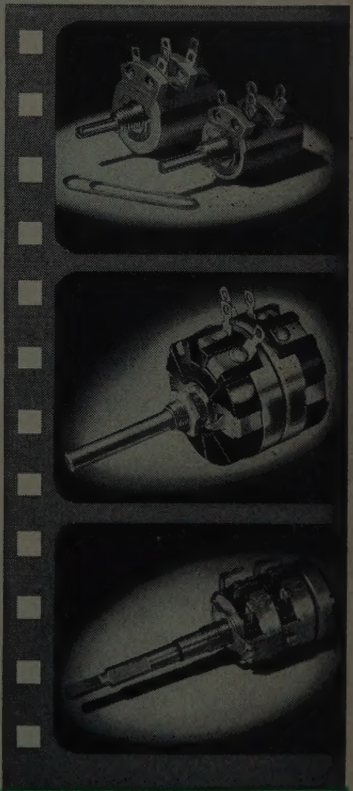
CONTROL HEADQUARTERS



You name it — we supply it. Most likely it's a *standard* number, for Clarostat's outstanding line provides the widest range of wire-wound and carbon controls in meeting usual needs. That means immediate delivery from factory stock. And for single pieces or small lots, wanted in a hurry, your local Clarostat distributor carries a representative inventory.

But if your control requirements are extraordinary, then Clarostat can design, tool-up and swing into full-scale production on your *specials*, in jig time.

Remember always that, from miniaturized carbon and wire-wound controls, to standard-sized controls, and again to all sorts of single and tandem units, shafts and switches, broad and tight tolerances, any tapers and taps, "You Can Stand Pat with Clarostat" for your simple or difficult control needs.



Exceptional engineering, tool-designing and manufacturing facilities second to none, are standing by for you at Clarostat. Let us collaborate on your control requirements, here at "Controls Headquarters".

STAND PAT WITH

CLAROSTAT Controls & Resistors

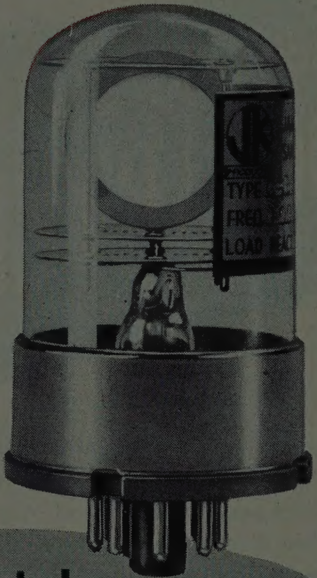
CLAROSTAT MFG. CO., INC., DOVER, NEW HAMPSHIRE
In Canada: Canadian Marconi Co., Ltd., Toronto, Ontario

JK PRODUCTS

Speeding Electronic Progress

through crystal research

This new JK G-12 is designed for ultra stable frequency control in applications such as frequency standards, timing and counting circuits, broadcast equipment and frequency monitors. Electrodes are deposited directly on the large, precision-made quartz plate shockmounted in an evacuated glass envelope. Frequency range 500 kc to 1500 kc. Crystal may be designed for a minimum temperature coefficient of from 0°C to 50°C or for temperature controlled operation at 60°C with a JKO7E-115V Oven. Approximate height above chassis, 2¾″. Maximum diameter of octal base, 1¾″. Consult us on specific applications.



JK STABILIZED G-12 CRYSTAL
For the "Difficult" 500 kc to 1500 kc Range

Tomorrow's Crystals

The increasing demand for ultra-stable frequency control to meet today's new requirements has necessitated a new approach to crystal design. Evacuated glass envelopes — for maximum protection and freedom from contamination — are a part of the new design of JK Crystals for the Critical. Consult us on your requirements for crystals of this advanced design.

THE JAMES KNIGHTS COMPANY,
SANDWICH, ILLINOIS

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 52A)

High Speed Counter

Several improvements in their Decavider 100-1 have been announced by **Decade Instrument Co.**, Box 153, Caldwell, N. J. The Decavider 100-1 is a precision high speed counter for use in extending the range of standard 100,000 cps counters to 1 mc. One of the new features consists of an output circuit providing square waves at one-tenth of the input frequency. Another output circuit furnishes sharp positive, or negative, going pulses having a rise time of 0.25 microsecond at an amplitude of 40 volts.

Use of the square wave output into conventional 100 kc counters permits accurate counting at input frequencies well over 1 mc, with little possibility of spurious readings over a very wide range of control-knob settings. Counters that require polarized sharp pulses will respond to the Decavider pulse output.

Input requirements are 100 millivolts, 100 cps to 1.2 mc. Dimensions are 18 wide ×10 high ×12 inches deep; shipping weight is 36 pounds. Price $295.00 f.o.b. Caldwell.

Bulletins on this and other instruments of the Decade family will be supplied on request.

Compact High-Rate Storage Cells

Yardney Electric Corp., 105 Chambers St., New York 7, N. Y., manufacturers of rechargeable storage batteries announces the addition of several new high-capacity models to their line of silver-zinc alkaline cells. These new models, known as "HR85" and "HR90" feature unusually high discharge currents and are rated conservatively at 100 ampere-hours.

The entire line of silvercells is said to be up to six times lighter and five times smaller than ordinary storage cells of comparable capacity. Spillproof and highly efficient, these units have completed successfully tests under extreme conditions of shock, vibration and acceleration. Further features of these cells are their freedom from corrosive fumes, vapors, spray, and gassing, their high discharge rates, and the flat output voltage characteristics.

These components range in capacity from ½ to over 100 ampere-hours. Yardney will supply a brochure and technical data sheets, as well as convenient pocket-size Application Guide, free of charge upon request.

(Continued on page 114A)

PROCEEDINGS OF THE I.R.E.®

Published Monthly by
The Institute of Radio Engineers, Inc.

VOLUME 41 *October, 1953* NUMBER 10

EDITORIAL DEPARTMENT
Alfred N. Goldsmith
Editor
E. K. Gannett
Administrative Editor
Marita D. Sands
Assistant Editor

●

ADVERTISING DEPARTMENT
William C. Copp
Advertising Manager
Lillian Petranek
Assistant Advertising Manager

●

BOARD OF EDITORS
Alfred N. Goldsmith
Chairman

PAPERS REVIEW COMMITTEE
George F. Metcalf
Chairman

ADMINISTRATIVE COMMITTEE OF THE BOARD OF EDITORS
Alfred N. Goldsmith
Chairman

Reg. U. S. Pat. Off.

Responsibility for the contents of papers published in the PROCEEDINGS OF THE I.R.E. rests upon the authors. Statements made in papers are not binding on the Institute or its members.

All rights of publication including translation into foreign languages, are reserved by the Institute. Abstracts of papers with mention of their source may be printed. Requests for republication privileges should be addressed to The Institute of Radio Engineers.

MEMBER AUDIT BUREAU OF CIRCULATIONS

PROCEEDINGS OF THE I.R.E.

Acknowledgment........................The Administrative Editor 1219
The Computer Issue........................Werner Buchholz 1220
4687. Computing Bit by Bit or Digital Computers Made Easy........................Arthur L. Samuel 1223
4688. Can Machines Think?........................M. V. Wilkes 1230
4689. Computers and Automata........................Claude E. Shannon 1234
4690. Electronic Computers and Telephone Switching....W. D. Lewis 1242
4691. Fundamentals of Digital Computer Programming........................Walker H. Thomas 1245
4692. Influence of Programming Techniques on the Design of Computers........................Grace M. Hopper and John W. Mauchly 1250
4693. Analogue vs. Digital Computers—A Comparison. Morris Rubinoff 1254
4694. The System Design of the IBM Type 701 Computer........................Werner Buchholz 1262
4695. Engineering Description of the IBM Type 701 Computer........................Clarence E. Frizzell 1275
4696. The Arithmetic Element of the IBM Type 701 Computer........................Harold D. Ross, Jr. 1287
4697. The SWAC—Design Features and Operating Experience........ H. D. Huskey, R. Thorensen, B. F. Ambrosio, and E. C. Yowell 1294
4698. SEAC...Sidney Greenwald, R. C. Haueter, and S. N. Alexander 1300
4699. Electronic Circuits of the NAREC Computer...Paul C. Sherertz 1313
4700. Diagnostic Programs for the Illiac........................David J. Wheeler and James E. Robertson 1320
4701. The Logistics Computer........................R. S. Erickson 1325
4702. The Remington Rand Type 409-2 Electronic Computer........................Loring P. Crosman 1332
4703. An Automatic Telephone System Employing Magnetic Drum Memory..................W. A. Malthaner and H. E. Vaughan 1341
4704. Machine Aid for Switching Circuit Design........................Claude E. Shannon and Edward F. Moore 1348
4705. The Design of the Bendix Digital Differential Analyzer........................Max Palevsky 1352
4706. Theory of Logical Nets...Arthur W. Burks and Jesse B. Wright 1357
4707. Elements of Boolean Algebra for the Study of Information-Handling Systems........................Robert Serrell 1366
4708. Dynamic Circuit Techniques Used in SEAC and DYSEAC........................Robert D. Elbourn and Richard P. Witt 1380
4709. The Design of Logical OR-AND-OR Pyramids for Digital Computers..S. E. Gluck, H. J. Gray, Jr., C. T. Leondes, and M. Rubinoff 1388
4710. A Survey of Digital Computer Memory Systems........................J. P. Eckert, Jr. 1393
4711. A Myriabit Magnetic-Core Matrix Memory...Jan A. Rajchman 1407
4712. Photographic Techniques for Information Storage..............Gilbert W. King, George W. Brown, and Louis N. Ridenour 1421
4713. The Logical Principles of a New Kind of Binary Counter........................Willis H. Ware 1429
4714. Combined Reading and Writing on a Magnetic Drum........................J. H. McGuigan 1438
4715. A Transistor Pulse Amplifier Using External Regeneration........................J. H. Vogelsong 1444
4716. Coded Decimal Number Systems for Digital Computers........................Garland S. White 1450
4717. An Electromagnetic Clutch for High Accelerations........................S. M. Oster and L. D. Wilson 1453
4718. A Survey of Analog-to-Digital Converters...Harry E. Burke, Jr. 1455

Contents continued, following page

PROCEEDINGS OF THE I.R.E.®

Published Monthly by

The Institute of Radio Engineers, Inc.

BOARD OF DIRECTORS, 1953

J. W. McRae
President

S. R. Kantebet
Vice-President

W. R. G. Baker
Treasurer

Haraden Pratt
Secretary

Alfred N. Goldsmith
Editor

I. S. Coggeshall
Senior Past President

D. B. Sinclair
Junior Past President

1953

R. D. Bennett
G. H. Browning (R1)
W. H. Doherty
A. W. Graf (R5)
W. R. Hewlett
A. V. Loughren
R. L. Sink (R7)
G. R. Town
Irving Wolff (R3)

1953–1954

J. T. Henderson (R8)
C. A. Priest (R4)
J. R. Ragazzini (R2)
J. D. Ryder
A. W. Straiton (R6)
Ernst Weber

1953–1955

S. L. Bailey
B. E. Shackelford

●

Harold R. Zeamans
General Counsel

●

George W. Bailey
Executive Secretary

Laurence G. Cumming
Technical Secretary

●

Changes of address (with advance notice of fifteen days) and communications regarding subscriptions and payments should be mailed to the Secretary of the Institute, at 450 Ahnaip St., Menasha, Wisconsin, or 1 East 79 Street, New York 21, N. Y.

• Numerals in parentheses following Directors' names designate Region number.

4719. An Analog-to-Digital Converter for Serial Computing Machines.................H. J. Gray, Jr., P. V. Levonian, and M. Rubinoff 1462
4720. Effectiveness of Two-Step Smoothing in Digital Control Computers.................Robert E. Spero 1465
4721. An AM-FM Electronic Analog Multiplier....William A. McCool 1470
4722. The Magnetic Amplifier as an Analog Computer Component.................Leonard J. Craig 1477
4723. An Input-Output Unit for Analog Computers.................P. R. Vance and D. L. Haas 1483
4724. Application of Electronic Differential Analyzers to Engineering Problems.................C. A. Meneley and C. D. Morrill 1487
4725. The Solution of Partial Differential Equations by Difference Methods Using the Electronic Differential Analyzer.................Robert M. Howe and Vincent S. Haneman, Jr. 1497
4726. Analog Computing Applied to Noise Studies......R. R. Bennett 1509
4727. Economic Analogs.................Otto J. M. Smith 1514

Correspondence:

4728. "An Historical Note of the Autocorrelation Function".................Paul E. Green, Jr. 1519
4729. "AC Circuits".................David W. Spence 1520
4730. "Echo Distortion in the FM Transmission of Frequency-Division Multiplex".................R. G. Medhurst 1520
Contributors to PROCEEDINGS OF THE I.R.E.................. 1522

INSTITUTE NEWS AND RADIO NOTES SECTION

News.................1531
Technical Committee Notes.................1532
Committees of the Professional Group on Electronic Computers.......1532
Radio Fall Meeting Program.................1533
Conference on Radio Meteorology.................1534
Computer Publications.................1542
Institute Committees—1953.................1542
Technical Committees—1953–1954.................1543
Institute Representatives in Colleges—1953.................1547
Institute Representatives on Other Bodies—1953.................1548
IRE People.................1549

Books:

4731. "Thermionic Vacuum Tubes" by W. H. Aldous and Sir Edward Appleton.................Reviewed by Scott Helt 1550
4732. "How to Improve the Utilization of Engineering Manpower." Prepared by the National Society of Professional Engineers............Reviewed by John L. Callahan 1550
4733. "Vacuum-Tube Oscillators" by William A. Edson......Reviewed by J. R. Pierce 1550
4734. "English-French Dictionary, of Terms Relative to Electrotechnique, Electronic and Joint Applications" by H. Piraux................. 1550
4735. "Faster Than Thought" edited by B. V. Bowden......Reviewed by W. Buchholz 1550
4736. "Principles of Color Photography" by R. M. Evans, W. T. Hanson, Jr. and W. L. Brewer.................Reviewed by W. T. Wintringham 1552
4737. "Filter Design Data for Communication Engineers" by J. H. Mole.................Reviewed by W. W. Tuttle 1552
4738. "Teamwork in Research" edited by G. P. Bush and L. H. Hattery.................Reviewed by Ralph I. Cole 1552
4739. "Mass Spectroscopy in Physics Research—National Bureau of Standards Circular 522".................Reviewed by R. E. Lapp 1553
4740. "Wave Propagation in Periodic Structures" by Leon Brillouin.................Reviewed by Seymour B. Cohn 1553
4741. "Radiotron Designer's Handbook—Fourth Edition" edited by F. Langford-Smith.................Reviewed by Kerim Onder 1553
4742. Abstracts and References.................1554

ADVERTISING SECTION

Meetings with Exhibits........ 2A
News—New Products.......... 24A
Industrial Engineering Notes.. 82A
Section Meetings............ 94A
Membership................ 94A
Professional Group Meetings.. 110A
Positions Open............. 145A
Positions Wanted............ 162A
Advertising Index............ 188A

Copyright 1953, by The Institute of Radio Engineers, Inc.

ACKNOWLEDGMENT

The reader will immediately recognize that this issue of the PROCEEDINGS differs from a regular issue in two important respects: First, it is a special issue devoted wholly to a single subject, namely, Electronic Computers. Secondly, it has been expanded to approximately three times the size of a regular issue. But perhaps the most noteworthy feature of this issue is the fact that it was assembled with the full collaboration of the IRE Professional Group on Electronic Computers (PGEC).

The Editorial Department is most grateful to J. H. Howard and M. M. Astrahan, PGEC Chairman and past Chairman, respectively, and to the Administrative Committee of the Group for their generous cooperation and helpful guidance in planning this issue. Special thanks are due to the PGEC Editorial Board and Papers Review Committee which, under the chairmanship of Werner Buchholz, reviewed the many papers submitted for the issue, brought about the inclusion of informative introductory and tutorial material, and arranged the papers in a coordinated sequence.

That the PGEC was in a position to render such substantial assistance in preparing this issue is a significant commentary on the extent to which this Group, and indeed all twenty-one Professional Groups, have developed in a few short years. In the two years since its formation, the PGEC has grown into a thriving organization of 2,000 members which issues its own technical publications, annually co-sponsors computer conferences on each coast, sponsors sessions at the IRE National Convention, and has organized local Chapters which hold meetings in conjunction with IRE Sections in Los Angeles, Philadelphia, San Francisco, and Washington, D. C. Additional Chapters are being formed in Boston, New York, and Detroit.

Of these many activities, perhaps the most important is the technical publication, called *Transactions*, which is issued quarterly to all members who have paid the $2.00 Group assessment. PGEC members have found the *Transactions* to be an invaluable source of authoritative information on the latest computer developments.

To these accomplishments of the PGEC must now be added a major share of the credit for the Computer Issue. And as the reader peruses the following pages, it is felt he will be quick to agree that the credit is well deserved.

—*The Administrative Editor*

The Computer Issue

WERNER BUCHHOLZ

The following guest editorial by Werner Buchholz is required reading for every reader of this issue. In it, the author provides the reader with a concise and invaluable guide to the significance of each paper presented herein together with an informative discussion of the growth of Electronic Computers as a branch of the radio engineering field.

Werner Buchholz is admirably qualified to introduce the reader to this issue by virtue of his position as Chairman of the Editorial Board and Papers Review Committee of the IRE Professional Group on Electronic Computers, to which fell the task of reviewing all the papers in this issue.—*The Administrative Editor*

About a year ago the IRE devoted a special issue of the PROCEEDINGS to one tiny component, the transistor, because its development promised to be one of the major advances in electronics. The present issue focuses attention on some of the largest assemblies of electronic components ever made, electronic computers. These machines frequently contain several thousand vacuum tubes each, and they are probably the most complex pieces of equipment of any kind ever assembled which have to operate as a single, centrally coordinated system, where each function depends on the correct operation of almost every component. The design of a successful computer demands a high degree of engineering skill, and the papers in this issue reflect the amount of engineering effort that has been expended in this rapidly growing field.

The urgent expansion of the electronic computer industry can be gauged by the many personnel advertisements appearing in the professional journals and the daily newspapers. The current situation is comparable to the rapid development of radar during World War II. Another sign of growth is the development of the IRE Professional Group on Electronic Computers: it has grown in just two years to be the third largest Professional Group in the IRE, having 2,000 members.

The PGEC co-operated with the Editorial Department of the IRE in the preparation of this special issue of the PROCEEDINGS. The purpose of this issue is two-fold: To provide a set of stimulating and informative articles which would introduce the non-specialist reader to the new and exciting field of electronic computer engineering, and to furnish the specialist with a single volume of reference material on a wide variety of computer subjects. This issue of the PROCEEDINGS thus gives recognition to the work being done by a young, but active, Group in the IRE. In the future the IRE will, of course, continue its usual publication policy: The normal outlet for the more specialized computer articles will be the quarterly *Transactions* of the Professional Group on Electronic Computers, while contributions of more general interest or developments of major significance will appear in the PROCEEDINGS from time to time.

Although electronic computers are a fairly recent development, it is well to point out that automatic computers considerably antedate the "age of electronics." We might choose to ignore the work during earlier centuries of such pioneers as Babbage, who first formulated many of the basic principles of the modern computers one hundred years ago, but whose attempts to build one foundered because current technology proved inadequate. However, we must include the Bush Differential Analyzer and the punched-card machines of the 1920's as the direct ancestors of the machines described in this issue. The first realization in electro-mechanical form of most of Babbage's ideas came in 1944, when the IBM Automatic Sequence Controlled Calculator (the Mark I at Harvard) was completed. Still, the present growth of the computer industry did not start until the results of the enormous development of electronic technology during World War II were brought into the field. It is interesting to note that many computer projects started around a nucleus of wartime radar experts. Electronics not only provided the technological means for greatly increased speed and capacity, and thereby enhanced the usefulness of computers many times, but the availability of cheap, mass-produced components and of engineers trained to use them made it possible to experiment on a greater scale and at a lower capital investment than before. In the late

40's and until the early 50's ideas for new computers and their weird names sprouted in great abundance all over the world.

There was a significant time lag, however, between the announcement of many a computer and its first successful operation. During this time the designers had to face engineering realities. The low-cost components of the radio industry were found to be inadequate for the high-precision demands of a complex computer, and new components and methods of construction had to be devised. The high-speed electronic computer also required input-output equipment of adequate capacity, which meant extensive development of electromechanical devices. Finally, when the machines were finished, better techniques for using them had to be devised. The resultant operating experience led to further design improvements. The contents of this issue reflect the maturing effect of several years of actual operation.

In spite of this period of sober adjustment the industry has continued to grow. Several electronic computers are in commercial quantity production; one type of machine alone accounts for two million tube sockets now in active computer service. Computers have become indispensable for engineering calculations in defense industries, particularly in the aircraft industry. Even more are being built for accounting applications to cope with the problems of an economy of ever-growing complexity. Thus electronic computing may soon affect the average person as much, if not as obviously, as radio and television; it is certainly of vital interest to the electronics engineer.

The Contents of this Issue

The Computer Issue starts with a series of invited articles by A. L. Samuel, M. V. Wilkes, and C. E. Shannon. These well-known authors discuss the nature, uses, and the limitations of computers, and touch on possible further developments in their imaginative and eminently readable papers.

In the next paper electronic computers are looked at from the point of view of the telephone switching engineer, thus providing an interesting parallel (Lewis). One cannot have a real appreciation of the nature of digital computers until he is familiar with the fundamentals of programming a typical machine. A tutorial paper on this subject (Thomas) provides a background which applies to most of the present-day digital computers even though they differ in detail. Basically, programming is a simple, logical procedure, but as the problems to be solved grow, the labor of programming also increases, and the aid of the computer is enlisted to devise its own programs (Hopper and Mauchly). To round out this series of papers there is a comparison of digital and analog computers (Rubinoff).

No computer publication would be complete without an account of some of the important digital-computer projects in existence: their purpose, their design, and current operating experience. The Type 701 Computer, a large-scale machine which IBM is producing in quantity, is described in a set of papers covering the over-all system design (Buchholz), the engineering design (Frizzell), and the arithmetic element (Ross). The SWAC (Huskey, Thorensen, Ambrosio, and Yowell) and the SEAC (Greenwald, Alexander, and Haueter) of the Bureau of Standards, and the NAREC of the Naval Research Laboratory (Sherertz) are representative of the work being done by government agencies. The problems of servicing a large, general-purpose digital computer are eased by the fact that the computer itself serves as its own test instrument; the ILLIAC at the University of Illinois serves as an example (Wheeler, Robertson). From Remington Rand, Inc. come descriptions of two plugboard-controlled computers: the Logistics Computer (Erickson) and the Type 409-2 Computer (Crosman). The last one is an example of a class of much smaller electronic computers of less capacity which are being produced by several companies in larger quantities for accounting purposes. The Bell Telephone Laboratories have constructed two exploratory, special-purpose machines: one to investigate the possibility of an electronically-controlled telephone exchange (Malthaner and Vaughan), and the other to aid in the analysis of relay circuits (Shannon and Moore). Both machines illustrate the fact that computers do not necessarily compute on numbers; these machines apply to switching and combinatorial problems, and techniques intended for numerical work are not very efficient on them. Although the large, "general-purpose" computers are extremely fast on numerical problems, a simple combinatorial problem as determining the best interconnection of a few relays can slow them down to a walk. "General-purpose" is a relative term.

Analog computers are generally described as using continuously variable functions. There is possibly one exception, the Digital Differential Analyzer, which solves problems in much the same manner as an analog differential analyzer, but which uses digital circuits, digital arithmetic, digital programming, and which provides a digital output. An improved version designed at the Bendix Aviation Corporation is discussed (Palevsky). This interesting type of machine bridges the gap between digital and analog computers. It shows that the two techniques do not represent separate and competing schools of thought, as is commonly assumed. One may expect digital or analog methods to be applied where each is best suited.

Next comes a series of papers on theories, techniques, and components useful in designing digital computers. The reader interested in theory will find the foundation laid for the study of a digital computer as a single large network, and the physical realizability of a given logical net is discussed (Burks and Wright). A tutorial paper on Boolean algebra gives the circuit designer a thorough and precise exposition of this important design technique (Serrell). A detailed account is given of a new design of standard circuit packages for the SEAC type of computer (Elbourn and Witt). These circuits have been used as prototypes by other computer projects, and already further improvements in the design of logical switching circuits are reported (Gluck, Gray, Leondes, and Rubinoff). Under the heading of storage there is an extensive survey of memory systems as evaluated by one of the pioneers in digital-computer engineering (Eckert), and another paper gives an idea of the effort being put into developing the still relatively new magnetic-core storage elements into a practical, large-scale, random-access memory system (Rajchman). Photographic techniques, which have been highly developed elsewhere, provide some excellent possibilities for computer storage which are outlined (King, Brown, and Ridenour). They have so far gone largely unnoticed because of obvious technical difficulties, but it should be a fruitful area of research. A binary counter (Ware) and a magnetic-drum recording technique (McGuigan) are presented, shedding some new light on well-explored territory. Two of the biggest handicaps of large computers are their very size and power requirements, for which it is hoped that the transistor, replacing the vacuum tube amplifier, will eventually offer a solution (Vogelsong). Computers operating in the decimal system require a code to represent the decimal digits; the number of variations and different considerations involved is surprisingly large (White). The inclusion in an IRE publication of a paper on the design of a mechanical device may be a little surprising, but it points out the important contribution of good mechanical design to the success of electronic computers (Oster and Wilson).

One use of digital computers is to digest large amounts of raw data produced by measuring instruments, in a windtunnel, for instance, and to put out finished results in tabular form. This data-processing application is closely related to commercial accounting problems, and standard accounting machines are frequently used here for computing, except that the input data are in analog form. This requires conversion of the data from analog to digital form. Various methods are surveyed in one paper (Burke) while another dedescribes a specific conversion technique (Gray, Levonian, and Rubinoff). Yet another use of the digital computer is as a control element, where it must communicate directly with the outside world, usually by continuous variables of the analog type, and be able to smooth out any noise contained in the input (Spero). Here again we see the close relation between analog and digital techniques in certain applications.

In the area of analog computers proper there are three papers dealing with new components: a multiplier (McCool), a magnetic amplifier (Craig), and an input-output unit capable of plotting a graph and automatically reading it back (Vance and Haas). Many different kinds of problems suitable for solving on the electronic analog computers (differential analyzers) in existence are indicated (Meneley and Morrill), the extension of analog computing to partial differential equations by the use of difference techniques is discussed (Howe and Haneman), and an application to noise studies is shown (Bennett). The paper on economic analogs (Smith) should be of wide interest because it shows that economic systems are feedback systems similar to servomechanisms, and analog computers can be used in studying economic models. This opens the possibility that major business policy decisions might in future be based on computer studies just as engineering decisions are today.

Finally the reader's attention might be drawn to the review of a new book on computers. In view of the scarcity of books in any rapidly expanding field, the publication of a new text is always of interest.

Computing Bit by Bit or Digital Computers Made Easy*

ARTHUR L. SAMUEL†, FELLOW, IRE

Since many readers may not be familiar with the technical language used by the computer engineer, particularly in the field of digital computing, the Editors asked A. L. Samuel to write an informal, but informative, introductory paper. Dr. Samuel, who is a Fellow of the IRE, is in charge of physical and chemical research related to the development of computer components at the IBM Laboratory in Poughkeepsie, N. Y. His broad interest and his close association with several computer projects qualify him to interpret the efforts of the computer designer to the non-specialist.—*The Editor*

THE POPULAR PRESS has had a great deal to say about "mechanical brains," so much so in fact that the first task for a paper of this sort might be that of placing the modern digital computer in the right perspective. However, the writer believes that you, the reader, are perfectly able to draw your own conclusions once you are presented with the facts. Your conclusion may well be that we are witnessing a revolution, akin to the industrial revolution, in which mankind will now be freed of the mental drudgery which has replaced the drudgery of unremitting manual labor. Or again, you may conclude that the modern digital computer has been oversold to the public and that there is still a long mental row to hoe before we will reach Utopia. Perhaps the truth lies somewhere in between.

As an aid to the non-specialist, this paper will attempt to explain in an elementary fashion the how's and why's of the modern digital computer and in so doing, to introduce some of the "lingo" of the computer engineer. This should give the reader an initial basis for judging for himself the role the modern computer appears destined to play in the future, and it may help him to read the more highly technical papers which follow. The paper will then briefly review those aspects of scientific research and engineering development as applied to computers in which the greatest opportunities for improvements seems to lie.

THE NEED FOR COMPUTERS

It is hardly necessary to point out the need for automatic calculators in view of the obvious advantages in terms of the reductions in clerical manpower and woman power which result from their use. The fact that such computers make possible a form of numerical experimentation which has never before been exploited, is perhaps somewhat less obvious. We are all aware of the existence of involved mathematical problems which are so lengthy and complicated that mankind has not been able to make even a start on their solution. The accurate forecasting of the weather, which certainly must depend upon the interaction of measurable effects, but in a very complicated and involved fashion, is but one example of a host of enticing problems which demand solution and which are for the first time coming within range. While a great deal of progress has been made in mechanizing office procedures, we all realize that only a small fraction of the entire job has been attempted. And finally, with the increasing mechanization of industry, the need for calculations as a part of automatic control is becoming more obvious. I think that we will all agree that there exists a real need for automatic calculators and that this need is increasing at a remarkable rate.

At first glance, a computer is a very complex device. It can be looked at from two different angles, which Professor Hartree[1] has called the "anatomical" and the "physiological," that is, "of what is it made?" and "how does it tick?" As engineers and scientists you can be expected to know something about its anatomy. It is made up of the same building blocks you know so well; resistors, condensers, magnetic cores, vacuum tubes, diodes, yes, maybe even transistors. These are put together into circuits which differ in detail it is true, but in detail only from many very familiar circuits. The "anatomy" is familiar, but the "physiology," the way these components work together to do computing, this is unique to the digital computer. An "introduction to physiology" seems to be in order.

THE COMPUTER IN FUNCTIONAL TERMS

What then is a computer in functional terms? Any computer can be thought of as an information or data processing device which accepts data in one form and delivers it in an altered form. This is as true for the

---

* Decimal classificaton: 621.375.2. Original manuscript received by the Institute, August 12, 1953.

† International Business Machines Corp., Poughkeepsie, N. Y.

[1] D. R. Hartree, "Calculating Instruments and Machines," University of Illinois Press, p. 56; 1949.

modern high-speed digital computer as it is for the adding machine and the lowly abacus. Just as we can understand the use of an adding machine without knowing in detail how the internal mechanism is constructed, we can as easily understand the largest digital computer.

Looked at from another point of view, when the human operator performs a reasonably complicated numerical calculation he is forcing his brain to act as a digital computer. Since all of us are capable of analyzing our own thought processes as we first of all break down the problem into its simple elements and then perform these simple computations, and we can do this incidentally with only the vaguest ideas of the way in which the individual brain cells operate, we should with equal facility be able to understand the operation of a device which is much less complicated than the human brain.

"Yes," you say, "that is all very well, but what is all this about digital versus analogue machines? What is the difference between a binary and a decimal machine? And what, pray tell, do you mean by a stored program?" Well let's just take things one at a time. Let us first of all briefly consider the analogue machine before proceeding to digital machines.[2]

THE ANALOGUE MACHINE

If words mean anything, an analogue machine must solve problems by analogy. Since there are many kinds of problems, and since it is frequently possible to devise many different analogies for any one class, there will be many types of machines which differ from each other in almost every conceivable way. Most of the problems of engineering, and many of the problems in physics deal with continuous parameters. One suspects that there will be parameters in the machine, perhaps shaft rotations or displacements, currents or voltages, which are expected to vary continuously in proportion to the real parameter and so simulate them. Furthermore, since the parameters in the real situation may be determined by relatively complex relationships, the machine must be able to relate various parameters according to these same mathematical rules. Since many of the laws of nature can be expressed in terms of integrations, integrators occupy a fairly prominent place in the analogue machine, at least in the more complicated ones. Sometimes the parameters employed in the machine are not proportional to the simulated parameters, but are related to them in some functional way. The slide rule, one of our simplest analogue machines, is a case in point. Here distances along the rule are not proportional to the quantities to be represented but rather to the logarithms of these quantities. This makes the device particularly suited for solving problems involving multiplication which is then performed by adding lengths proportional to the logarithms of the quantities to be multiplied. In summary, the analogue machine performs a specialized function in a very efficient manner and can frequently outperform a digital computer in the solution of specific types of problems.

COUNTING ON ONE'S FINGERS

A digital machine obviously uses digits, so it counts, and just as it is possible to do arithmetic by counting on one's fingers—it does arithmetic. In fact, some of the newer and larger machines are unbelievably naive. They do not even know how to count to ten; instead they can only count up to two. These machines are said to be binary.[3] We will have more to say about this later. An ordinary adding machine is a simple example of a digital computer. Any operation which can be reduced to arithmetic or to simple logic can be handled by such a machine. There does not seem to be any theoretical limit to the types of problems which can be handled in this way. The user may occasionally find, to his chagrin, that it is harder to reduce a given problem to arithmetic than it is to solve the problem by direct methods.

Fortunately, problems requiring the use of the modern digital computer have a habit of falling into classes. Solution methods have already been worked out or are currently being developed for many of these classes so that the work of analyzing a special problem may be limited to the task of identifying the class to which it belongs. This is a situation which will continue to improve with time, and particularly as more and more machines of the same type come into general use. Nevertheless, a great deal of thinking is required when one attempts to make use of a digital computer. Once this thinking has been done the computer makes up for the delay by its speed in arriving at the solution which may easily be 20,000 or 30,000 times as great as that of a man operating a desk calculator.

CAN COMPUTERS THINK?

It might be well, at this point, to dispel some of the fuzzy sensationalisms of the popular press regarding the ability of existing digital computers to think. Over a hundred years ago Lord Byron's daughter, Lady Lovelace, in commenting on Charles Babbage's analytical engine, made a remark which is as true today for the modern computer as it was then. She said, "The analytical engine has no pretentions whatever to originate anything. It can do whatever we know how to order it to perform."[4] More recently Dr. M. V. Wilkes, in his characteristic style, had some very illuminating things to say on this same subject.[5] The digital computer can and does relieve man of much of the burdensome detail of numerical calculations and of related logical operations, but perhaps it is more a matter of definition than of fact as to whether this constitutes thinking.

---

[2] For a comparison of analogue and digital machines see M. Rubinoff, "Analogue vs. digital computers—a comparison," PROC. I.R.E., pp. 1254–1262; this issue.

[3] Even so-called decimal machines usually make use of binary devices and must actually express each digit by its binary equivalent, or at least in terms of some coded equivalent. See G. S. White, "Coded decimal number systems for digital computers," PROC. I.R.E., pp. 1450–1452; this issue.

[4] R. Taylor, "Menebrea," Lf Scientific Memoirs (London Ed.), vol. 3, p. 722; 1842.

[5] M. V. Wilkes, "Can machines think?," *Discovery*; May 1953. (The editors have thought so highly of this paper that it is reprinted in PROC. I.R.E., pp. 1230–1234; this issue.

Regardless of what one calls the work of the digital computer, the unfortunate fact remains that more rather than less human thinking is required to solve a problem using a present day machine since every possible contingency which might arise during the course of the computation must be thought through in advance. The jocular advice recently published to the effect, "Don't Think! Let UNIVAC do it for you,"[6] cannot be taken seriously. Perhaps, if IBM's familiar motto needs amending, it should be "Think: Think harder when you use the 'ULTIMAC'."[7]

INFORMATION PROCESSING

We will start then by considering a digital computer as being merely an information processing device. This is the only thing that the computer does. *It cannot create any new information* not contained in the original source, although *it may transform the input information* into a very much more useful form. This is an important concept, and a full recognition of its implications will go a long way toward dispelling any mystical feelings with respect to the modern computer.

The input information to be processed may be the statement of a mathematical problem, the rules governing the mathematical operations to be performed, and the input data. It may be the statement of a problem in logic or, if one wishes, the rules for playing some game such as checkers or chess together with the conditions of the board at some particular time and a statement of the logic to be applied to determine the best next move. The digital computer is capable of handling all of these cases and more[8] but in every case it simply processes the input data according to rules specified by the operator. By analogy we might call the computer a mathematical translator in the same sense that a literary translator takes information in one language without adding or subtracting any basic information and renders this information intelligible to someone not understanding the original language.[9]

One aspect of this information-processing concept, as already intimated, has to do with the fact that the computer can, and does, make use of more than one source of information during the processing. One such source of information is the input data. A second source of information is the list of instructions. Still another source is, in effect, a rule book of mathematical and logical operations, which can by analogy be related to the translator's bilingual dictionary. This rule book may be built into the wiring of the machine, or it may be given to the machine, as needed, in the form of instructions.

We might express the idea of Information Processing by saying that a computer simply rearranges information from one spatial relationship at the input to the machine to another spatial array at the output. However, a moment's reflection will show that the machine must translate information not only in space but also in time. Consider a situation in which we tell the machine how to perform a series of operations. It is customary first to give the machine the program (or list of instructions) and, subsequently, to give it the numbers on which the operations are to be performed. The machine must, therefore, be able to remember the instructions at least until it receives the data on which it is to operate. In fact, since most of the required operations cannot be performed simultaneously, a continued use of memory or information storage is required.

SWITCHING AND STORAGE

Getting closer to the language used by computer engineers we can say that two functions are basic to any computer, these being information switching and information storage. By switching we mean changing the arrangement of information in space; while storage can be thought of as changing the time sequence of information. Switching and storage are frequently discussed as separate entities, although it is quite unusual for them to be actually separated, except in their simplest physical embodiments. Most so-called switching devices will on closer analysis be found to contain elements of memory or of information storage; while most storage devices in order to be at all effective must contain certain internal switching mechanisms.

To bring the discussion down to earth let us consider the ordinary electric light switch in your home. This is by definition a switch. It enables one to direct electric current to a lighting fixture at will. Usually there is a detent mechanism which enables the switch to remember what it is supposed to be doing so that once you turn the lights on they will remain on. It therefore has a memory. It is also a binary, or perhaps we should say a bistable device. By way of contrast, the ordinary telegrapher's key is a switch without memory since the key will remain down only as long as it is depressed by the operator's hand. Both the light switch and the telegraph key are binary devices, that is, they have but two operating states. While we are on the subject we might note that most of the switching and storage mechanisms which are employed in modern computers are also essentially binary in nature. Because of this, many of the larger machines operate in the binary number system.

---

[6] A. F. Draper, "Univac on election night," *Elec. Eng.*, vol. 72, pp. 291–293; April, 1953.

[7] A coined term for the "Ultimate in Automatic Computers." The reader may, if he prefers, insert any name he likes selected from the following partial list of existing machines: *Ace, Amos, Ape(x)c, Arc, Avadac, Bark, Binac, Cadac, Caldic, Circle, Cpc, Deuce, Dyseac, Edsac, Edvac, Elecom, Era-1103, Ferut, Flac, Hurricane, IBM-701, Illiac, Johniac, Leo, Lorpgac, Madm, Maniac, Midac, Mosaic, Narec, Nicholas, Oarac, Omibac, Oracle, Ordvac, Rascal, Raydac, Seac, Sec, Swac, Univac, Whirlwind, Wisc*, etc.

[8] Read C. E. Shannon, "Computers and automata," PROC. I.R.E., pp. 1234–1241; this issue.

[9] This reference to literary translation is something more than a simile since the use of digital computers for translating is already receiving serious consideration. The limited memory capacity of existing machines is the only real deterrent, although the problem of programming and coding is far from simple.

Of course, you can spoil all the fun by asking about the three-way switch on the common floor lamp and so bring up the subject of ternary arithmetic, but we will ignore this complication since no one has yet come up with a ternary machine.

COMPONENT DEVICES

In cataloging the basic mechanisms involved in a computer into switching and storage we have unwittingly discussed the computer as an entity and indeed this is one way to look at the problem. However, when one attempts to build a practical computer out of these two basic kinds of elements one finds it desirable to group the switching and storage elements into subassemblies which perform specialized functions in terms of the flow of information through the machine. Let us consider some of these functions.

In the first place we must get the information into and out of the machine. This calls for some sort of input device and one or more output devices. If the information is not presented to the machine in exactly the most convenient form, both with respect to its spatial and temporal relationships, we can expect the input device itself to contain both storage and switching functions. Then, since the operations to be performed on the input data are either logical or arithmetic there must of a consequence be a logical and arithmetical unit.[10] In some machines the only operation performed is that of addition, in which case this portion of the machine is simply called the adder. We certainly need an input device, an output device, and an adder or a logical and arithmetical unit.

Now let us consider how one would perform a simple multiplication. If you ask an assistant to multiply two, three or four digit numbers together, his first impulse will be to pick up a scrap of paper on which to write the two numbers to be multiplied.

By the way, we are going to run into trouble with nomenclature in the use of the term "number," which can mean either a digit or a group of digits. It might be well to adopt the computer engineer's terminology in which he may speak of "digits" but will use the term "word" to apply to a group of digits. Such an array of digits may, of course, have a non-numeric significance; a good example is an instruction. A purist will even object to the use of the term digit, since this implies a decimal machine and many modern machines are binary where the term "bit" is more appropriate. The most general term and the one obviously required for machines handling alphabetical as well as numerical data is the term "character."

So you have asked your assistant to multiply a couple of three or four-character "words" together. He starts by writing down the given words. He will then perform the operation of multiplication and will probably write down a number of additional "words" on the piece of paper, the so-called partial sums which he uses during the course of the calculation, but which of themselves are not the answer. This calls for a somewhat larger piece of paper than that which would be necessary to write the two given "words" and the "word" which represents the final answer. He is, in effect, using a piece of paper as a temporary storage device or supplementary memory to store "words" needed during the calculation. The scientific computer obviously needs just such a memory and a special portion of the machine is assigned this responsibility and is usually referred to as "the memory." As we will see later, it is customary to make this memory considerably larger than would be required to store temporary information of the type just mentioned and to store in this same memory most if not all of the instructions necessary to perform a rather lengthy calculation, much of the input data and a substantial part of the output data, or at least until enough has accumulated to keep the output device working continuously for a reasonable period of time.

As you may have noted, we have used the terms "storage" and "memory" more or less synonymously. This usage of the term memory to refer to certain types of storage has become quite common and some people have gone so far as to ascribe human attributes to digital computers. Any anthropomorphical implication of this sort in the use of the term memory should be dissipated when I remind you that the printed page is perhaps still our best information storage medium in terms of storage capacity and from this point of view it far surpasses the more glamorized types of memory currently used in computers. By memory, then, we will simply mean a specialized portion of the machine capable of providing information storage.

We have discussed input and output devices, the logical and arithmetical unit, and the memory. The only major part left is the control unit which forces these other components to work as a team. Control will largely involve switching although even here there will be some storage functions. For example, there will be a counting register to keep track of the current computational step being performed, other registers to remember which of the various possible input or output units are currently being employed, etc.

PROGRAMMING[11]

We are now at the nub of the problem—how does the control work? Well there are a variety of ways of varying degrees of complexity, but for simplicity we will discuss just two types which we will refer to as fixed programming and stored programming. By fixed programming we mean the kind of programming which controls your automatic dishwasher for example. Here the sequence of operations is fixed and built into the wiring of the control or sequencing unit. Once started, the dishwasher will proceed through a regular series of operations, washing, rinsing and drying. Of course, if one wished, one could change the wiring to alter the program. In many automatic calculators of the fixed program type this facility is provided in the form of a plugboard on which the wiring can be changed, or as a still further refinement, the plugboard itself is removable and quickly replaced by another previously wired board.

---

[10] One such form of unit is discussed in H. D. Ross, Jr., "The arithmetic element of the IBM type 701 computer," PROC. I.R.E., pp. 1287–1294; this issue.

[11] For a more detailed description of the logic of one type of programming, see W. H. Thomas, "Fundamentals of digital computer programming," PROC. I.R.E., pp. 1245–1249; this issue.

Lest you get the idea that this type of programming is as unimaginative and prosaic as a dishwasher let me remind you that considerable sophistication is possible. For example, one can cause some of the program steps to make tests and perhaps transfer control not to the next step in order but to some other step. Suppose one sets up a closed loop of steps which will do the same thing over and over again, a so-called iteration loop, perhaps to solve for some quantity by the method of successive approximations. It is easy enough to get such a loop started, but it is also necessary to stop it. This can be done by having as one step in the loop a computation of the difference between the last two approximations. Whenever this difference is close enough to zero (being smaller than some preassigned value) one can arrange to terminate the loop. A sort of judgment might be implied in such an operation but on more careful analysis the judgments were actually made by the programmer when he decided to terminate the loop in this way and when he picked the difference value. The machine simply tests as directed and uses the result of the tests in a manner which has been prescribed in advance. The term "programming" is obviously used to refer to those phases of the planning of a problem for a computer which consist of recording the steps required, the tests to be made, and the way in which the solution steps are to be altered as a result of these tests.

The Stored Program

And now we come to the concept of a stored program. . . . Suppose you wished to give your assistant a large number of instructions for manual computations all in advance. You could do this by supplying him with a prepared set of instructions, or you could dictate the instructions and have him write them down, perhaps at the top of the same sheet of paper on which he is later to perform the computations. Two different situations are here involved, although at first glance the distinction appears trivial. In the first case the instructions are stored on a separate instruction form, while in the second case they are stored by the same medium which is used for data. Both situations are found to exist in computing machines. The first case is exemplified by certain machines which use special program tapes. The second situation is becoming quite common in the newer machines and is the case usually meant when the term "stored program" is used.

To make the matter definite let us review some of the steps which might be required to store a program and to execute the program once it is stored. The machine operator must prepare a list of the instructions and a list of the input data, either on punched cards, on a punched tape, or perhaps on a magnetic tape, in any case on some medium which can be read by the input mechanism of the computer. The instructions could conceivably be in ordinary English but, obviously, it will be expedient to adopt some sort of shorthand notation or "code" in terms of numbers or letters which condenses the information as much as possible and presents it in a more convenient form for machine use. It is customary to have these instructions in the form of "words" which are similar in every respect to the "words" used to represent numerical quantities. This process of translating a program into the machine's language is called "coding."

Now consider a typical case where the start or load button on the operator's panel will only cause the machine to read-in the first two instructions and then transfer control to the first of these instructions. The reading operation will cause these two instructions to be stored in the first two positions in memory, but what happens then? Well, we see the need for at least two registers, one in the form of a program counter or register which keeps track of the program step number, or more generally of the address in memory from which the current instruction is to be obtained, and an instruction register into which the current instruction can be transferred in order to enable it to set up the necessary switching so that the instruction can be executed. The first instruction in the case we are considering would be one telling the machine to copy the next two instructions from the input device being used into the third and fourth positions in memory. By continuing in this way we can eventually introduce the instructions needed to execute the problem itself, since each copy instruction will require one instruction but will call in two new instructions. This is really all there is to it, but if the reader is left with the feeling that the matter is still far from clear he will do well to read another paper in this issue[12] which describes a much neater solution to the loading problem and one which is in current use for one type of machine.

Types of Instruction Codes

You will note that the typical instruction must consist of at least two parts, an operation part which tells the machine what to do, and an address part. During the loading operation just described, the operation part specified that information was to be accepted at the input to the machine while the address part specified where the information was to be stored. In other instructions the address part might specify where in memory one must go to get a desired word, while the operation part might specify that the word be sent to the adder, for example, but in any case at least one address must be provided. It should be observed that the instruction always contains the address of the word on which the operation is to be performed, rather than the word itself. This simplifies the substitution of new data into a problem since one can change the stored data without in any way altering the instructions. Machines based on this principle are called "Single Address Machines."

---

[12] W. Buchholz, "The system design of the IBM type 701 computer," Proc. I.R.E., pp. 1262–1275; this issue.

Some machines use instructions which do more than this. For example, one might have a "two address code," the first address being that of the word on which the operation is to be performed, and the second being the address at which the next instruction is located. If this is done, the machine does not require a program counter since it does not take instructions in the order they are listed but always in the order specified by these second addresses. As still another example one might have a "three address code," in which the first two addresses specify locations at which two desired words are to be found, and the third address specifies the location where the result of the operation (maybe the sum of the two original words) is to be stored. In this case, since no new instruction address is provided we would again depend on the program counter. Or again, one might design a machine using a "four address code" in which each instruction contains two input addresses, one output address, and the address of the next instruction. It is still a matter of some dispute as to which of these and various other possible systems is the best.

KINDS OF OPERATIONS

We still have not said anything about the kinds of operations the computer can perform. Here there is even more variation from machine to machine. However, we can classify the instructions into several logical categories. In the first place there must be a few instructions relating to the input and output devices used with the computer. One must be able to specify that an input or output device be operated and that data be copied from the input or to the output. Closely related to this, there must be instructions enabling one to store information in memory or to recall it as desired. Then, of course, there must be a number of mathematical operations such as add, subtract, multiply and divide. And finally there must be a number of control transfer operations which enable one to transfer the control to some specified instruction, either unconditionally or subject to some specified condition. For example, we might have a "transfer on zero" operation which will cause the control to be transferred to the instruction stored at the specified address if the result of the previous operation is zero. This could be used to terminate the iterative loop we mentioned earlier. Other conditional transfer operations frequently encountered are "transfer on plus," "transfer on minus" with obvious significance, or "transfer on overflow": that is if a previous operation has led to a result which exceeds the capacity of the machine.

VIRTUES OF THE STORED PROGRAM

We can now go back and consider one property of the "stored program" method of operation which is rather unique and which really must be understood to appreciate the full value of such a concept. This property is that of being able to operate on the instructions themselves just as if they were ordinary data. This means that the entire course of a computation can be altered, including the operations themselves, the choice of data on which the operations are to be performed, and the location at which the results are to be stored, and this can all be done on the basis of results obtained during the course of the calculations through the use of conditional transfer instructions. The clever programmer need not write out every operation which he wishes the machine to perform. Instead he works out procedures for portions of the problem and then arranges a master program which calls for these "sub-programs" as required, perhaps over and over again, and which causes the machine to modify and adapt these sub-programs as required during various stages in the solution. Programming, in its more advanced form, thus becomes an art. Much of the apparent complexity of the computer resides in the program rather than in the machine itself. It is interesting to speculate on the way in which improved programming techniques are sure to increase the usefulness of existing computers beyond the fondest hope of their designers and how they are apt to influence the design of future computers.[13]

LIMITATIONS OF PRACTICAL MACHINES

In concept, the modern digital computer is a universal machine since it can be made to simulate the behavior of any other special purpose machine, or to solve any problem which can be reduced to arithmetic. The practical machine falls short of this, both with respect to data handling capacity and speed.

Data handling capacity obviously refers primarily to the storage functions. It is a truism to say that better memory devices are needed. However, as intimated earlier, most practical storage devices have associated with them certain aspects of switching as well. What is really needed is a larger memory which contains a fast switching mechanism as an integral part. It is a lamentable fact that most memory devices with large potential capacity seem to involve slow switching mechanisms, while the faster switching devices are most easily associated with devices having limited storage capacity.

A complete discussion of the present day methods of handling this problem would lead us well beyond the scope of the present paper. We can note, however, that most modern machines employ a hierarchy of memory devices. A typical array might start with a punched card storage facility with substantially unlimited capacity but which is only capable of being "read" at say 150 characters a second. This will be supplemented with a magnetic tape storage facility which provides for "ordered" access to information at a very much faster rate of around 10,000 characters a second, but which is of limited utility if information is wanted in an order differing from that in which it is stored on the tape. Here again the capacity may be substantially infinite but the larger the capacity the more the time required to sort through many, many reels of tape to select the desired reel and then to read through this tape from end to end to locate the desired bit of information. The next hierarchy might be magnetic drums which would store say 100,000 characters with an access time of several milliseconds. Finally, the machine might have a memory composed of electrostatic storage tubes which can store 40,000 characters with a truly "random" access of say 12 microseconds. This array of different mechanisms is the result of a practical compromise between speed, capacity and cost.

---

[13] For example, see G. M. Hopper and J. W. Mauchly, "Influence of programming techniques on the design of computers," PROC. I.R.E., pp 1250–1254; this issue.

Some very exciting things are in the offing as far as new memory systems are concerned, in the form of improved memory tubes, magnetic cores used as memory devices and, even more speculative, the use of ferroelectric materials such as barium titanate.[14]

The next most serious limitation at present seems to relate to speed, but here the problem is not simply one of speed per se, but rather of speed as a function of cost. It is possible to strike a variety of compromises between these two factors as dictated by the requirements of the particular application. This is convincingly demonstrated by the existence of different types of arithmetic units. For example, a number of machines have been built on the so-called "serial" basis in which a relatively simple but fast type of adder may be used to add two words, bit by bit, usually proceeding from the least significant bit position and progressing with time toward the most significant position. Contrasted with this there are so-called "parallel" machines in which a complete array of individual adder units handle all the digit or bit positions at the same time. Finally, there are hybrid forms of machines, the so-called "serial-parallel" in which the bits comprising the binary code for each decimal digit are handled in parallel, but the digits themselves are then handled in series, and the inverse of this called "parallel-serial" operation. This problem of speed versus cost can, of course, be helped by the introduction of very much faster components. An alternate solution would be to develop components which will greatly reduce the cost, or at least devices which reduce the over-all size of the computer, its power consumption and its complexity, thus reducing its cost.

Here again, we seem to be just around the corner from significant developments. An increase in the use of diodes and the application of transistors are frequently cited as being very promising ways to reduce the size and power requirements. Printed circuit techniques offer possibilities in the way of economies in assembly, and there is a general trend toward miniaturization of almost all of the needed components. Miniaturization may also bring in its wake an automatic increase in speed, because of the lowering of stray capacitances, the decrease in lead inductances, etc. We can certainly look forward to a continual, although perhaps gradual reduction in the size and cost of data processing machines.

Of course, along with improvements of these sorts, we must always keep in mind the problem of machine reliability. As machines become more complicated and faster, error free operation becomes of dominating importance. A typical machine may perform additions, requiring the functioning of hundreds and even thousands of components, at the rate of say 16,000 additions per second. Such a machine has to be well nigh perfect if it is to operate for periods measured in hours or days without an error. The temporary malfunctioning of a single component for a period of less than one microsecond may completely invalidate the final result. As someone has put it, "Every bit counts." Unfortunately, such perfection is not easily achieved.[15] One popular way out of the difficulty is to utilize automatic checking procedures, or to carry along additional information in the form of so-called "redundancy bits" which will detect an error through a lack of internal consistency. In the extreme case, "error correcting codes" may be used which will give the correct answer in spite of the malfunctioning of some components. These schemes are not without drawbacks since the necessary equipment inevitably complicates the machine and may under certain conditions actually result in an increase in the frequency of error. There is no substitute for reliability of the basic components.

Another limitation and in many ways the most serious, since a straightforward engineering approach to its solution is not so obvious, has to do with the increasing demands which computers seem to place on the analytical processes of the men who "program" them or, more succinctly, on the ability of these people to think. Something must be done to transfer some of the load of the routine or semi-routine mental work associated with programming to the machine itself. The path is not clear but we urgently need machines or machine operating procedures which will solve problems that are stated in the more conventional forms of symbolic mathematics, or in terms of standard accounting practices, and thus eliminate the tedium of converting problems to a series of elementary arithmetic operations. A start has been made in terms of "compiling," "sub-programming," "symbolic programming," "program assembly" techniques and the like, but this is only a start.

Finally, we need to provide our computers with devices which will detect intermittent faults as they develop and which will indicate their location and thus reduce the Herculean task of finding trouble in a very complex machine. The ultimate along this line, at present only a pipedream, is a machine which is capable of maintaining itself.

---

[14] For a survey of some existing memory systems see J. P. Eckert, Jr., "A survey of digital computer memory systems," Proc. I.R.E., pp. 1393–1406; this issue.

[15] The use of "diagnostic programming" as one means of causing a computer to help locate its own faults is becoming quite common. See, for example, D. J. Wheeler and J. E. Robertson, "Diagnostic programs for the ILLIAC," Proc. I.R.E., pp. 1320–1325; this issue.

ARE COMPUTERS HERE TO STAY?

Perhaps it is time to call a halt. The writer cannot forbear a brief reference to the present-day importance of data processing machines. Regardless of what the reader may conclude regarding the long-range future of digital computers, the scientifically trained individual who is mildly interested in these devices and who does not follow up this interest is missing some of the more exciting technical experiences of the present time. In a similar vein, anyone who puts off the use of existing data processing machines because of their rapid development is simply denying himself or his organization the opportunity to profit from their present use and he is not training his personnel in thinking in terms of machine aids; in short, he is not being realistic. Present day computers are very exciting, yet they are down-to-earth, practical devices, and they operate unbelievably well.

This paper will have served its purpose if it has given the non-specialist reader a feeling that he has an understanding of the logical principles on which digital computers are constructed and that he is beginning to be acquainted with the specialized nomenclature which beclouds the issue. We have noted that the only thing really different about computers is their "physiology" since they are made of well known building blocks. A digital computer simply processes digital information. Furthermore, only two basic functions are involved, information switching and information storage, and these are easily explained in terms of such common things as an electric light switch and a piece of paper. It is true that these functions are combined into sub-assemblies such as input and output devices, a logical unit, a memory, and a control unit, but this is largely for convenience and in any case the names are nearly self-explanatory. Understanding programming is perhaps a bit more difficult, but fixed programming is already familiar in a variety of household devices, while stored programming is simply a scheme which permits the program information to be stored and operated on just as if it were any other kind of input data. An interesting aspect of this concept has to do with the way in which the subsequent course of a solution can be made to depend upon preliminary results through the use of conditional transfer instructions. Computers are really not so very difficult to understand after all, since most of the apparent complexity resides in the program rather than the machine itself. Finally, there is a great need for the development of new computer components which will increase the memory capacity, increase the speed and decrease the size and cost, although some very exciting things are in the offing. Computers are here to stay, and it is high time for us to be learning more about them.

Can Machines Think?*

M. V. WILKES†

Since the capabilities and the limitations of computers are topics of wide-spread interest, this paper by a well-known British authority on digital computers is reprinted here, with permission, from the May 1953 issue of *Discovery* (London, England). Prof. M. V. Wilkes was in charge of designing the EDSAC at Cambridge University, England, which had the distinction of being a very early stored-program type of electronic computer. Since then his group has pioneered in developing new programming techniques and in applying computers to a large variety of problems, which include experiments to find out whether a digital computer can be made to exhibit symptoms of "learning."—*The Editor*

THE SUBJECT of this article can be discussed on various levels, ranging from that of a sensational Sunday newspaper to that of a sober philosophical periodical. It arouses deep-seated emotions, and views are apt to be expressed with vigor.

Two contrary attitudes are common. In the first place there is a widespread, although mostly unconscious, desire to believe that a machine can be something more than a machine, and it is to this unconscious urge that the newspaper articles and headlines about mechanical brains appeal.

On the other hand, many people passionately deny that machines can ever think. They often hold this view so strongly that they are led to attack designers of high-speed automatic computing machines, quite unjustly, for making claims, which they do not in fact make, that their machines have human attributes. Such people are often misled by the use of technical terms based on physiological analogies; a good example is the use of the word "memory," for the part of the machine in which numbers are stored.

We must begin by deciding what a machine must be able to do in order to qualify for the description "thinking machine." An extreme view is that of Berkeley, who in his book *Giant Brains* says, after writing about cer-

---

* Decimal classification: 621.375.2. Reprinted from *Discovery* (England) vol. 14, p. 151; May, 1953.

† Director, University Mathematical Lab.; Cambridge, Eng.

tain automatic calculating machines: "A machine can handle information; it can calculate, conclude, and choose; it can perform reasonable operations with information. A machine, therefore, can think."

The use of the expression "reasonable operations" appears to beg the question, but from the examples that he gives it is clear that Berkeley means actions which depend on the power of the machine to compare two quantities and perform one set of operations if they are equal and another set of operations if they are unequal.

This, for example, would make it possible for the machine to consult a city directory which had been placed beforehand in its memory, and determine the block in which a house having a given address lay. However, other machines, such as automatic railway signaling systems, can perform this kind of "reasonable operation," and Berkeley's definition of what is meant by a thinking machine appears to be so wide as to miss the essential point of interest in the question, "Can machines think?"

An alternative approach is to say that a machine is a thinking machine if it can imitate a human being. There are plenty of existing machines which will do this in a limited field; for example, a doctor friend of mine has a device which will answer his telephone in his absence and repeat a message he has previously recorded. But again, to describe this as a thinking machine would strike most people as playing with words and no more.

IMITATING HUMAN BEINGS

It is, however, undoubtedly the power of some machines to simulate human behavior that people have in mind when they discuss this subject, and a machine which could pass itself off as a human being when given an extended test covering a wide range of different subjects might well qualify for the title "thinking machine." Among other things the machine would have to have some power of learning; for example, it should be possible for the examiner to play a game with the machine, having first explained the rules of the game.

Of course, the machine need not necessarily have the physical appearance of a human being, and in order to avoid any unfairness arising on this account the test could best be conducted with the examiner in one room and the machine in another, the connection between them being provided by a teletype circuit. The test would then take the form of a series of questions put by the examiner, with replies and counter questions automatically transmitted by the machine.

These ideas were first put forward by A. M. Turing in a penetrating article published in *Mind* (October 1950). The following example of a dialogue which might take place between the examiner and the machine is based on one given by Turing.

Examiner: Do you know the sonnet which begins, "Shall I compare thee to a summer's day?"

Machine: Yes.

Examiner: Would not "a spring day" do as well or better?

Machine: It wouldn't scan.

Examiner: How about "a winter's day"; that would scan all right.

Machine: Yes, but nobody wants to be compared to a winter's day.

Examiner: Would you say Mr. Pickwick reminded you of Christmas?

Machine: In a way.

Examiner: Yet Christmas is a winter's day, and I do not think Mr. Pickwick would mind the comparison.

Machine: I don't think you're serious. By a winter's day one means a typical winter's day, rather than a special one like Christmas.

The questions put by the examiner are supposed to be entirely unpremeditated so that there is no possibility of the answer being built into the machine on some sort of record. It is a fantastic suggestion that a machine should be able to carry on a conversation of this sort and many people will be inclined to reject it out of hand. Certainly no existing machine is in the least capable of doing anything of the kind.

I would agree with Turing, however, that the ability to pass this test or something like it is what people mean, or ought to mean, when they talk about the possibility of a machine thinking. If ever a machine is made to pass such a test it will be hailed as one of the crowning achievements of technical progress, and rightly so. Whether everyone will then agree that the machine thinks is another matter; I suspect that to many people thinking means something which can be done by a human being, or possibly by an animal, but not by a machine.

This, however, is leading us from a discussion of what machines can do to an entirely different question, namely, "Is the brain a machine?" This is a question on which science has hardly begun to touch and the answer which would be given to it by any particular person would depend on his philosophical beliefs, particularly as to the relation between mind and matter. Indeed from one point of view, to say that the brain is a machine is equivalent to denying altogether, as some philosophers do, the distinction between these two things.

In some ways it might be said that people now tend more than they formerly did to regard human beings in the same light as machines. For example, the prevalent attitude to the delinquent is to regard him as the victim of circumstances and to say that he requires treatment rather than punishment. This is just the attitude one takes to a machine. One does not get cross with it when it does something wrong, but one looks for and rectifies the fault.

AUTOMATIC DIGITAL COMPUTERS

The subject of this article is not a new one, but its discussion has been greatly stimulated by the development of high-speed automatic digital computing machines, since these machines are capable of performing operations of much greater complexity than any machines hitherto available. I shall therefore give a description of their mode of operation with special reference to those properties which seem particularly relevant to the present discussion.

The basic operations performed by a digital computer are very simple—addition, subtraction, multiplication and such like—but the machine can be set up so as to perform a long sequence, or *program* as it is called, of these operations one after the other. The complexity which so impresses the layman is in fact a feature of the program, rather than of the machine, and the machine can be changed over from one kind of work to another by changing the program.

For this reason machines of this kind are sometimes known as *universal* machines. Given a suitable program a universal machine can do anything which could be done by a specially built machine; for example, it can simulate the behavior of an analog device incorporating feed-back. It is therefore convenient to discuss the problem of mechanical thinking in terms of writing a program for a universal machine, rather than in terms of building a special machine.

It is, of course, assumed that the universal machine is provided with a suitable output organ for the work it has to do; for the purposes of discussion this can be a printer capable of printing figures and letters. A machine built specially for experiments in mechanical thinking would need to have a very large memory, or "store" as it is perhaps better called, and its basic operations might be different from those of a machine intended for mathematical work, but the relation between mathematics and logic is so close that the differences would be unimportant in general discussion.

Some of the basic operations which can be performed by a digital computer are "conditional"; that is, their nature can depend on whether a certain number (perhaps one that the machine has just computed) is positive or negative, or whether one number is greater or less than another number. The effect of a conditional operation is that a choice is made in regard to the subsequent action of the machine; if the condition is not satisfied the machine follows a course of action specified by one section of the program, whereas if it is satisfied the machine follows a different course of action specified by some other section of the program.

As an example of the use of a conditional operation, I will give a program for calculating a square root by a method of successive approximation. Suppose we want to find the square root of the number N, and suppose we have a first approximation x_0; then a closer approximation to $\sqrt{N}$ is given by $x_1 = \frac{1}{2}(x_0 + N/x_0)$. A still better approximation can be obtained by applying the formula a second time, using the old value obtained for x_1 as the new value of x_0. This process can be repeated until it is found that the latest approximation does not differ significantly from the previous one, i.e. until x_1 and x_0 differ by a quantity which is not greater than ϵ (say). The numbers N, x_0 (the first approximation) and ϵ must be placed beforehand in the store of the machine. The store of a large machine can hold many hundreds of numbers and it is usual to number, for easy reference, the "locations" in which they are held. It will be supposed that N, x_0 and ϵ are respectively placed in storage locations 100, 101 and 102.

The program then consists of the following sequence of operations:

No. of operation in sequence	Operation
1	Copy number in 101 into 103
2	Divide number in 100 by number in 101, and put result in 104
3	Add number in 101 to number in 104, and place result in 104
4	Divide number in 104 by two, and place result in 101
5	Subtract number in 103 from number in 101, and place result (neglecting sign) in 105
6	Subtract number in 105 from number in 102, and place result in 106
7	If number in 106 is negative, go back to operation 1; otherwise go straight on to operation 8
8	Print number in 101

Here the *seventh* operation is the conditional one. This short program might form part of a longer program in which the calculation of a square root was necessary.

DISCRIMINATION

Clearly, conditional operations are very important in the present context since they give the machine a power of discrimination. The possibility of programming a machine to consult a directory, as in Berkeley's example, depends on the use of conditional operations. However, when a machine performs a conditional operation it can be said to think just to the same extent, and no more, that a subway train can be said to think whenever it approaches points which have been set automatically by the passage of a previous train, and goes in one direction rather than another. The use of the word *think* in connection with conditional operations would be justifiable only if the use of a convenient technical term were thereby secured. I know of no computing machine laboratory where the word is used in this way, although the somewhat comparable words *decision* and *discrimination* are sometimes used.

Before a program such as that given above can be put into the machine it must be expressed in a form suitable for the input device with which the particular machine is equipped. Often this means that it must be punched on paper tape like a teletype message; sometimes it must be punched on cards.

In the modern high-speed machines the whole program, or a considerable section of it, is taken into the machine before any of the operations are actually carried out. Since calculations performed on a high-speed machine always involve a great deal of repetition (as does the program given above), this makes for faster operation than would be possible if the input tape or cards had to be read afresh each time a given set of operations were to be performed.

Thus it will be seen that storage is required inside the machine for the program as well as for the numbers used in the calculation. In most modern machines the same store is used for both purposes. This is made possible by the device of using a numerical code to represent the various operations to be carried out.

For example, operation no. 2 in the above program could be represented by the following number, 4,100,101,104. Here the first figure indicates that a division is to be performed—a multiplication, for example, might be represented by 3 and an addition by 1; the remaining figures stand for the numbers of the storage locations referred to. One consequence of representing the operations in a program by numbers is that the operations may be altered by adding constants to the numbers which represent them. For example, if 1 is added to the above number, it will then stand for an operation which is similar to the previous one except that the result will be put in storage location 105 instead of 104.

This technique of changing operations in a program is used on a very extensive scale when writing programs for a high-speed digital computer, and it enables the program to be greatly compressed, thus saving space in the store. It is possible for the machine to add a new section to the program by computing, according to rules provided, the numbers which stand for the operations concerned and then planting them in positions where they will form part of the program. This is done only in a small way in practical computation, but it is important from the point of view of the present article since it means that there is no theoretical reason why a program should not be written which, when once inside the machine, will modify and extend itself indefinitely.

PROGRAMMING A MACHINE TO LEARN

The action of a machine when performing a conditional operation depends, as was explained above, on the magnitude or sign of some number at that moment in the store. If the operations before the conditional operation are arranged so that the number in question depends wholly or partly on a number which has just been taken into the machine from the outside world through the input mechanism, the action of the machine may be made to depend on signals given to it. These signals can, moreover, bring about a gradual modification of the information held inside the machine so that the action of the machine upon receiving any signal depends on previous signals it has received and on the actions it has taken in response to them. It is on this principle that the so-called "learning" programs which are sometimes demonstrated on large automatic calculating machines are constructed. Some of these programs can be very impressive in operation.

A particularly elaborate one which was constructed recently by A. G. Oettinger for the EDSAC, a large machine in the Cambridge University Mathematical Laboratory, enabled the operator to teach the machine to perform a conditioned reflex action. When the machine was working under the control of this program, it was possible to apply a stimulus whose intensity could be chosen within certain limits. The machine responded by printing a symbol—either one of the figures between 0 and 7, or an X (which was interpreted as indicating that it could not make up its mind which figure to print). The operator could then give a signal (through the input mechanism of the machine) expressing approval or disapproval, and could vary the degree of intensity of his approval or disapproval within certain limits; alternatively he could express unconcern.

Suppose he decided that he would like to teach the machine to print a 3 every time it received a stimulus, even a small one. He would begin by giving the machine a sequence of medium stimuli and noting the responses. Whenever the machine printed a 3 he would express strong approval and whenever it printed some other figure he would express strong disapproval. After a time he would find that the machine would always print a 3, even if he reduced the stimulus to a low value. However, if he went on stimulating the machine lightly and expressed neither approval nor disapproval the machine would then gradually "forget," that is, it would begin to print an occasional figure that was not a 3, and after a time would be printing just as many other figures as 3's.

Various experiments could be tried and the behavior of the machine compared with the typical behavior of an animal in similar circumstances. For example, the effect could be tried of expressing disapproval occasionally during the teaching process, even though the machine had done the correct thing. It was also possible to destroy a conditioned reflex which had been formed and to replace it by another one.

The means by which this animal-like behavior on the part of the machine is secured are very simple. Eight numbers are held inside the machine, one corresponding to each of the possible figures which can be printed. These numbers will be denoted by a_0 to a_7. When the machine is stimulated it selects the largest of these eight numbers, a_r say, and adds to it the number representing the strength of the stimulus. If the result exceeds a certain minimum value the figure corresponding to a_r is printed. Otherwise the machine prints an X. a_r is then increased or decreased according as the operator expresses approval or disapproval by an amount depending on the strength of that approval or disapproval.

Finally a small random number, which may be positive or negative, is added to a_r. The number used is random only in the sense that it is obtained by a side calculation which is not linked in any way with the operations being carried out by the rest of the program. The effect of adding a random number in this way each time a figure is printed is to give a certain irregularity to the behavior of the machine. In order that the machine shall "forget" if no approval is expressed, the eight numbers a_0 to a_7 are periodically multiplied by a constant slightly less than 1, so that if no approval is expressed they have a tendency to decay to zero.

It will be seen that the effect of expressing approval when a particular figure has been printed is to increase the chance of that figure being printed on subsequent occasions, and so, if done sufficient times, to give the appearance of a conditioned reflex action having been established.

GENERALIZED LEARNING PROGRAMS

The construction of a learning program of the above type presents no difficulty to anyone who is familiar with the technique of programming. However, such a program makes it possible to teach the machine only those things which the programmer had in mind when he wrote the program. For example, the program just described would not enable the operator to teach the machine to print different figures after alternate stimuli. If the programmer had wished to do so, he could have allowed for this possibility in his program. In fact, at the expense of making the program longer and more complicated, he could include any number of extra features, but obviously he could not think of every possible experiment which anyone might wish to try on the machine.

All the programmer is doing, in fact, is to program the action of the machine as it were at one remove; when he writes the program he visualizes, if not in complete detail, at any rate in general terms, all the possible actions which the machine can take in response to legitimate actions on the part of the operator.

Such programms are not, therefore, as interesting as at first sight might appear from the point of view of this article. What is wanted is a "generalized" learning program, which would enable an operator to teach the machine anything he chose, whether the idea of his doing so had occurred to the programmer or not. I believe that such a program would not be a mere elaboration of the simple learning programs which have been constructed up to date but would need to be based on some entirely new ideas. Presumably the program would modify and extend itself as the learning process went on.

As I have pointed out, existing machines contain the means for this extension; the difficulty is to construct a program to make use of them. If such a program could be made then it would be possible to teach the machine in much the same way as a child is taught.

Whether the new ideas I have referred to will be forthcoming, it is hard to say. Certainly, for the present, progress appears to be held up. Perhaps this will give comfort to those who cannot bear the idea of machines thinking; on the other hand it may stimulate others to further effort.

BIBLIOGRAPHY

E. C. Berkeley, "Giant Brains," John Wiley & Sons, New York, N. Y.; 1949.

A. G. Oettinger, "Programming a digital computer to learn," *Phil. Mag.*, vol. 7, no. 43, pp. 1243–1263; 1952.

C. E. Shannon, "Programming a computer for playing chess," *Ibid.*, vol. 7, no. 41, pp. 256–275; 1950.

A. M. Turing, "Computing machinery and intelligence," *Mind*, vol. 59, pp. 433–460; 1950.

M. V. Wilkes, "Can machines think?" *The Spectator*, no. 6424, pp. 177–178; 1951. "Automatic calculating machines," *Jour. Roy. Soc. A.*, vol. 100, pp. 56–90; 1951.

M. V. Wilkes, D. J. Wheeler, and S. Gill, "The Preparation of Programs for an Electronic Digital Computer," Addison-Wesley Cambridge, Mass.; 1951.

Computers and Automata*

CLAUDE E. SHANNON†, FELLOW, IRE

C. E. Shannon first became known for a paper in which he applied Boolean Algebra to relay switching circuits; this laid the foundation for the present extensive application of Boolean Algebra to computer design. Dr. Shannon, who is engaged in mathematical research at Bell Telephone Laboratories, is an authority on information theory. More recently he received wide notice for his ingenious maze-solving mechanical mouse, and he is well-known as one of the leading explorers into the exciting, but uncharted world of new ideas in the computer field.

The Editors asked Dr. Shannon to write a paper describing current experiments, and speculations concerning future developments in computer logic. Here is a real challenge for those in search of a field where creative ability, imagination, and curiosity will undoubtedly lead to major advances in human knowledge.—*The Editor*

***Summary*—This paper reviews briefly some of the recent developments in the field of automata and nonnumerical computation. A number of typical machines are described, including logic machines, game-playing machines and learning machines. Some theoretical questions and developments are discussed, such as a comparison of computers and the brain, Turing's formulation of computing machines and von Neumann's models of self-reproducing machines.**

INTRODUCTION

SAMUEL BUTLER, in 1871, completed the manuscript of a most engaging social satire, *Erewhon*. Three chapters of *Erewhon*, originally appearing under the title "Darwin Among the Machines," are a witty parody of *The Origin of Species*. In the topsy-turvy logic of satirical writing, Butler sees machines as gradually evolving into higher forms. He considers the classification of machines into genera, species and vari-

---

* Decimal classification: 621.385.2. Original manuscript received by the Institute, July 17, 1953.

† Bell Telephone Laboratories, Murray Hill, N. J.

eties, their feeding habits, their rudimentary sense organs, their reproductive and evolutionary mechanisms (inefficient machines force men to design more efficient ones), tendencies toward reversion, vestigial organs, and even the problem of free will in machines.

Rereading *Erewhon* today one finds "The Book of the Machines" disturbingly prophetic. Current and projected computers and control systems are indeed assuming more and more the capacities and functions of animals and man, to a far greater degree, in fact, than was envisaged by Butler.

The bread-and-butter work of large-scale computers has been the solution of involved numerical problems. To many of us, however, the most exciting potentialities of computers lie in their ability to perform non-numerical operations—to work with logic, translate languages, design circuits, play games, co-ordinate sensory and manipulative devices and, generally, assume complicated functions associated with the human brain.

Non-numerical computation is by no means an unproven offspring of the more publicized arithmetic calculation. The shoe is rather on the other foot. A hundred years ago Charles Babbage was inspired in the design of his remarkably prescient analytical engine by a portrait woven in silk on a card controlled Jacquard loom—a device then in existence half a century. The largest and most reliable current information processing machine is still the automatic telephone system. Our factories are filled with ingenious and unsung devices performing almost incredible feats of sensing, processing and transporting materials in all shapes and forms. Railway and power systems have elaborate control and protective networks against accidents and human errors.

These, however, are all special-purpose automata. A significant new concept in non-numerical computation is the idea of a general-purpose programmed computer—a device capable of carrying out a long sequence of elementary orders analogous to those of a numerical computer. The elementary orders, however, will relate not to operations on numbers but to physical motions, operations with words, equations, incoming sensory data, or almost any physical or conceptual entities.

This paper reviews briefly some of the research in non-numerical computation and discusses certain of the problems involved. The field is currently very active and in a short paper only a few sample developments can be mentioned.

THE BRAIN AND COMPUTERS

The brain has often been compared, perhaps over-enthusiastically, with computing machines. It contains roughly 10^{10} active elements called neurons. Because of the all or none law of nervous action, neurons bear some functional resemblance to our binary computer elements, relays, vacuum tubes or transistors. The number of elements is six orders of magnitude greater than our largest computers. McCullough has picturesquely put it that a computer with as many tubes as a man has neurons would require the Empire State building to house it, Niagara Falls to power it and the Niagara river to cool it. The use of transistors in such a comparison would improve the figures considerably, power requirements coming down to the hundreds of kilowatt range (the brain dissipates some 25 watts) and size requirements (with close packing) comparable to an ordinary dwelling. It may also be argued that the increased speed of electronic components by a factor of, say, 10^3 might be partially exchangeable against equipment requirements.

Comparisons of this sort should be taken well salted—our understanding of brain functioning is still, in spite of a great deal of important and illuminating research, very primitive. Whether, for example, the neuron itself is the proper level for a functional analysis is still an open question. The random structure at the neural level in number, placement and interconnections of the neurons, suggests that only the statistics are important at this stage, and, consequently, that one might average over local structure and functioning before constructing a mathematical model.

The similarities between the brain and computers have often been pointed out. The differences are perhaps more illuminating, for they may suggest the important features missing from our best current brain models. Among the most important of these are:

1. Differences in size. Six orders of magnitude in the number of components takes us so far from our ordinary experience as to make extrapolation of function next to meaningless.
2. Differences in structural organization. The apparently random local structure of nerve networks is vastly different from the precise wiring of artificial automata, where a single wrong connection may cause malfunctioning. The brain somehow is designed so that overall functioning does not depend on the exact structure in the small.
3. Differences in reliability organization. The brain can operate reliably for decades without really serious malfunctioning (comparable to the meaningless gibberish produced by a computer in trouble conditions) even though the components are probably individually no more reliable than those used in computers.
4. Differences in logical organization. The differences here seem so great as to defy enumeration. The brain is largely self-organizing. It can adapt to an enormous variety of situations tolerably well. It has remarkable memory classification and access features, the ability to rapidly locate stored data via numerous "coordinate systems." It can set up stable servo systems involving complex relations between its sensory inputs and motor outputs, with great facility. In contrast, our digital computers look like idiot savants. For long chains of arithmetic operations a digital computer runs circles around the best humans. When we try to program computers for other activities their entire organization seems clumsy and inappropriate.

5. Differences in input-output equipment. The brain is equipped with beautifully designed input organs, particularly the ear and the eye, for sensing the state of its environment. Our best artificial counterparts, such as Shepard's Analyzing Reader for recognizing and transcribing type, and the "Audrey" speech recognition system which can recognize the speech sounds for the ten digits seem pathetic by comparison. On the output end, the brain controls hundreds of muscles and glands. The two arms and hands have some sixty independent degrees of freedom. Compare this with the manipulative ability of the digitally controlled milling machine developed at M.I.T., which can move its work in but three co-ordinates. Most of our computers, indeed, have no significant sensory or manipulative contact with the real world but operate only in an abstract environment of numbers and operations on numbers.

TURING MACHINES

The basic mathematical theory of digital computers was developed by A. M. Turing in 1936 in a classic paper "On Computable Numbers with an Application to the Entscheidungsproblem." He defined a class of computing machines, now called Turing machines, consisting basically of an infinite paper tape and a computing element. The computing element has a finite number of internal states and is capable of reading from and writing on one cell of the tape and of moving it one cell to the right or left. At a given time, the computing element will be in a certain state and reading what is written in a particular cell of the tape. The next operation will be determined by the current state and the symbol being read. This operation will consist of assuming a new state and either writing a new symbol (in place of the one currently read) or moving to the right or to the left. It is possible for machines of this type to compute numbers by setting up a suitable code for interpreting the symbols. For example, in Turing's formulation the machines print final answers in binary notation on alternate cells of the tape, using the other cells for intermediate calculations.

It can be shown that such machines form an extremely broad class of computers. All ordinary digital computers which do not contain a random or probabilistic element are equivalent to some Turing machine. Any number that can be computed on these machines, or in fact by any ordinary computing process, can be computed by a suitable Turing machine. There are, however, as Turing showed, certain problems that cannot be solved and certain numbers that cannot be computed by any Turing machine. For example, it is not possible to construct a Turing machine which, given a suitably coded description of another Turing machine, can always tell whether or not the second Turing machine will continue indefinitely to print symbols in the squares corresponding to the final answer. It may, at a certain point in the calculation, relapse into an infinite intermediate computation. The existence of mechanically unsolvable problems of this sort is of great interest to logicians.

Turing also developed the interesting concept of a universal Turing machine. This is a machine with the property that if a suitably coded description of any Turing machine is printed on its tape, and the machine started at a suitable point and in a suitable state, it will then act like the machine described, that is, compute (normally at a much slower rate) the same number that the described machine would compute. Turing showed that such universal machines can be designed. They of course are capable of computing any computable number. Most digital computers, provided they have access to an unlimited memory of some sort, are equivalent to universal Turing machines and can, in principle, imitate any other computing machine and compute any computable number.

The work of Turing has been generalized and reformulated in various ways. One interesting generalization is the notion of A computability. This relates to a class of Turing type machines which have the further feature that they can, at certain points of the calculation, ask questions of a second "oracular" device, and use the answers in further calculations. The oracular machine may for example have answers to some of the unsolvable problems of ordinary Turing machines, and consequently enable the solution of a larger class of problems.

LOGIC MACHINES

Boolean algebra can be used as a mathematical tool for studying the properties of relay and switching circuits. Conversely, it is possible to solve problems of Boolean algebra and formal logic by means of simple relay circuits. This possibility has been exploited in a number of logic machines. A typical machine of this kind, described by McCallum and Smith, can handle logical relations involving up to seven classes or truth variables. The required relations among these variables, given by the logical problem at hand, are plugged into the machine by means of a number of "connective boxes." These connective boxes are of six types and provide for the logical connectives "not," "and," "or," "or else," "if and only if," and "if-then." When the connections are complete, starting the machine causes it to hunt through the $2^7=128$ combinations of the basic variables, stopping at all combinations which satisfy the constraints. The machine also indicates the number of "true" variables in each of these states. McCallum and Smith give the following typical problem that may be solved on the machine:

It is known that salesmen always tell the truth and engineers always tell lies. G and E are salesmen. C states that D is an engineer. A declares that B affirms that C asserts that D says that E insists that F denies that G is a salesman. If A is an engineer, how many engineers are there?

A very suggestive feature in this machine is a selective feedback system for hunting for particular solutions of the logical equations without an exhaustive search through all possible combinations. This is achieved by elements which sense whether or not a particular logical relation is satisfied. If not, the truth variables involved in this relation are caused to oscillate between their two possible values. Thus, variables appearing in unsatisfied relations are continually changing, while those appearing only in satisfied relations do not change. If ever all relations are simultaneously satisfied the machine stops at that particular solution. Changing only the variables in unsatisfied relations tends, in a general way, to lead to a solution more rapidly than methodical exhaustion of all cases, but, as is usually the case when feedback is introduced, leads to the possibility of continual oscillation. McCallum and Smith point out the desirability of making the changes of the variables due to the feedback unbalance as random as possible, to enable the machine to escape from periodic paths through various states of the relays.

GAME PLAYING MACHINES

The problem of designing game-playing machines is fascinating and has received a good deal of attention. The rules of a game provide a sharply limited environment in which a machine may operate, with a clearly defined goal for its activities. The discrete nature of most games matches well the digital computing techniques available without the cumbersome analog-digital conversion necessary in translating our physical environment in the case of manipulating and sensing machines.

Game playing machines may be roughly classified into types in order of increasing sophistication:

1. Dictionary-type machines. Here the proper move of the machine is decided in advance for each possible situation that may arise in the game and listed in a "dictionary" or function table. When a particular position arises, the machine merely looks up the move in the dictionary. Because of the extravagant memory requirements, this rather uninteresting method is only feasible for exceptionally simple games, e.g., tic-tac-toe.
2. Machines using rigorously correct playing formulas. In some games, such as Nim, a complete mathematical theory is known, whereby it is possible to compute by a relatively simple formula, in any position that can be won, a suitable winning move. A mechanization of this formula provides a perfect game player for such games.
3. Machines applying general principles of approximate validity. In most games of interest to humans, no simple exact solution is known, but there are various general principles of play which hold in the majority of positions. This is true of such games as checkers, chess, bridge, poker and the like. Machines may be designed applying such general principles to the position at hand. Since the principles are not infallible, neither are the machines, as indeed, neither are humans.
4. Learning machines. Here the machine is given only the rules of the game and perhaps an elementary strategy of play, together with some method of improving this strategy through experience. Among the many methods that have been suggested for incorporation of learning we have:

   a) trial-and-error with retention of successful and elimination of unsuccessful possibilities;

   b) imitation of a more successful opponent;

   c) "teaching" by approval or disapproval, or by informing the machine of the nature of its mistakes; and finally

   d) self-analysis by the machine of its mistakes in an attempt to devise general principles.

Many examples of the first two types have been constructed and a few of the third. The fourth type, learning game-players, is reminiscent of Mark Twain's comment on the weather. Here is a real challenge for the programmer and machine designer.

Two examples of the third category, machines applying general principles, may be of interest. The first of these is a machine designed by E. F. Moore and the writer for playing a commercial board game known as Hex. This game is played on a board laid out in a regular hexagon pattern, the two players alternately placing black and white pieces in unoccupied hexagons. The entire board forms a rhombus and Black's goal is to connect the top and bottom of this rhombus with a continuous chain of black pieces. White's goal is to connect the two sides of the rhombus with a chain of white pieces. After a study of this game, it was conjectured that a reasonably good move could be made by the following process. A two-dimensional potential field is set up corresponding to the playing board, with white pieces as positive charges and black pieces as negative charges. The top and bottom of the board are negative and the two sides positive. The move to be made corresponds to a certain specified saddle point in this field.

To test this strategy, an analog device was constructed, consisting of a resistance network and gadgetry to locate the saddle points. The general principle, with some improvements suggested by experience, proved to be reasonably sound. With first move, the machine won about seventy per cent of its games against human opponents. It frequently surprised its designers by choosing odd-looking moves which, on analysis, proved sound. We normally think of computers as expert at long involved calculations and poor in generalized value judgments. Paradoxically, the positional judgment of this machine was good; its chief weakness was in end-game combinatorial play. It is also curious that the Hex-player reversed the usual computing procedure in that it solved a basically digital problem by an anlog machine.

The game of checkers has recently been programmed into a general-purpose computer, using a "general principle" approach. C. S. Strachey used a method similar to one proposed by the writer for programming chess—an investigation of the possible variations for a few moves and a minimax evaluation applied to the resulting positions. The following is a sample game played by the checker program with notes by Strachey. (The white squares are numbered consecutively, 0–31, from left to right and top to bottom. Numbers in parentheses indicate captures.)

MACHINE	STRACHEY
11—15	23—18
7—11	21—17
8—12	20—16 *a*
12—21 (16)	25—16 (21)
9—14 ! *b*	18— 9 (14)
6—20 (16, 9) *c*	27—23
2— 7 *d*	23—18
5— 8	18—14
8—13 *e*	17— 8 (13)
4—13 (8)	14— 9
1— 5 *f*	9— 6
15—19	6— 1 (K)
5— 9	1— 6 ?*g*
0— 5 ! *h*	6—15 (10)
11—25 (22, 15)	30—21 (25)
13—17	21—14 (17)
9—18 (14)	24—21
18—23	26—22
23—27	22—17
5— 8 *i*	17—14
8—13	14— 9
19—23	9— 6
23—26 *j*	31—22 (26)
27—31 (K)	6— 2 (K)
7—10	2— 7
10—15	21—16 ?*k*
3—10 (7)	16— 9 (13)
10—14	9— 6
15—19	6— 2 (K)
31—27 *m*	2— 6
27—31 *m*	6—10
31—26 *n*	10—17 (14)
19—23	29—25
26—31 *p*	

Notes:

a) An experiment on my part—the only deliberate offer I made. I thought, wrongly, that it was quite safe.
b) Not foreseen by me.
c) Better than 5–21 (9, 17).
d) A random move (zero value). Shows the lack of a constructive plan.
e) Another random move of zero value. Actually rather good.
f) Bad. Ultimately allows me to make a King. 10–14 would would have been better.
g) A bad slip on my part.
h) Taking full advantage of my slip.
i) Bad, unblocks the way to a King.
j) Sacrifice in order to get a King (not to stop me Kinging). A good move, but not possible before 19–23 had been made by chance.
k) Another bad slip on my part.
m) Purposeless. The strategy is failing badly in the end game.
n) Too late.
p) Futile. The game was stopped at this point as the outcome was obvious.

While obviously no world champion, the machine is certainly better than many humans. Strachey points out various weaknesses in the program, particularly in certain end-game positions, and suggests possible improvements.

Learning Machines

The concept of learning, like those of thinking, consciousness and other psychological terms, is difficult to define precisely in a way acceptable to the various interested parties. A rough formulation might be framed somewhat as follows. Suppose that an organism or a machine can be placed in, or connected to, a class of environments, and that there is a measure of "success" or "adaptation" to the environment. Suppose further that this measure is comparatively local in time, that is, that one can measure the success over periods of time short compared to the life of the organism. If this local measure of success tends to improve with the passage of time, for the class of environments in question, we may say that the organism or machine is learning to adapt to these environments relative to the measure of success chosen. Learning achieves a quantitative significance in terms of the broadness and complexity of the class of environments to which the machine can adapt. A chess playing machine whose frequency of wins increases during its operating life may be said by this definition to be learning chess, the class of environments being the chess players who oppose it, and the adaptation measure, the winning of games.

A number of attempts have been made to construct simple learning machines. The writer constructed a maze-solving device in which an arbitrary maze can be set up in a five-by-five array of squares, by placing partitions as desired between adjacent squares. A permanently magnetized "mouse," placed in the maze, blunders about by a trial and error procedure, striking various partitions and entering blind alleys until it eventually finds its way to the "food box." Placed in the maze a second time, it will move directly to the food box from any part of the maze that it has visited in its first exploration, without errors or false moves. Placed in other parts of the maze, it will blunder about until it reaches a previously explored part and from there go directly to the goal. Meanwhile it will have added the information about this part of the maze to its memory, and if placed at the same point again will go directly to the goal. Thus by placing it in the various unexplored parts of the maze, it eventually builds up a complete pattern of information and is able to reach the goal directly from any point.

If the maze is now changed, the mouse first tries the old path, but on striking a partition starts trying other directions and revising its memory until it eventually reaches the goal by some other path. Thus it is able to forget an old solution when the problem is changed.

The mouse is actually driven by an electromagnet moving beneath the maze. The motion of the electromagnet is controlled by a relay circuit containing about 110 relays, organized into a memory and a computing circuit, somewhat after that of a digital computer.

The maze-solver may be said to exhibit at a very primitive level the abilities to (1) solve problems by trial and error, (2) repeat the solutions without the errors, (3) add and correlate new information to a partial solution, (4) forget a solution when it is no longer applicable.

Another approach to mechanized learning is that of suitably programming a large-scale computer. A. E. Oettinger has developed two learning programs for the Edsac computer in Cambridge, England. In the first of these, the machine was divided into two parts, one part playing the role of a learning machine and the second its environment. The environment represented abstractly a number of stores in which various items might be purchased, different stores stocking different classes of items. The learning machine faced the problem of learning where various items might be purchased. Starting off with no previous knowledge and a particular item to be obtained, it would search at random among the stores until the item was located. When finally successful, it noted in its memory where the article was found. Sent again for the same article it will go directly to the shop where it previously obtained this article. A further feature of the program was the introduction of a bit of "curiosity" in the learning machine. When it succeeded in finding article number j in a particular shop it also noticed whether or not that shop carried articles $j-1$ and $j+1$ and recorded these facts in its memory.

The second learning program described by Oettinger is modeled more closely on the conditioned reflex behavior of animals. A stimulus of variable intensity can be applied to the machine in the form of an input integer. To this stimulus the machine may respond in a number of different ways indicated by an output integer. After the response, it is possible for the operator to indicate approval or disapproval by introducing a third integer at a suitable point. When the machine starts operating, its responses to stimuli are chosen at random. Indication of approval improves the chances for the response immediately preceding; indication of disapproval reduces this chance. Furthermore, as a particular response is learned by conditioning it with approval, the stimulus required for this response decreases. Finally, there is a regular decay of thresholds when no approval follows a response.

Further embellishments of programs of this sort are limited only by the capacity of the computer and the energy and ingenuity of the program designer. Unfortunely, the elementary orders available in most large-scale computers are poorly adapted to the logical requirements of learning programs, and the machines are therefore used rather inefficiently. It may take a dozen or more orders to represent a logically simple and frequently used operation occurring in a learning routine.

Another type of learning machine has been constructed by D. W. Hagelbarger. This is a machine designed to play the game of matching pennies against a human opponent. On the front panel of the machine are a start button, two lights marked + and −, and a key switch whose extreme positions are also marked + and −. To play against the machine, the player chooses + or −, and then pushes the start button. The machine will then light up one of the two lights. If the machine matches the player, that is, lights the light corresponding to the choice of the player, the machine wins; otherwise the player wins. When the play is complete, the player registers by appropriate movement of the key switch the choice he made.

The machine is so constructed as to analyze certain patterns in the players' sequence of choices, and attempt to capitalize on these patterns when it finds them. For example, some players have a tendency if they have won a round, played the same thing and won again, to then change their choice. The machine keeps count of these situations and, if such tendencies appear, plays in such a way as to win. When such patterns do not appear the machine plays at random.

It has been found the machine wins about 55–60 per cent of the rounds, while by chance or against an opponent that played strictly at random it would win only 50 per cent of the time. It appears to be quite difficult for a human being to produce a random sequence of pluses and minuses (to insure the 50 per cent wins he is entitled to by the theory of games) and even more difficult to actually beat the machine by leading it on to suspect patterns, and then reversing the patterns.

A second penny-matching machine was designed by the writer, following the same general strategy but using a different criterion to decide when to play at random and when to assume that an apparent behavior pattern is significant. After considerable discussion as to which of these two machines could beat the other, and fruitless attempts to solve mathematically the very complicated statistical problem involved when they are connected together, the problem was relegated to experiment. A third small machine was constructed to act as umpire and pass the information back and forth between the machines concerning their readiness to make a move and the choices made. The three machines were then plugged together and allowed to run for a few hours, to the accompaniment of small side-bets and loud cheering. Ironically, it turned out that the smaller, more precipitate of the two machines consistently beat the larger, more deliberate one in a ratio of about 55 to 45.

A still different type of learning machine was devised by W. Ross Ashby who christened it the Homeostat. Homeostasis, a word coined by Walter B. Cannon, relates to an animal's ability to stabilize, by feedback, such biological variables as body temperature, chemical concentrations in the blood stream, etc. Ashby's device is a kind of self-stabilizing servo system. The first model of the Homeostat contained four interconnected servos. The cross-connections of these servos passed through four stepping switches and resistors connected to the points of the steppers. Thus the effect of unbalance in the other three loops on a particular loop depended on the values of the resistors being contacted by the stepper associated with that loop. When any one of the servos was sufficiently out of balance, a corresponding limit relay would operate and cause the corresponding stepping switch to advance one point. Now normally, a servo system with four degrees of freedom and random cross- and self-gain figures will not be stable. If this occurred, one or more of the stepping switches would advance and a new set of resistors would produce a new set of gain figures. If this set again proved unstable, a further advance of the steppers would occur until a stable situation was found. The values of the resistors connected to the stepping switches were chosen by random means (using a table of randon numbers). Facilities were provided for introducing many arbitrary changes or constraints among the servos. For example, their connections could be reversed, two of them could be tied together, one of them held at a fixed value, etc. Under all these conditions, the mechanism was able to find a suitable stable position with all the servos in balance. Considering the machine's goal to be that of stabilizing the servos, and the environment to be represented by the various alterations and constraints introduced by the operator, the Homeostat may be said to adapt to its environment.

Certain features of the Homeostat are quite attractive as a basis for learning machines and brain models. It seems in certain ways to do a bit more than was explicitly designed into it. For example, it has been able to stabilize under situations not anticipated when the machine was constructed. The use of randomly chosen resistors is particularly suggestive and reminiscent of the random connections among neurons in the brain. Ashby, in fact, believes that the general principle embodied in the Homeostat, which he calls ultra-stability, may underlie the operation of the animal nervous system. One of the difficulties of a too direct application of this theory is that, as Ashby points out, the time required for finding a stable solution grows more or less exponentially with the number of degrees of freedom. With only about 20 degrees of freedom, it would require many lifetimes to stabilize one system. Attempts to overcome this difficulty lead to rather involved conceptual constructions, so involved that it is extremely difficult to decide just how effectively they would operate. Our mathematical tools do not seem sufficiently sharp to solve these problems and further experimental work would be highly desirable.

SELF-REPRODUCING MACHINES

In *Erewhon* the reproduction process in machines was pictured as a kind of symbiotic co-operation between man and machines, the machines using man as an intermediary to produce new machines when the older ones were worn out. Man's part is akin to that of the bee in the fertilization of flowers. Recently von Neumann has studied at an abstract level the problem of true self-reproduction in machines, and has formulated two different mathematical models of such "machines."

The first of these may be pictured somewhat as follows. "Machines" in the model are constructed from a small number (of the order of twenty) types of elementary components. These components have relatively simple functions, for example, girders for structural purposes, elementary logical elements similar to simplified relays or neurons for computing, sensing components for detecting the presence of other elements, joining components (analogous to a soldering iron) for fastening elements together, and so on. From these elements, various types of machines may be "constructed." In particular, it is possible to design a kind of universal construction machine, analogous to Turing's universal computing machine. The universal constructing machine can be fed a sequence of instructions, similar to the program of a digital computer, which describe in a suitable code how to construct any other machine that can be built with the elementary components. The universal constructing machine will then proceed to hunt for the needed components in its environment and build the machine described on its tape. If the instructions to the universal constructing machine are a description of the universal constructing machine itself, it will proceed to build a copy of itself, and would be a self-reproducing machine except for the fact that the copy is not yet supplied with a set of instructions. By adding to the universal machine what amounts to a tape-copying device and a relatively simple controlling device, a true self-reproducing machine is obtained. The instructions now describe the original universal machine with the addition of the tape reproducer and the controlling device. The first operation of the machine is to reproduce this entity. The controlling device then sends the instruction tape through the tape reproducer to obtain a copy, and places this copy in the second machine. Finally, it turns the second machine on, which starts reading its instructions and building a third copy, and so ad infinitum.

More recently, von Neumann has turned from this somewhat mechanical model to a more abstract self-reproducing structure—one based on a two-dimensional array of elementary "cells." Each cell is of relatively simple internal structure, having, in fact, something like thirty possible internal states, and each cell communicates directly only with its four neighbors. The state of a cell at the next (quantized) step in time depends only on the current state of the cell and the states of its four neighbors. By a suitable choice of these state transitions it is possible to set up a system yielding a kind of self-reproducing structure. A group of contiguous cells can act as an organic unit and operate on nearby quiescent cells in such a way as to organize a group of them into an identical unit.

This second model avoids many of the somewhat extraneous problems of locating, recognizing and positioning components that were inherent in the first model, and consequently leads to a simpler mathematical formulation. Furthermore, it has certain analogies with various chemical and biological problems, such as those of crystal and gene reproduction, while the first model is more closely related to the problem of large scale animal reproduction.

An interesting concept arising from both models is the notion of a critical complexity required for self-reproduction. In either case, only sufficiently complicated "machines" will be capable of self-reproduction. Von Neumann estimates the order of tens of thousands of components or cells to obtain this property. Less complicated structures can only construct simpler "machines" than themselves, while more complicated ones may be capable of a kind of evolutionary improvement leading to still more complicated organisms.

CHALLENGE TO THE READER

We hope that the foregoing sample of non-numerical computers may have stimulated the reader's appetite for research in this field. The problem of how the brain works and how machines may be designed to simulate its activity is surely one of the most important and difficult facing current science. Innumerable questions demand clarification, ranging from experimental and development work on the one hand to purely mathematical research on the other. Can we design significant machines where the connections are locally random? Can we organize machines into a hierarchy of levels, as the brain appears to be organized, with the learning of the machine gradually progressing up through the hierarchy? Can we program a digital computer so that (eventually) 99 per cent of the orders it follows are written by the computer itself, rather than the few per cent in current programs? Can a self-repairing machine be built that will locate and repair faults in its own components (including components in the maintenance part of the machine)? What does a random element add in generality to a Turing machine? Can manipulative and sensory devices functionally comparable to the hand and eye be developed and coordinated with computers? Can either of von Neumann's self-reproducing models be translated into hardware? Can more satisfactory theories of learning be formulated? Can a machine be constructed which will design other machines, given only their broad functional characteristics? What is a really good set of orders in a digital computer for general purpose non-numerical computation? How can a computer memory be organized to learn and remember by association, in a manner similar to the human brain?

We suggest these typical questions, and the entire automata field, as a challenge to the reader. Here is research territory ripe for scientific prospectors. It is not a matter of reworking old operations, but of locating the rich new veins and perhaps in some cases merely picking up the surface nuggets.

BIBLIOGRAPHY

W. R. Ashby, *Design for a Brain* (New York, Wiley, 1951).
E. C. Berkeley, *Giant Brains, or Machines That Think* (New York, Wiley, 1949).
S. Butler, *Erewhon and Erewhon Revisited* (New York, Modern Library Edition, 1927).
J. Diebold, *Automation* (New York, Van Nostrand, 1952).
A. S. Householder and H. D. Landahl, *Mathematical Biophysics of the Central Nervous System* (Bloomington, Principia Press, 1945) pp. 103–110.
S. C. Kleene, *Representation of Events in Nerve Nets and Finite Automata*, Rand Corporation Memorandum RM-704, 1951.
D. M. McCallum and J. B. Smith, "Mechanized Reasoning," *Electronic Engineering* (April, 1951).
Warren S. McCulloch, and Walter Pitts, "A Logical Calculus of the Ideas Immanent in Nervous Activity," *Bull. Math. Biophysics*, (1943) vol. 5, pp. 115–133.
W. S. McCulloch, "The Brain as a Computing Machine," *Electrical Engineering* (June, 1949).
John Meszar, "Switching Systems as Mechanical Brains *Bell Labs. Record*, (1953) vol. 31, pp. 63–69.
A. Oettinger, "Programming a Digital Computer to Learn," *Phil. Mag.*, (December, 1952) vol. 43, pp. 1243–1263.
W. Pease, "An Automatic Machine Tool," *Scientific American*, (September, 1952) vol. 187, pp. 101–115.
C. E. Shannon, *Presentation of a Maze-Solving Machine*, Transactions of the Eighth Cybernetics Conference, Josiah Macy, Jr. Foundation, New York, 1952, pp. 173–180.
C. E. Shannon, "Programming a Computer for Playing Chess," *Phil. Mag.*, (March, 1950) vol. 41, pp. 256–275.
C. S. Strachey, "Logical or Non-Mathematical Programmes," *Proc. of the Assn. for Computing Machinery*, Toronto (1952), pp. 46–49.
A. M. Turing, "Computing Machinery and Intelligence," *Mind*, (1950) vol. 59, pp. 433–460.
A. M. Turing, On Computable Numbers, with an Application to the Entscheidungsproblem, *Proc. Lond. Math. Soc.*, (1936) vol. 24, pp. 230–265.
J. Von Neuman, "The General and Logical Theory of Automata from Cerebral Mechanisms in Behavior," (New York, Wiley, 1951, pp. 1–41.
J. Von Neumann, *Probabilistics Logics*, California Institute of Technology, 1952.
N. Wiener, Cybernetics (New York, Wiley, 1948).

Electronic Computers and Telephone Switching*

W. D. LEWIS†, SENIOR MEMBER, IRE

Summary—Automatic telephone switching and digital computation have much in common. Both rely upon discrete rather than continuous devices. Development of recent switching systems with a close functional resemblance to large digital computers has increased this overlap.

The next big step in telephone switching should be towards electronics. In making this step, switching scientists and engineers can be much helped by modern electronic computer technology. To be successful, they must also contribute to this technology.

MANY TELEPHONE SWITCHING RESEARCH and development engineers are fascinated by digital computers. They talk computer language, join professional computer societies and groups, attend computer meetings. They read, and even write, articles about digital computer subjects. Digital computer engineers must wonder if their interest in these matters is solidly justified, or if they are merely succumbing to the glamor of a new technology.

The technology of electronic digital computing is undoubtedly new and glamorous, but even if it were not switching engineers would continue their interest in it. Why should they? Perhaps this question can be answered by a broad discussion of the nature of telephone switching and its relation to digital computing.

Why is there so much in common between digital computation and mechanized telephone switching? It is easy to see why the two subjects are related. Both are digital. The customers are identified by digital numbers, and it is natural that machinery which enables a subscriber to select another subscriber should be digital. But the similarity between a digital computer and a "common control" switching system extends beyond the machinery. It is functional as well.

The history of telephone switching shows persistent growth towards modern computer ideas. In the earliest days of the telephone, the digital control was provided by plug boys. In 1879, only four years after Bell invented the telephone, exchanges were installed which displayed the essential features of present manual systems. Plugs, jacks, and cords were used for connecting, and girl operators provided the digital control.

In a manual exchange the principal work of the operator is to receive, remember, translate (from number to location), and finally act upon digital information. This part of her job parallels that of a digital mechanism with input, storage, logic, and output.

The earliest commercially practical automatic exchanges in the United States were of the step-by-step variety. In them, control signals from the subscriber's dial direct a switch by moving it forward one position for each pulse. The functions of connecting, of storing, and of translating are all present, as in a manual exchange, but they are inextricably mingled. This system is still used in the majority of dial offices. However, its superficial functional resemblance to a modern digital computer is slight.

As time went on, telephone inventors and designers began to see advantages in more subtle control mechanisms, mechanisms that could store up information about the desired connection and plan to establish it in a better way, taking more facts into account. The "panel" system, for example, stores up the entire called number in a relay register, then uses two or three digits at a time to set connecting switches. A crossbar system needs at least some storage, since in a crossbar switch connections are set up at any of nm "crosspoints" by actuating one of n horizontal bars and one of m vertical bars, rather than by passing a brush over a number of contacts in sequence as in the step-by-step switch.

Even though all crossbar systems require storage, there are wide differences among them in the way storage is used and control is accomplished. European crossbar systems store some of the digits of the called number, then operate one switch, or at most two consecutive switches, at a time. In contrast, American crossbar systems use "common control" automatic switching.

In a common control switching system, central units are used to process information about all calls and to control all the switches. Here there is a particularly close resemblance to the modern large digital computer. The central control units, or "markers," are analogous to the control units in a digital computer. Information about desired calls is collected in "registers" which correspond to the "memory" of the digital computer. When information about a particular call is complete, it is transferred to the marker. The marker has access to the switching network which corresponds to the "processing or arithmetic unit of" the digital computer. The marker first tests a set of possible paths through the network. If these are busy, it then selects a new trunk and makes a second trial. When a free path is found, it closes switches in all "levels" or stages (six-switch stages in the No. 1 crossbar, and four in the No. 5). The marker can take a large number of alternative actions, depending on the status of switches, registers, other markers, and on "busy" and "trouble" conditions.

Some electromechanical switching systems have then a strong functional resemblance to digital computers. For computers using electromechanical devices, such as relays and stepping switches (e.g., Harvard's Mark I and Mark II, and the Bell relay computer), the resemblance is physical as well.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, July 13, 1953; revised manuscript received July 31, 1953.

† Bell Telephone Laboratories, Inc., Murray Hill, N. J.

The newest art of computing has, however, already surpassed the switching art in one important way. Most modern large computers rely heavily on electronics, but modern switching offices do not. There are good practical reasons for the gap. Reasons of history, economics and reliability constrain telephone engineers to a conservative approach. Any new exchange must be compatible with almost every old exchange. In other words, it must understand signals sent by the old exchanges and send signals understandable by them. In addition, the office has to work with existing wires and telephone sets in the presence of trouble and misuse. Also, newer techniques must demonstrate economic as well as technical superiority. The burden of economic proof is heavy in the face of an existing and satisfactory switching exchange even in cases where this exchange is 20 or 30 years old. Finally, exchanges must continue to operate reliably despite some equipment failures. Even the most optimistic electronic computer designers cannot yet claim 99 per cent, let alone 99.9 per cent reliability for continuous operation.

Despite these considerable difficulties, it seems probable that the next big advance in practical switching will be electronic. Electronics has high speed to offer the telephone engineer. This speed can be well used in a large exchange to handle the flood of control operations necessary to keep up with incoming telephone traffic. As many as a dozen relay markers have been used in a No. 5 office. One sufficiently reliable electronic marker could replace all of these. Of course such a simple replacement would hardly give the best design. It would be better to redesign from the ground up.

A picture of how speed could be used to advantage in a large exchange may be had by thinking first of a manual exchange which is small enough so that a single operator can handle all calls. She does this when responding to each calling subscriber's signal by plugging into his jack, listening as he gives the desired call number, then setting up the other end of the same cord to this number. She must also take down both ends of the cord when the circuit is no longer in use, handle calls to other exchanges on a special basis, provide information, record charges, and perform a variety of other duties. If the number of subscribers on this small exchange is increased, they would normally be served by adding more operators. Imagine, however, an operator who is human in every way except that she can operate at electronic speeds. She would not be able to take care of a much larger number of subscribers, not having the time to listen patiently as each call subscriber repeated the number he wished. At ten calls a second, common in a large office during a busy period, if each number required five seconds on the average to give by voice, at least fifty operators would be required even though all other functions could be compressed to zero time.

This fast electronic operator could then, obviously, do little without something else to help her. If she could have some kind of bulletin board however on which calling subscribers could write, through dialing, in their slow and ponderous human way the calls they wished to make, and if she could read this bulletin board in her fast electronic way, then sufficient speed would enable her to set up or take down each call and still have time to spare for other necessary tasks. But this bulletin board requires what computer designers mean by storage, or memory.

Therefore, the essential elements of a common control electronic exchange, besides the switching network or processing unit corresponding to the arithmetic unit of the digital computer, include a high-speed marker corresponding to the control unit and storage means corresponding to the memory in the digital computer. The input and output devices of the computer are in the exchange too. They include dials, switches, charge recording equipment, and attention and trouble signals for human beings. In both cases, there must, of course, be means for connecting the elements together.

The close resemblance, electrical and mechanical, between electronic exchanges and digital computers appears in ECASS[1] and is even more obvious in DIAD.[2] DIAD, in common with many modern computers, has a magnetic drum storage unit, rectifying diode logic circuits, and hot cathode tubes for amplifier and tempotary register circuits.

It is important to understand also the considerable differences between the arithmetic unit of the computer and its analog in the exchange—the switching network. These do different physical things, and occupy different proportions of the total equipment. The network must do much more than handle binary information. It must switch many simultaneous and independent voice channels with low attenuation, low noise, and low mutual interaction. If the full possibilities of electronics are realized, it seems likely that the equipment for performing the two functions of control and memory can be reduced to a small fraction of its present cost and size. Unless a comparable method of reducing the connecting network is found, this will then become the most formidable part of the exchange. Fortunately, ways of doing this are on the horizon.

In one of these ways gas tubes would be used as talking path switches. In the DIAD system an array of gas tubes associated with special relay switches is used for control. This array is used to select a path at electronic speeds and holds the selected path until the corresponding metallic relay path can be set up. In the proposed simplification the gas tubes themselves would be used for talking and thereby eliminate much bulky and expensive relay equipment. This would require specially

---

W. A. Malthaner and H. Earle Vaughan, "An experimental electronically controlled automatic switching system," *Bell System Tech. Jour.*, vol. 31; May, 1952.

[1] Malthaner and Vaughan, "Drum information assembler and dispatcher," Proc. I.R.E., pp. 1341–1347; this issue.

designed, noise-free gas tubes. It must be regarded as a future, rather than an immediate possibility since it calls for changes in the subscriber's telephone set.

In another proposed scheme for reducing cost and size of the talking network of a telephone exchange, far fewer switches are needed because they are shared on a time division basis. Information is transmitted between subscribers over the switches by means of amplitude modulated pulses. As is well known to engineers who have worked on time division transmission systems, a good voice channel can be provided if the pulses in a given connection are repeated at a 10 kc rate. This is possible only with electronic switches.

It is seen in the foregoing how electronics can be used to build a single control unit fast enough to handle the entire exchange on a "one-at-a-time" basis. It is also seen that electronic storage with short access time should be a feature of this electronic exchange and how electronic speeds can help with the switches themselves.

Electronic devices have advantages for switching other than speed. One advantage is size. Some of the most valuable space in the world is occupied by floor above floor of switching equipment in downtown Manhattan. Electronics may ultimately cut this space to a fraction of its present size. Another advantage lies in power consumption. Most relays absorb about a watt of power. A semi-conductor information-processing circuit containing a transistor and a few germanium diodes absorbs only a few milliwatts and can handle far more information per second.

A third advantage, potential though not yet completely achieved, is in reliability. Despite the high level of reliability and low cost which relays have achieved, they are essentially complex devices relying as they do on a combination of electrical, magnetic, and mechanical phenomena. A relay which can outlast a billion operations is an engineering marvel. A megacycle electronic counter stage performs a billion binary operations in just 16 minutes and 40 seconds. Preliminary results indicate that solid state electronic devices can be designed to last many years. The expectation of failure per operation is obviously far less with these devices than with relays, a fact which when combined with proper systems design, should substantially reduce maintenance troubles.

The foregoing indicates why so many who are concerned with telephone switching follow the electronic computer art and expect that the exchange of the future will profit much from the great progress in electronic computers. Indeed, the benefit need not be all one way. Switching research and development may contribute something to computing. Contributions seem possible in at least three areas: to devices, to reliability, and to systems employing two or more computers.

The contributions to devices should be made simply because as telephone data storage and processing problems are solved computer device problems are inevitably solved also. Digital transistor research and fundamental development read equally in the two fields. The same applies to other devices, for example, diodes, storage tubes, ferrites, and ferroelectrics.

A realization of reliability must be made before electronic telephone switching can become an operating actuality. The service must go on. Satisfactory reliability for a switching office, whether achieved through better components or through self-protecting circuit and systems design, must be much greater than is now acceptable in large digital computers used for scientific computation or accounting purposes. Such improvements may not be too significant in the mathematical computers where circuit or program checks will guard against error. On the other hand, they will be significant wherever it is desired to use a computer to control or to keep up with a real situation which must go forward regardless of the readiness of the computer.

To see the possible contribution of switching to systems employing two or more computers may require a longer look into the future. It is based upon an analogy with the way in which switching is done in a large city. A single telephone call is usually handled by two or more central offices: an originating office, a terminating office, and often one or more intermediate or "tandem" offices (It is planned to extend a fully automatic system of this sort to the United States, Canada, and part of Mexico.) Applying this to computers there emerges the possibility of joint action of two or more computers to solve problems which are too big for any one alone. It would perhaps be economically sound to get away from the ideal of the general-purpose computer and to design specialized computers which would be most efficient in one field, but which could call upon other computers for help when approached on problems outside of their best range of skills.

Since big computers are likely to be separated geographically, this would call for means for high-speed transmission and reception of digital information. And, as they are coded according to many different schemes, they would be incompatible without appropriate translating equipment. If the group of computers were to handle more than one problem at a time as the need for efficient use of the system would demand, rules and means for doing this without confusion would have to be devised. All of these functions have parallels in telephone switching, all occurring millions of times each day by present techniques. Future switching technology should suggest, if not actually provide, means for performing them in systems of electronic computers.

All of the above can be summarized simply: nature and economics seem to lead digital computing and telephone switching into parallel paths. This association should be profitable to switching, and it is hoped it may also benefit digital computing.

Fundamentals of Digital Computer Programming*

WALKER H. THOMAS†

Summary—**A simplified stored-program digital computer is described in order to demonstrate the fundamentals of computer programming. Using eight instructions, a number of basic techniques are illustrated by means of programs which perform elementary arithmetic and logical computations. The stored-program computer's capacity for modifying its own program is demonstrated.**

INTRODUCTION

A LARGE FAMILY of high-speed, large-scale, stored-program, digital computers have been built with a basic logical design pattern which allows discussion of elementary programming in general terms. Variations from the basic pattern are found in all such computers, but these variations take the form of added refinements which may make programming easier and may speed up computation by reducing the number of operations required for a given computation. Other variations arise from the nature of the input and output devices and the type of memory used.

This paper has been written for newcomers to the digital computer field and for those whose work has been limited to computer components and circuits. It is intended to give an introduction to the way in which programmers and coders use computer instructions to do useful computations. Its approach is deliberately unsophisticated to achieve generality. Wherever possible standardized terminology has been used.[1]

To discuss programming we must describe a typical, though simplified, computer to which the programs apply. A computer consisting of the basic logical elements and a relatively small number of basic instructions will be described. Although the decimal number system will be used in discussion, the same principles will hold for programming binary computers, the only difference being in the representation of the numbers.

BASIC ELEMENTS OF DIGITAL COMPUTERS

All stored-program digital computers have four basic elements: the memory or storage element, the arithmetic element, the control element, and the terminal equipment or input-output element.

The memory element consists of a number of storage locations in which information can be stored and from which this information can be extracted. Information stored in memory remains unchanged until it is replaced by new information. Obtaining information from a memory location does not change its contents. Each of the storage locations which comprise memory is identified by a number; its address. In the computer to be used as an illustration, memory will consist of 1,000 locations which will be addressed by the numbers 000 through 999. Each location will be capable of storing 5 decimal digits and sign, which may be either a number or an instruction. Since the coded form in which an instruction appears in memory is a number, there is no distinction between a number representing data for calculations and a number representing an instruction.

The arithmetic element of our computer is simply an accumulator with its appropriate information and control paths. The accumulator may be likened to a desk calculator. Addition of numbers is performed by first entering one of the numbers (the augend) in the accumulator and then giving the command to add, at the same time entering the other number (the addend). After the operation the sum will be retained in the accumulator. Subtraction is performed in the same manner except that the command to subtract is given. The accumulator has been provided with the necessary logical circuits to attach the correct sign to the difference. For multiplication the multiplier is entered in the accumulator, and the command to multiply is given while the multiplicand is entered. The product, with the correct sign, will be retained in the accumulator, replacing the multiplier. The control circuits provide the correct sequence of control pulses to the accumulator for each arithmetic operation.

The control element consists of counters and switches which take each instruction in sequence from memory and send the proper command signals to the various parts of the computer to execute the instructions. The control element consists of the instruction counter, the instruction register, and various other control circuits. Their functions will be made clear in the following description of the operation of the computer.

No input-output element will be described for this simple computer. Input-output elements differ greatly in different machines, and their basic function of bringing in information from input equipment and sending out information to output units is about all that is common to the different computers that have been built. For the computer used as an example, it will be assumed that all necessary instructions and initial data have already been put into memory and that the results, after computation, will be stored in memory.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 23, 1953.

† International Business Machines Corp. Engineering Laboratory, Poughkeepsie, N. Y.

[1] "Standards on electronic computers: definition of terms, 1950," PROC. I.R.E., vol. 39, pp. 271–277; March, 1951.

Operation of the Simple Computer

Fig. 1 is a block diagram of the simple computer showing the interconnection of the basic elements.

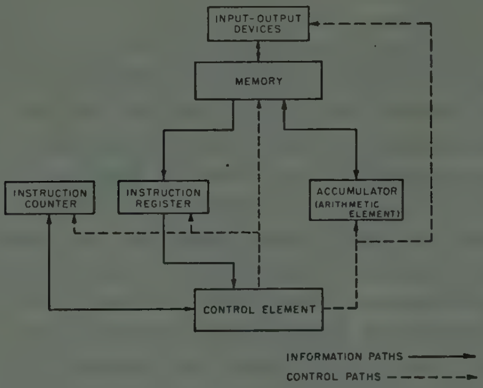


Fig. 1—Block diagram of simple stored program digital computer.

The simple machine has been provided with eight instructions. They are:

Instruction	*Operation Code*
add	01
subtract	02
multiply	03
clear and add	04
store	05
transfer	06
transfer if minus	07
stop	00

An instruction, as stored in memory ready to be executed, has five digits. The first two of these are the operation code. The last three, called the address part, usually give the address of the memory location which contains the information to be acted upon. Thus the instruction which directs the machine to add the contents of the memory location whose address is 356 would be stored in memory as 01356. The sign of an instruction is immaterial. It should be noted that this instruction in its coded form is a number. It may be acted upon by other instructions to change its meaning. The only thing which identifies an instruction to the computer is that it is brought into the instruction register under control of the instruction counter. This action is described in the following paragraphs.

Fig. 1 shows two paths from memory, exclusive of the input-output connections. The left path is used to put instructions into the instruction register where they are decoded and executed. The right path, which operates in both directions, is used to send numbers to the arithmetic element and to receive the results of computation. The execution of each instruction takes place in two cycles, an instruction cycle and an execution cycle. During the instruction cycle the left path is used, and during the execution cycle the right path is used if an arithmetic operation is to be performed.

The operation of the computer during an instruction cycle is the same for all instructions. When the computer is started, the instruction counter contains 000, and the machine automatically performs an instruction cycle. The contents of the instruction counter are acted upon by the control circuits to select the addressed memory location, in this case the location whose address is 000. The contents of this location are put into the instruction register.

During the execution cycle, which always follows an instruction cycle, switches in the control circuit provide appropriate command signals to the rest of the computer according to the contents of the left two digits, the instruction code, of the instruction. If the instruction is one which calls for a reference to memory, the control circuits select the memory location specified by the address part of the instruction and set up the appropriate information path. On arithmetic instructions, *Add*, *Subtract*, *Multiply*, and *Clear and Add*, the accumulator receives the proper sequence of command signals to perform the desired operation. After each execution cycle is completed, except in the cases of the *Transfer* and *Transfer if Minus* instructions, the instruction counter contents are increased by one. Then another instruction cycle is called for to bring the next instruction into the instruction register.

Thus the machine alternates between instruction cycles and execution cycles, bringing an instruction from memory, executing it, and obtaining the next instruction. The function of the instruction counter should be noted. It is used during the instruction cycle to determine from which memory location an instruction is to be obtained. As mentioned above, on most instructions the contents of this counter are increased by one at the end of each execution cycle. Thus instructions are normally obtained from sequential memory locations, starting with location 000 when the machine is placed in operation. The effect of the *Transfer* and *Transfer if Minus* instructions on the instruction counter will be described later.

The following description of the sequence of events that occur during the execution cycle when the *Add* instruction is executed also applies in most details to the *Subtract*, *Multiply*, and *Clear and Add* instructions. After the *Add* instruction has been brought into the instruction register during the instruction cycle, the control element provides the appropriate control signals to execute the instruction. The contents of the memory location specified by the address part of the *Add* instruction are sent to the accumulator where, on command from the control element, the incoming number is added to the original contents of the accumulator. The sum remains in the accumulator. The execution is now completed; the instruction counter contents are increased by one, and another instruction cycle is executed. After the execution of the *Subtract* or *Multiply* instructions the result is retained in the accumulator. After multiplication, the product is rounded to five digits. The *Clear and Add* instruction first clears the accumulator to 00000, then adds the number from memory, thus bringing the contents of the specified memory location into the accumulator unchanged. None of the instructions described make any change in the contents of memory.

The *Store* instruction is used to return information from the accumulator to memory. The control element, on obtaining the signal from the instruction register to execute the *Store* instruction conditions the specified memory location to accept information. The original contents of the selected memory location are lost, being replaced by the contents of the accumulator, but the accumulator still retains the information which was stored. The instruction counter is now stepped and the next instruction is obtained.

The execution of the *Transfer* instruction is simple. Upon being signaled to execute the *Transfer* instruction, the control element distributes signals which transfer the last three digits of the instruction in the instruction register to the instruction counter. The instruction counter is not increased by one during the execution of this instruction, and the next instruction is obtained from the memory location specified by the instruction counter contents. Thus, the *Transfer* instruction provides the programmer with the ability to break the sequence in which instructions are obtained from memory. For example, if the instruction counter contained 067 and memory register 067 contained the instruction *Transfer* to 115, coded as 06115, the next instruction would be obtained from memory location 115 and the program would continue in sequence from there until another *Transfer* instruction was executed.

The *Transfer if Minus* instruction tests the sign of the contents of the accumulator. If the accumulator contents are negative, the *Transfer* instruction is executed as described above. If the contents of the accumulator are positive or zero, the *Transfer* instruction is not executed. Instead the contents of the instruction counter are increased by one, and the next instruction in sequence will be executed. This conditional instruction makes it possible for the programmer to write programs which take different courses of action depending upon the results of previous computation.

The execution of the *Stop* instruction stops the computer, leaving the contents of all registers and counters unchanged. The address part of this instruction has no effect.

SIMPLE ARITHMETIC PROGRAMS

The first program to be discussed adds up three numbers, a, b, and c, and stores their sum. Let a, b, and c be stored in memory locations 005, 006, and 007. The program will add the three numbers and store the result in memory location 008.

Location	Operation	Address Part	Effect
000	*clear and add*	005	Puts a into the accumulator.
001	*add*	006	Forms $a+b$ and leaves it in the accumulator.
002	*add*	007	Forms $a+b+c$ and leaves it in the accumulator.
003	*store*	008	Stores result, $a+b+c$, in memory location 008.
004	*stop*	000	Stops the computer.
005	a		Initial Data
006	b		
007	c		
008	—		Location for storing result.

If the values +1436, −3712, and +57632 were assigned to a, b, and c, the coded program would appear in memory as follows:

Memory Location	*Contents*
000	+04005
001	+01006
002	+01007
003	+05008
004	+00000
005	+01436
006	−03712
007	+57632
008	+00000

After the instructions of the above program have been executed, memory location 008 will contain +55356. Notice how the *Stop* instruction stops the computer before any of the numbers to be added can be interpreted as if they were instructions.

The second example evaluates the expression ax^2+bx+c. The memory locations whose addresses are 007, 008, 009, and 010 contain a, b, c, and x. The result is to be stored in location 011.

Location	Operation	Address Part	Effect
000	*Clear and add*	007	Puts a into the accumulator.
001	*multiply*	010	Accumulator now contains ax.
002	*add*	008	Accumulator now contains $ax+b$.
003	*multiply*	010	Accumulator now contains $x(ax+b)=ax^2+bx$.
004	*add*	009	Accumulator now contains ax^2+bx+c.
005	*store*	011	Stores result in memory location 011.
006	*stop*	000	Stops computer.
007	a		Initial data
008	b		
009	c		
010	x		
011	—		Location for storing result.

SIMPLE LOGICAL PROGRAM

The programmer's ability to write programs which give the computer the power of making simple decisions is provided by the inclusion of conditional instructions. The *Transfer if Minus* instruction incorporated into our computer is such an instruction.

The following program is an example of the use of the *Transfer if Minus* instruction in making decisions. This program examines three numbers, a, b, and c, and determines the largest number of the set. When the machine stops, the largest number will be stored in memory location 016.

Location	Operation	Address Part	Effect
000	*clear and add*	013	Forms $a-b$ in the accumulator.
001	*subtract*	014	
002	*transfer if minus*	005	If $a<b$, transfers to 005.
003	*clear and add*	013	If $a \geqq b$, puts a into the accumulator and executes 006 next.
004	*transfer*	006	
005	*clear and add*	014	If $a<b$, puts b into accumulator.
006	*store*	016	Stores the larger, a or b, in memory location 016.
007	*subtract*	015	Subtracts c from larger, a or b.
008	*transfer if minus*	010	If $c>a$ and b, transfers to 010.
009	*stop*	000	Computer stops here if a or b is the largest with that number stored in memory location 016.
010	*clear and add*	015	If $c>a$ and b, stores c in memory location 016, replacing a or b.
011	*store*	016	
012	*stop*	000	Computer stops here if c is the largest of the set.
013	a		Initial data
014	b		
015	c		
016	—		Storage for largest number.

It will be noted that not all the instructions are executed for any one case. Depending upon which number is the largest, some of the instructions will be skipped. The reader may want to assume values for a, b, and c and follow through the program on paper. The validity of a program may always be tested on paper by going through it step by step. The programmer should pretend to be as "dumb" as the computer and try to forget the purpose of each step. By following each instruction to the letter he may uncover errors in the logic of the program.

CYCLICAL PROGRAM

Much of the versatility of digital computers lies in their ability to have instructions operate on other instructions in a program as if they were numbers. To show this ability, the above program will be expanded into a program to find the largest of a set of 500 numbers.

If enough memory registers were available, this could be done by adding more comparison instructions to the above program. Such a program would be doing the same kind of operations over and over. A short cyclical program can be written which will execute the required comparison instructions, change the address parts of those instructions, and then execute the modified instructions again. A test is required during each execution to determine if all numbers have been compared. At the end of the execution of the program the largest number will be stored in memory location 014.

Fig. 2 is a flow chart of the following program. Such flow charts show graphically the operation of a program. When complex programs are to be written, a flow chart will assist the programmer in his work.

Location	Operation	Address Part	Effect
000	*clear and add*	017	Stores first number in memory location 014.
001	*store*	014	
002	*clear and add*	(018)	Subtracts the contents of location 014 from the number currently being tested.
003	*subtract*	014	
004	*transfer if minus*	007	If number in memory register 014 is larger, transfers to 007.
005	*clear and add*	(018)	If current number is larger, stores it in location 014.
006	*store*	014	
007	*clear and add*	002	Puts the instruction from location 002 into the accumulator.
008	*add*	015	Adds one to the instruction.
009	*store*	002	Stores the modified instruction in locations 002 and 005.
010	*store*	005	
011	*subtract*	016	If last number has not been compared, transfers back to 002 and checks next number.
012	*transfer if minus*	002	
013	*stop*	000	Stops computer after last comparison.
014	———		Storage for largest number.
015	+00001		Constant for increasing instructions.
016	+04517		Constant for testing if last number has been compared. It has the same form as the instruction *clear and add* 517.
017			Initial data (500 numbers to be compared.)
·			
·			
·			
·			
·			
516			

NOTE: The parentheses around the address parts of instructions in memory locations 002 and 005 indicate that the address parts will be changed as the program progresses. When the program is put into memory, their address parts will be 018.

CONCLUSIONS

This paper has illustrated such features of digital computer programming as the sequence in which instructions are executed, how this sequence may be broken, and the provisions for modifying instructions by arithmetic processes. The example above shows the use of these features to write a short, powerful program.

The programs used as examples show, of necessity, only the most basic of the programmer's techniques. One programming problem of the first magnitude not mentioned above is scale factoring, the problem of keeping the magnitudes of data, intermediate results, and final results within the range of the computer's registers. Computers usually have a number of shifting instruc-

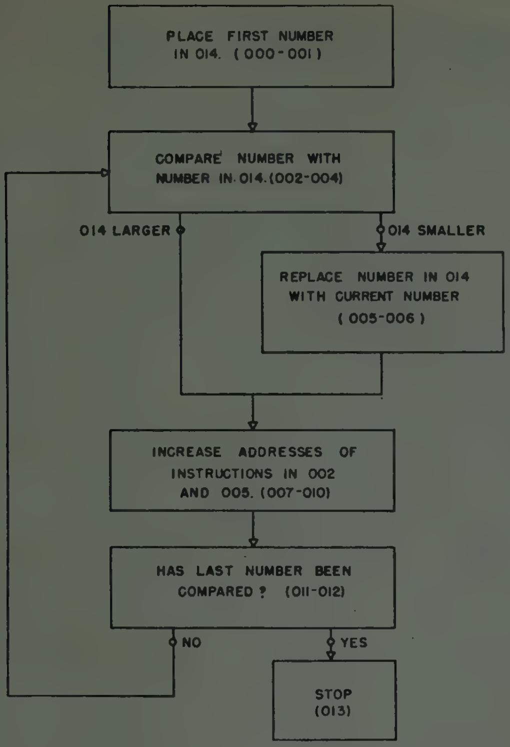

PLACE FIRST NUMBER IN 014. (000-001)
COMPARE NUMBER WITH NUMBER IN 014. (002-004)
014 LARGER
014 SMALLER
REPLACE NUMBER IN 014 WITH CURRENT NUMBER (005-006)
INCREASE ADDRESSES OF INSTRUCTIONS IN 002 AND 005. (007-010)
HAS LAST NUMBER BEEN COMPARED ? (011-012)
NO
YES
STOP (013)

Fig. 2—Flow chart for simple cyclical program.

tions which multiply or divide the numbers by powers of the radix employed. Another common type of instruction is an instruction which modifies only the address part of a stored instruction. Most, but not all, machines include a divide instruction. A number of instructions are always provided to permit programmed control of the input-output devices.

In this paper, a computer was described which uses a single-address system of instructions. Each instruction in such a machine specifies the location of only one operand. Computers with double-, triple-, and quadruple-address instructions have been and are being built. These multiple-address instructions allow certain economies of time and programming effort, but, in most cases, add to machine complexity. An example of the *Add* instruction for each type of machine follows.

No. of Addresses	Instruction Form	Method of Operation
1	*Add* a	Add the contents of a to the contents of the accumulator and retain the sum in the accumulator.
2	*Add* a, b	Add the number in a to the number in b and retain the sum in the accumulator.
3	*Add* a, b, c	Add number in a to number in b and store result in c.
4	*Add* a, b, c, d	Add number in a to number in b, store the sum in c, and take the next instruction from d.

For the person interested in advanced programming, the publications listed in the bibliography will take him into the realm of abstract coding, assembly programs, relocation subroutines, interpretative subroutines, and a host of other programming techniques designed to save time and effort.

BIBLIOGRAPHY

AIEE-IRE, "Review of Electronic Digital Computers," 1950.

Association for Computing Machinery, "Proceedings of the Association for Computing Machinery, May 2 and 3, 1952," Richard Rimbach Assoc., Pittsburgh; 1952.

———, "Proceedings of the Association for Computing Machinery, Toronto, Sept. 8–10–52."

Berkeley, E., "Giant Brains," John Wiley and Sons, Inc.; 1950.

Engineering Research Assoc., "High Speed Computing Devices," McGraw-Hill Book Co., New York, N. Y.; 1950.

Gill, S., "The Diagnosis of mistakes in programmes on the EDSAC," *Proc. Roy. Soc. (A)*, vol. 206, p. 538; 1951.

Hartree, D. R., "Calculating Instruments and Machines," University of Illinois Press, Urbana, Ill.; 1949.

Koons, F., and Lubkin, S., "Conversion of numbers from decimal to binary form in the EDVAC," *MTAC*, vol. 3, No. 26, p. 427; April, 1949.

Los Angeles IRE Professional Group on Electronic Computers, "Proceedings of the Electronic Computer Symposium"; April 30, May 1–2, 1952.

Perry, D. P., "Minimum access programming," *MTAC*, vol. 6, No. 39, p. 172; July, 1952.

Van der Poel, "A simple electronic digital computer," *Appl. Sci. Res. Sec. B*, vol. 2, p. 367; 1952.

Wilkes, M. V., "Programme design for a high speed automatic calculating machine (EDSAC)," *Jour. Sci. Inst.*, vol. 26, p. 217; June, 1949.

Wilkes, M. V., Wheeler, D. J., and Gill, Stanley, "The Preparation of Programs for an Electronic Digital Computer," Addison-Wesley Press, Cambridge; 1951.

* * *

Influence of Programming Techniques on the Design of Computers*

GRACE M. HOPPER†, AND JOHN W. MAUCHLY†, ASSOCIATE, IRE

Summary—**Along with advances in hardware design, the programmer is making advances in programming techniques. These new techniques take advantage of the high-speed checked operation of the computer to perform the routine work of programming. It is quite conceivable that these techniques will exert a strong influence on computer design in the future.**

A GROUP OF ENGINEERS who have just completed the design of an electronic computing system are at no loss for ideas for improving their new creation. The engineer feels that a computer has become obsolete as soon as its design has been frozen. The attitude of the programmer is quite different. His design problems are just beginning. The programming specialist will discover new ways of adapting the computer to particular applications, and the techniques evolved in response to the challenge of each new task may bring about improvements comparable to those which the engineer achieves by changing circuitry and hardware. In fact, the programmer is a kind of engineer who uses mathematical equations, system diagrams, flow charts, procedure manuals and instruction codes as the tools of his trade. It is his job to bridge the gap between the problem stated in terms of accounting procedures or mathematical equations, and the specific coded instructions which control the computer system.

The design of the general-purpose computer must always be a compromise involving many different requirements which are to some extent conflicting. To keep initial cost and maintenance down, a simple design is preferable. On the other hand, if considerable enhancement of the speed or other performance factors can be secured through modest additions in hardware or complexity, there is economic justification for moving in such a direction. One of the factors which has always seemed to deserve heavy weight in shaping such decisions has been the ease or difficulty with which the human programmer can adapt himself to the instruction code peculiar to his own computer. A design which has emphasized simplicity of equipment may turn out to be anything but simple for the programmer, yet a computer which has supposedly been made handy and versatile by the inclusion of a large variety of special instructions may likewise be difficult to program. That various groups have reached different conclusions regarding what constitutes a desirable repertoire of instructions is obvious from the range displayed in existing computers.

Although the fact is often overlooked, an extremely simple general-purpose computer can duplicate exactly every operation of the most complicated computer imaginable. The choice between two computers is therefore, one involving the economy of operation, rather than the possibility or impossibility of such operation. For many users, one of the important economic factors is the cost associated with the programming staff needed to secure effective use of the electronic equipment. Special instructions designed for the greater convenience of the programmer, are likely to increase initial cost. A larger investment in the physical equipment leads to greater concern over inefficient use of this equipment through delays or errors in programming. It is clear that for computer installations which operate for extremely long periods of time on just a few major problems, programming convenience is not important. A general-purpose computer, however, must be designed on the assumption that new problems or variations of old ones will be rather common, and the ease with which programs may be created or modified is therefore an important factor to be reckoned with.

What should the computer designer incorporate in his equipment in order to facilitate the task of the programmer? Certainly the programmer must help the engineer in evaluating proposed engineering plans, and he can often suggest possibilities for the engineer to consider. Sometimes a relatively minor design modification can result in savings in programming. More often, a proposed new instruction for the computer is useful only in certain special applications and is at the same time difficult to achieve from the engineering point of view.

This relation between the programmer and the designer of computers is by no means a static one. While the engineer is developing new components and better ways of using such components, the programmer is likewise developing new techniques for the application of computers and is continually enlarging the range of applications as well. Hence, it must not be expected that, as the art of programming advances, there will be a gradual but certain convergence upon some optimum instruction code defining the ideal computer toward which engineering designers should strive. The development of new techniques in programming may have as profound an influence on computer design as would be produced by an entirely new type of memory or switching element.

In the field of programming for automatic computers, there are current developments which must inevitably affect the design of future computers. Electronic computers are now being used to create their own sequence of instructions. The computer is being made to take over from the human programmer most of the time-consuming and burdensome routine work which hereto-

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute July 2, 1953.

† Remington Rand, Inc. Eckert-Mauchly Div., Philadelphia, Pa.

fore has been done by human programmers. The fact that any general-purpose automatic computer could be made to do this has been known for a long time, but, as in many engineering developments, there has been a lapse of time between the first glimpse of the theoretical possibility and the reduction to actual practice.

The need for automatic programming has been growing for several reasons. The present shortage of trained programmers is not likely to be relieved in a short time, since new computers are going into use at an ever-increasing rate. Computers are being applied to larger and more complex tasks and this tends to increase the cost of the programming effort. There is also the inescapable fact that human beings do make errors, and that complex programs usually contain some errors, even after they have been subjected to several independent checks. It is reasonable to expect, and it has been found in practice, that an automatic computer is much less likely to make mistakes than a human doing the same work. Ridding a new program of errors turns out to be a costly job when done by human labor, and may be almost as costly when computer time is used for this purpose.

In addition to the economic arguments just cited, we also must recognize that experienced programmers are always anxious to make the computer carry out as much routine work as they can. Anyone with even a modest amount of experience in programming and coding comes to realize that there is a considerable amount of repetitive and routine operation in these jobs as they are usually done by the human programmer. In the early days of programming for automatic computers, creating a specific program for a specific application was fascinating enough. The construction of programs which would in turn generate other programs was a generality to be left to the future. However, the fancy of yesterday may be commonplace tomorrow.

Methods whereby the computer itself can be made to do most of the work associated with programming have been developed in various ways and to various degrees at a number of computing centers, both in the United States and elsewhere. The differences in approach by these separate groups is partly a result of differences both in central and auxiliary equipment and in other characteristics such as the instruction code peculiar to a particular system. In view of this, there is some satisfaction in noting that, just as there are some characteristics which are similar in all automatic computers, there are also elements common to all of these diverse efforts toward automatic programming. One such universal element is the subroutine.

A subroutine is a clearly defined, easily symbolized, often repeated program; for example, the computation of cosine x, floating-decimal arithmetic $(+, -, \times, \div)$, social security deduction, interest at x per cent from (day, month, year) to (day, month, year). Early in the history of computers, the most frequently used subroutines were built-in as a part of the hardware of the computer.

The Automatic Sequence Controlled Calculator, Harvard's Mark I, contained subroutines for sine x, $\log_{10}x$, 10^x, and interpolate for x, each called for by a single operation code. These subroutines existed as functional units consisting of relays and counters which used the multiply-divide unit and the transfer bus. Not long after Mark I started running in the spring of 1944, disadvantages were discovered in this subroutine method. Once a subroutine had been called into action, no other operation could be performed because the main bus was tied up. Then subroutines could not be abridged; they always computed to full computer precision. They could not make use of approximations which sometimes are available in the computation. Each used largely its own separate hardware. Left idle, they developed bugs when increasingly infrequent calls were made on them.

With the design of the Aiken Relay Calculator, Mark II, many of these disadvantages were eliminated. The necessary constants were built-into the computer and made rapidly available by code. Certain special readouts were added such as "times two," "times five," "select approximation." The operation could be programmed to any desired precision. The subroutines were decidedly faster, more accessible, and more flexible. However, they were limited in number: cos x, arc tan x, $1/x$, $1/\sqrt{x}$, $\log_{10}x$, 10^x, and interpolate for x. More serious, they had to be, at least in part, programmed. Even when the standard subroutine, programmed for full computer precision, was to be used, it had to be copied with appropriate changes made in the memory locations.

A "coding machine" was provided for Mark III. Now the subroutine was stored in the relays of the coding machine which automatically inserted the proper memory location. Still the subroutines available were limited to those built into the hardware of the coding machine.

Meanwhile, in England, the EDSAC group under the leadership of Drs. Wilkes, Wheeler and others, while waiting for the computer to be checked out, laid plans for a library of subroutines. Defining certain standard methods of locating arguments and results, and standard procedures for transferring control to and from the subroutines, they developed the first easily used and referenced library. Fortunately, they also wrote a book discussing their methods.

Simultaneously, groups in this country had been collecting files of subroutines. In particular, the group at the Eckert-Mauchly Computer Corporation drawing upon Binac and UNIVAC experience, had piled up by 1949 a most respectable body of subroutines. It could not yet be called a library because it was not standardized and referenced. However, in two fields, well-integrated volumes for the library were ready when the first UNIVAC was delivered. These were the programs for data processing; i.e., sorting, collating, and merging prepared by Mrs. John H. Holberton and the programs for matrix algebra outlined by Dr. Herbert F. Mitchell, Jr.

Soon, many subroutines were available. Unfortunately, they were not standardized; memory locations were assigned at will by the programmers. Arbitrary rather than relative coding was employed. Errors made in copying the subroutines into a new program required debugging time. This led to a policy of standardization of memory locations and relative coding was instituted.

During the same period, a "short code" was developed for UNIVAC to speed the programming of mathematical problems. This was the first pseudo code for UNIVAC. The original conception of an "interpretation" routine for UNIVAC was suggested by Dr. John W. Mauchly, who proposed that the UNIVAC should be programmed to accept, as nearly as possible, the mathematical symbols as written by the mathematicians, including the significant parentheses and juxtaposed characters for multiplication. Flow charts were prepared to show how this could be done, but the the detailed coding was never completed. The "short code" as it now exists for the UNIVAC, was developed as an offshoot of this original plan. For this program, subroutines for the elementary algebraic and transcendental functions are stored in preassigned portions of the internal memory. Problems are submitted to the computer expressed in pseudo code. An "interpretive" routine then decodes the input information and calls the subroutines into play as required. This later "short code" system has proved its value for certain types of problems, although it is only a first approximation to the complete plan as originally conceived. The present short code can use only the set of subroutines which are stored in the computer, and cannot readily be made to include new subroutines. Also, the translation of a problem into the pseudo code is a human task; the errors which may creep into the operation are sometimes not easy to detect. However, it has served to illustrate and point up a principle. The mathematician could be supplied with a far more abundant set of readily available operations without increasing the computer's hardware and cost. Programming and debugging time could be materially reduced.

Building on all that had gone before, but attempting to establish a general plan, the Programming Development Group of the UNIVAC Applications Department started work in the fall of 1951. The first "compiling" routine was successfully tested in the spring of 1952. The work of this group up to May 1953 will be described later, but the above dates deserve comment because the design of so-called interpretive, compiling, generating, executive, master and slave, and operating routines is closely akin to the design of a computer. Such a project cannot be carried out in a few weeks. It requires far more accurate checking and debugging than routine programming. Techniques which seem obvious when completed, require many false starts and run into many dead-ends before they are perfected.

Three types of routines—compilers, generators, and operators, and three techniques—subprogramming, pseudo coding, and coded coding, required definition. These terms have acquired quite specific meanings within the group.

A pseudo code is a symbolism other than the instruction code of the computer for presenting the information defining a problem to the computers. For example, the 37th operation of a problem, $x_{13}+x_{28}-x_{46}$ (floating decimal) is submitted to compiler $A-0$ as four UNIVAC words.

```
aa0   000   f00   00i
1rg   013   037   000
2rg   028   000   000
1rs   000   000   046
```

In a more advanced pseudo code the operation $u+v=w$ is presented to the differentiator as

```
A00   00u   00v   00w.
```

It will be noted that these pseudo codes are highly redundant. Obviously, they can be reduced to fewer bits. However, with a readily available secondary memory which is virtually unlimited, there is no need to eliminate the redundancies. The two pseudo codes here presented are easily and speedily operated upon by the computer, again exemplifying the programming principle that speed can be bought by sacrificing space and vice versa.

Compilers prepare programs. They accept information in pseudo code, decode it, search for the appropriate subroutine, adjust the subroutine addresses to the position of the subroutine in the programs, select and insert the memory locations of the arguments and results, arrange control transfers, and write the finished program on tape. One example of the application of a compiler and the speed at which such programs may be expected to operate is cited here.

It is desired to tabulate the function

$$\Phi = -A \sum_{(\alpha\beta\gamma)} \frac{\alpha e^{-\alpha t}}{(\alpha-\beta)(\gamma-\alpha)}$$

between $t=0$ and $t=T$, at intervals Δt; where α, β, and γ are zeros of

$$p^3 + ap^2 + bp + c = 0;$$

and $A=f(a, b, c)$. Values of Φ are required for 1875 combinations of the parameters; 10 per cent precision is desired; it is desired that precision be maintained as the roots tend to confluence.

The preliminary survey indicated that the complex number computation must be carried out in floating-decimal to attain the desired precision. After the problem had been analyzed and stated in pseudo code, the UNIVAC, under the instruction of Compiler A-1 and calling on the floating-decimal library, produced the necessary program in six and one-half minutes.

No time was needed to debug the program. Because the elimination of debugging time far more than covered the compiling time, less computer time was required by the automatic coding method than by the hand-tailored methods. The over-all elapsed time, from statement of the problem to printed results, was drastically reduced.

The example cited above has been computer tested. However, it is by no means the "last word." Compiler

A-0 which proved the technique feasible is now an antique. A-1, as currently used, is a prototype, not completely general relative to input and output, and limited to a straight line of program segments. Still not a production model, A-2 has been computer tested. It will turn out far more complex programs than A-1, and its programs may extend to over 100,000 instructions. Here again, the particular computer employed has influenced the design of the compilers. With practically infinite secondary memory readily available through buffer storage, little attempt need be made to conserve memory space. Indeed, in many cases, the use of the computer to construct extremely long programs has led to *significant reductions in computation time.*

The term "subprogramming" has been applied to the technique of requiring the computer to "unwind" iterative control loops and produce straight line programs for often repeated problems. If successive sweeps are to be made over a large mesh, conventional programming dictates that the operations be subroutined for a single mesh point. In the absence of *B*-lines or similar built-in devices, the memory locations are altered so that the subroutine treats the next point, and it is repeatedly altered and used again. In extreme cases, the time required to alter memory locations may exceed the time required for computation. A second method, that of transferring successive points to standard memory locations and repeating the subroutine, is also time consuming. It is more efficient to instruct the computer to write out a "straight-line" program for the entire mesh, and use this long program for each main sweep. Of course such a program could be hand-written and typed, but since it may consist of 150,000 single address instructions, the error frequency in manual transcription prohibits such a procedure. In high-cost, high-speed computers, hardware devices and special instructions will no doubt eliminate the necessity for the subprogramming technique. However, in low-priced computers with fewer instructions, less hardware and less speed, the technique will remain valuable. In a specific case, computer-tested by both the conventional and subprogramming methods, the time required to sweep a particular mesh was reduced from 63 seconds by conventional programming to 43 seconds using the subprogramming technique.

A *generator* is a special type of compiler designed for data processing. If only a limited number of operations are to be performed upon each item of a large amount of data, the required program may be generated rather than pieced together from subroutines. The subroutines are reduced to "*coded coding.*" For example, in order to prepare new computer data for printing, it must be "edited." Titles, headings, and page numbers must be supplied. Zeros must be suppressed preceding integral values; decimal points and plus and minus signs must be inserted. An editing generator has been computer-tested to program these operations for any specific set of data. After the printed page has been designed, specifications are written, and a "background" prepared. The specifications, following a few general statements such as the item size, take for the form, 06 z0 08 13 01 06, indicating that digits 3 through 8 of the sixth word of the input item (raw data) are to be transferred to digit positions 1 through 6 of the thirteenth word of the output item, with zero suppression. The background contains all titles, headings, decimal points, tabs, carriage returns, line feeds, etc., with zeros in the positions to be occupied by the data.

The generator contains, within itself, skeleton subroutines in "coded coding" such as "BFE OO RUEC OOO" from which is developed relative coding, which is in turn, adjusted and subprogrammed. Thus the generator, on the basis of the specifications, selects and expands the coded coding, producing a limited subprogrammed program containing within itself all the controls required to handle and process the data. In one case, the generated program contained approximately one-fourth the number of instructions required by the corresponding hand-tailored program and required a little more than half the time to process the data. Less than three minutes of computer time were required to generate the instructions and they were error free.

One might question whether the usefulness of the editing generator will disappear as more elaborate printers become available. Plugboards and switches can replace editing runs. However, an editing routine may generate a full reel of data processed in less than ten minutes. It is doubtful whether one could set up and check a plugboard in so short a time. Hence, the data to be edited in any given form must extend over many reels of tape before the plugboard set up is justified. The generator will always be useful in the low-cost computers where the elimination of hardware is a primary consideration.

The production of error-free programs depends upon the fact that the operation of the UNIVAC is checked. Thus, if the compiling, and generating routines and the libraries of subroutines have been thoroughly computer-tested and proved, the resulting programs will be error-free. Since it is almost impossible to devise mathematical, programmed checks on either compiled or generated coding, these techniques provide a strong argument for checked operation.

The checking feature becomes of even greater importance when the *operators* are considered. One such routine, a differentiator, has been programmed for the UNIVAC. Its mathematical derivation and its applications form the substance of a thesis presented by Harry Kahrimanian to Temple University. If the analytical *formula* for a function is presented in pseudo code (second type cited), the differentiator will derive the *formulas* for the nth derivative (total or partial); the first n derivatives; the mth through nth derivatives ($m, n < 99$). The results are presented in the pseudo code, ready for submission to a compiler. If the formulas for the derivatives are desired rather than numerical values, a routine now in process will translate the pseudo code into edited formulas suitable for printing. The time ratio between the manual derivation of the formulas and the computer derivation may easily reach a million to one. Here for the first time, the computer replaces the human being performing routine mental labor, a task in which not even a desk computer has yet been able to provide assistance. Naturally, the time ratio is high. The differentiator first operated successfully in April 1953. At present, insufficient time has been available to explore its applications, but together with its "algebra routine" which includes collection and cancellation of terms, it offers pleasant possibilities for the elimination of routine mathematics.

Not one of the programs described above, except perhaps the editing generator, is a production model. They are not yet ready for a service bureau, or for mathematicians and engineers who cannot call upon a trained programmer. It is hoped that production models will soon be devised and operated.

The existence of such routines, computer-tested and proved, with known operating times, points up the new problems facing a designer of computers.

Consider the low-cost, low-speed computer. Reduction of the quantity and cost of hardware is a primary consideration. A low-cost computer probably means a low-cost installation which cannot afford a large programming staff. Such a computer, if designed with a very large, comparatively slow, internal storage (magnetic drum) to contain a compiler or interpreter and a library of subroutines, would require very little input and output and an extremely small instruction code. Compilers and subroutines could be programmed once and for all by expert programmers. Depending upon the compiler and library read onto the drum at the start of the problem, the computer could operate as a complex-number floating-point machine for the electronics engineer, or as an alpha numeric accounting machine. All problems would be entered in suitable pseudo codes, adaptable, flexible and suited to the particular user.

At the other end of the scale, expensive, very fast computers with both large internal and secondary storage could be designed with extremely elaborate instruction codes designed for speed and not convenience. Only the expert programmers who create the executive routines would be required to manipulate this cumbersome code. Again, use would be made of a pseudo code.

That such types of computers are possible is evident. That their pseudo code can be simple is not quite so evident, but becomes so when it is realized that the best pseudo code for mathematical problems is the symbolism of mathematics with the addition of some "plain English" such as "differentiate" where a derivative is desired. It may be anticipated that simple English will be the best pseudo code for commercial problems.

The routines here described have been confined to mathematical and engineering applications. Other groups in the UNIVAC Applications Department have been and are considering the use of subroutines in commercial applications. The extrapolations into the design of future computers are the personal ones of the authors, and are not to be construed as "official" or as reflecting the views of the UNIVAC Applications Department or of Remington Rand, Inc.

Acknowledgment

The authors wish to express their thanks and appreciation to the staff of programmers who have contributed in many different ways to the work reported in this paper.

Analogue vs. Digital Computers—A Comparison*

MORRIS RUBINOFF†, ASSOCIATE, IRE

***Summary*—Analogue and digital computing machines are both capable of solving numerous types of mathematical problems. Nevertheless, these two kinds of machines mechanize the solutions in fundamentally different ways. The problem of simulation in real time is used as a basis for comparing the characteristics of the two kinds of machines as regards basic units, size, speed, precision, accuracy, stability, input-output, flexibility and future possibilities. The mathematical operations discussed include addition, subtraction, multiplication, division, evaluation of polynomials and other functions, square root extraction, and the solution of ordinary differential equations.**

Introduction

ANALOGUE COMPUTING INSTRUMENTS and machines have been used for many years in devices requiring simulation in real time. With the advent of large-scale digital computing machines, the question naturally arises that, since digital computers have been built which are megacycle fast and capable of more accurate solutions than analogue machines, why cannot digital machines be used in real-time simulators. This paper undertakes to review the basic processes of both machines, to compare and contrast their capabilities and to reach a tentative qualitative answer to the question just posed. It should be kept in mind that the basis for comparison is specialized to the case where the computers are to be used to solve real-time problems. Conclusions reached on this basis are not applicable to all non-real-time solutions.

Real-time simulation is most frequently effected as the solution of a set of ordinary nonlinear equations with time as the independent variable. For the purposes of the comparison it is assumed that the algebraic processes to be encountered are as follows:

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, May 18, 1953.

† University of Pennsylvania, Philadelphia 4, Pa.

1. Addition and subtraction.
2. Multiplication and division.
3. Evaluation of polynomials.
4. Square root extraction.
5. Computation of functions, namely, sine and cosine, arc sine and arc tangent, exponential.
6. Solution of a set of ordinary nonlinear differential equations.

Whereas a sharp delineation in order of increasing complexity would be difficult to make, it is clear that the operations (1) and (2) are fundamental and rudimentary while the process (6) is a complex composite routine.

The algebraic notion of operation-complexity is almost immediately applicable to digital computation. On the other hand, it does not apply at all when the computations are mechanized by analogue techniques. Because of the many variations of analogue devices, the discussion below will be limited to one specific type. A similar limitation will later be placed on the description of digital computers. It is believed, however, that basic considerations will be essentially unaffected by this specialization.

ANALYSIS OF MECHANIZATION REQUIREMENTS

The first decision which must be made when designing a calculating machine is the choice of a device to represent the parameters which occur. These parameters will in general consist of constants, both additive and multiplicative, and of variables, such as a, b, and x, respectively, in the expression $(a+bx)$.

Next it is necessary to invent a compatible mechanism for performing the (algebraically) basic operations, addition, subtraction, multiplication and division, listed as (1) and (2) above.

Finally, it is necessary to devise apparatus for performing the remaining operations. The latter must be divided into two groups which, at least machine-wise, are quite different. The first group consists of the processes (3), (4), and (5), or, more generally, the evalution of functions, which we shall find is a relatively straightforward matter. The second group consists of the solution of equations, of which process (6) is an example and which makes considerably more serious demands on computers, both human and machine.

The mechanisms used to perform these operations will now be described in some detail.

MECHANIZATION OF PARAMETERS

In analogue computers of the type considered, parameters are represented as voltages. Technical considerations necessitate restricting the voltage range between upper and lower limits, usually an equal voltage above and below ground, e.g. +50 v. and −50 v. In order to attain maximum precision for variable parameters, it is usual to "normalize" all variables; that is, the full range of the variable is represented by the full 100 volt range available. Normalization can always be performed by altering multiplicative constants; e.g., if $-100 \leqq x \leqq 100$ and if $y=0.1x$ be required, then one can write $y=0.1x\times(2/2)=(0.1\times2)\times(x/2)=0.2\ X$ and $-50 \leqq X \leqq 50$.

The representation of variables is effected by means of potentiometers. For example, the variable x is shown in Fig. 1 to be represented by the voltage delivered to the adjustable arm of the potentiometer P.

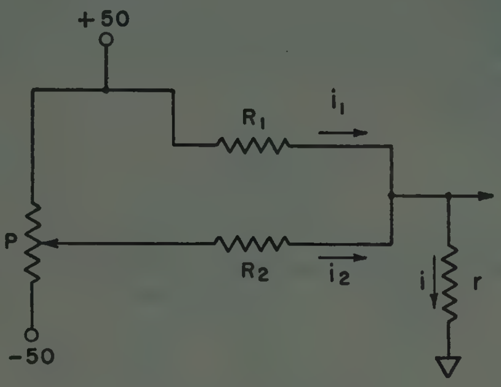


Fig. 1—Analogue adder.

Because the arithmetic processes are performed by current summation in resistors (theoretically of negligible resistance), constants are represented by resistors with large fixed resistance values. For example, in Fig. 1, R_1 represents an additive constant by determining the component $i_1=50/R_1$ of the current i flowing through the (small) summing resistor r. At the same time R_2 is a multiplicative constant which determines the current i_2 generated by the variable voltage x from the potentiometer, so that $i_2=(1/R_2)x$. Briefly, then, the current $i=i_1+i_2=(50/R_1)+(1/R_2)x$ represents the function $y=(a+bx)$ where $a=50/R_1$ and $b=1/R_2$.

Several significant remarks are now in order. Note first that the variable x, as represented, is a continuous variable; any value of x within the range is theoretically possible. On the other hand, the value of x can never be specified exactly but only as lying within a narrow range of voltage because it is physically impossible to generate infinitely precise voltages or to manufacture infinitely precise potentiometers. Although precisions up to one part in 10^6 can be obtained in the laboratory by exercising extreme care, the precision of analogue simulators is limited in general to one part in 10^3 or at most 10^4.

Secondly, it should be noted that the mechanization process is one involving an appreciable amount of labor, including the precise measurement of resistors and their connection physically into an electric circuit. Each parameter must be incorporated separately; moreover, if the variable x be required at more than one point in the simulator, it is generally necessary to provide separate resistors to represent the associated multiplicative constant at each point. Briefly, then, an analogue system is inherently a simultaneous or "parallel" system, one in which a separate unit is provided for every parameter.

As a direct consequence of their parallel construction, analogue simulators lack flexibility. Once a system is assembled to perform a given task, it is restricted to the performance of that task. To alter it to perform an appreciably different task would be an undertaking of considerable magnitude.

In digital computers, parameters are represented by an ordered sequence of digits. In most cases it is understood that each digit is to be multiplied by a number or "weight" according to the position of the digit in the sequence. Thus the parameter A, which happens to be represented by the sequence $a_n a_{n-1} a_{n-2} \cdots a_1 a_o$, has the magnitude

$$A = \sum_{j=0}^{n} a_j w_j$$

where the weights, w_j, are implied from previous information. In most cases, the weights are given as powers of a "radix" r as in the expression:

$$w_j = r^{j-c} \qquad j = 0, 1, 2, \cdots, n$$
$$c = \text{(given) integer.}$$

In the decimal system the radix r is 10, each digit a_j is restricted to the set 0 through 9, and the constant c locates the decimal point. Thus, for the decimal number $A_{10} = 63.859$, $n = 4$, $r = 10$, $c = 3$, and

$$A_{10} = 6 \times 10 + 3 \times 10^0 + 8 \times 10^{-1} + 5 \times 10^{-2} + 9 \times 10^{-3}.$$

In most digital computers of recent design, parameters are represented in the binary notation, with radix $r = 2$. This notation is particularly simple since the digits a_j are restricted to only two possible values "0" and "1." Thus, the number $A_2 = 1101.100$ has the (decimal) significance:

$$A_2 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2 + 1 + 1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} = 13.5.$$

It is generally believed that the simplicity of the binary system lends itself to digital mechanization, since such mechanization most frequently utilizes devices which have two stable states, e.g. high vs. low voltage, open vs. closed relay contacts, conducting vs. nonconducting tubes, pulse vs. no pulse. The discussion which follows will be restricted to binary machines since they are most amenable to clarity of exposition, but remarks apply to all digital systems with only minor modification.

It has just been pointed out that binary digits are mechanized by means of bi-stable devices. When used in an arithmetic unit the latter are commonly referred to as binary cells. In one class of digital computers, a single parameter is represented by a set of $(n+1)$ binary cells called a register. The magnitude of the parameter is given by the states of the binary cells, the digit value a_j being determined by the state of the corresponding cell. The binary point [the value of c] is "built into the machine." Since an arithmetic unit which utilizes $(n+1)$-celled registers usually provides transmission of the digital information over $(n+1)$ separate lines, it is referred to as a parallel unit.

Clearly, since the number of binary digits is independent of the location of the binary point, the precision is determined only by $(n+1)$, and is, in fact, exactly one part in 2^{n+1}. Thus, any desired precision can be obtained by supplying a sufficient number of binary cells. On the other hand, every digital computer requires at least three registers in its arithmetic unit, and the associated equipment rises roughly in proportion to $(n+1)$. Consequently, the size and cost of a parallel arithmetic unit rises appreciably with increase of precision. However, where only low precision is demanded the size and cost may prove to be smaller than in the serial unit now to be described.

In a serial arithmetic unit only one binary cell is provided for each parameter. The parameter digits are presented to the binary cell one at a time and in temporal sequence, with the lowest-order digit a_0 leading and with the highest-order digit a_n last to leave. The weight w_j is here determined by a clock which "counts" the digits as they pass and simultaneously directs the computer to establish a 1-1 correspondence between digit j and "machine time j." The rate of flow of digits must be synchronized with (and is usually synchronized by) the master clock; this rate is referred to as the pulse repetition frequency (PRF) of the computer. Thus, the computer requires a time interval $t = (n+1) \times \text{PRF}$ to scan each parameter as it flows through the binary cell. Clearly, a serial machine effects a saving in equipment (at least where high precision is required) at the expense of speed of computation.

Regardless of the organization of the arithmetic unit, it would be folly both financially and technically to attempt to incorporate enough registers in the machine to store simultaneously all the parameters required by any one simulator. Consequently every modern computer includes an internal storage unit or memory and operates by selecting a parameter from its memory only when the parameter is required, and by returning the results of the operations of its arithmetic unit to the memory as soon as their immediate usefulness has expired.

A computer memory unit may also be classified as a parallel or a serial device. A parallel memory unit is one from which all digits of the requested parameter are transmitted simultaneously over separate lines to the specified register in the arithmetic unit and, similarly, in the reverse direction. A complete parameter transmission is thus accomplished in the time required to transmit only one digit.

A serial memory unit is one from which the parameter digits are removed in time sequence at PRF over one line. It does not follow, however, that the time, t_a, for access to a parameter is equal to the time $t_t = (n+1) \times \text{PRF}$ required for transmission of the $(n+1)$ digits of that parameter. This is because serial memory units are generally "circulatory" in character, storing parameter digits in the form of a time sequence of pulses. Two examples of such memory units are (1) acoustic delay lines and (2) rotating (magnetic) drums carrying many "lines" of information. Technical considerations decree that the lines be long enough to accommodate many parameters (say m in number, $m \gg 1$). Consequently, in order to read a parameter into or out of the memory it is necessary to indicate in advance which of the m locations within the line is in demand. A time interval t_s is required to activate the number-selection equipment and a second time interval t_w is wasted in waiting for the desired m location to arrive at the end of the line. The access time is given by the equation:

$$t_a = t_t + t_s + t_w.$$

It is presumably possible to eliminate the waiting interval t_w in a simulator because of the predetermined and fixed character of its instruction routine; consequently, t_w will be assumed negligible. Also, most machines provide a (usually negligible) "dead" interval for number-selection purposes, so that in general $t_s \ll t_t$. Note, however, that in the absence of this dead interval, access to the memory must await a full additional transfer interval on account of the manner in which the lines are synchronized with the arithmetic unit. It follows that, with the above assumptions,

$$t_a \approx t_t = (n + 1) \times (PRF) \quad \text{[dead interval provided]},$$

$$t_a \geqq 2t_t \quad \text{[no dead interval provided]}.$$

From the preceding remarks several characteristics of digital parameter representation are evident. Note first that, in contrast with analogue representation, every parameter is represented as a discrete magnitude; if the parameter is a time-dependent variable it must be represented as a discrete set of numbers whose time co-ordinates are known to the computer.

On the other hand, parameters are here represented not by sizes of physical components but by instantaneous states of the latter. Any parameter may be erased from the memory unit at will or may be replaced by the insertion of a different parameter in its number-location. Consequently, the computer is completely flexible; the performance of diverse routines associated with completely unrelated mathematical equations calls for preliminary pencil and paper work together with the translation of equation-information into machine language through equipment external to the computer itself. Once several problems have been prepared in this manner, it is a trivial task to switch from the computation of any one problem to the computation of any other one; the machine need not be altered physically in any way.

The range of the parameters need not be restricted as severely in the case of digital computers as with analogue computers, because of the theoretically-unlimited precision available. However, for technical reasons many digital machines require each variable x to be normalized, generally so that $|x| < 1$.

MECHANIZATION OF BASIC OPERATIONS AND FUNCTION EVALUATION

It was pointed out that parameters are represented in analogue computers by resistors and potentiometers. At the same time, the connections for simulating addition of and multiplication by a constant were shown in Fig. 1. In this paragraph it is intended to indicate the mechanization of the basic arithmetic operations +, −, ×, ÷, of sudden discontinuity or "transfer," and, (briefly) of function evaluation.

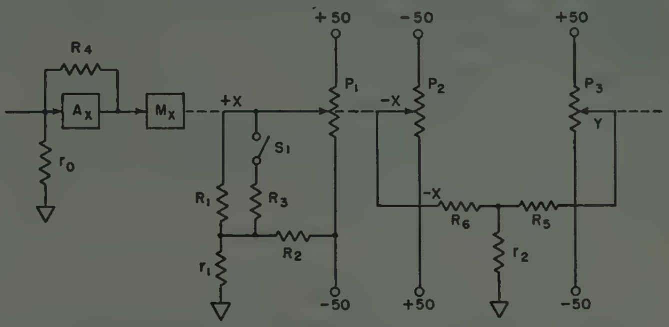


Fig. 2—Analogue function evaluator.

Referring to Fig. 2 the small resistor r_o is the summing resistor for the variable x. Since the voltage across r_o is too small to be used directly, an amplifier A_x is provided. The output of the amplifier feeds the motor M_x which drives the arms of two linear potentiometers P_1 and P_2. Because of the manner of connection, the arm of P_1 carries a voltage representing $+x$ while the arm of P_2 generates $-x$. Clearly, then, r_1 is the summing resistor for $ax-b$, where a and b are determined by R_1 and R_2, respectively. Similarly, the summing resistor r_2 computes $cy-dx$, where c and d are determined by R_5 and R_6, respectively, and y is obtained from the motor-driven arm of P_3.

It often happens that a function z is represented most conveniently by two or more straight lines, e.g.:

$$z_- = ax - b \qquad -50 \leqq x < 0$$

$$z_+ = Ax - b \qquad 0 \leqq x \leqq +50.$$

$$A \neq a$$

Discontinuities of this kind are easily incorporated by the inclusion of a switch operated by a cam on the shaft of a motor; e.g., S_1 in Fig. 2 is held closed by a cam on motor M_x's shaft when $x > 0$, and R_1 and R_3 in parallel represent the new slope A of the line z_+. All discontinuities can be handled by this technique.

Multiplication is also easily performed, as indicated in Fig. 3. Here the voltage x is applied across potentiometer P, the arm of which is positioned by the y-generating motor M_y: clearly the arm carries a voltage proportional to (xy).

Monotonically varying functions may be computed as simply as linear functions by using nonlinear potentiometers. For example, sin α can be mechanized over the interval $-(\pi/2) \leqq \alpha \leqq (\pi/2)$ by means of a potentiometer whose resistance P varies with arm rotation $\theta(\pi \leqq \theta \leqq \pi)$ according to the relation $P = \sin \theta/2$ and whose arm is driven by a motor M_α representing α. Similarly, any part of $\sin \alpha$ within that range can be mechanized through an appropriately-designed nonlinear potentiometer, as can also any monotonic piece of the cosine, the arc sine and tangent, the exponential, and even a given polynomial and the square root. In other words, any monotonic function of a single variable x can, if desired, be mechanized extremely simply merely by replacing the linear potentiometer driven by M_x with the appropriate nonlinear one.

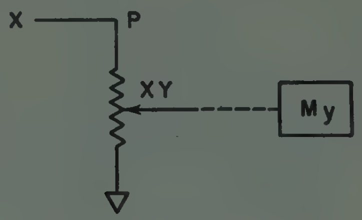


Fig. 3—Analogue multiplier.

Where the function being evaluated is dependent on two variables, or where a function of one variable is not monotonic, the function must be generated by extended connections of adders and multipliers. Clearly, as functions become more complex (i.e. consist of a larger number of basic operations), the bulk and the cost of equipment rises, roughly in proportion to the number of units required. At the same time, the computing system becomes increasingly looser. This looseness is directly attributable to (1) the compliance of motor shafts and the backlash in potentiometer arms, (2) the inertia of motors and their associated mechanical systems, and (3) the delay in voltage transmission through amplifiers (electrical compliance). The first two of these are clearly sources of lag; the amplifier delay will be discussed below.

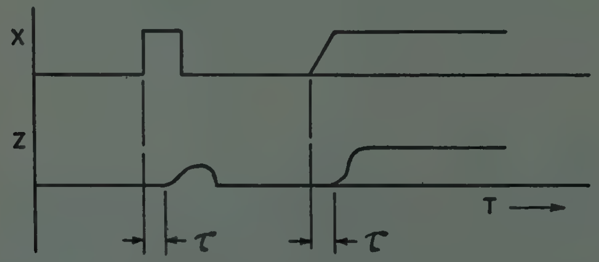


Fig. 4—Illustrating effect of compliance.

As a consequence of this looseness in the connections between units the function represented is computed inaccurately. For suppose that z is a function of several variables of which one variable x is machinewise related to z through many connections producing a delay τ. Then, if x should rise and return to its original value in a time less than τ, its influence on z will be felt only after the termination of its excursion, and the eventual z-excursion will differ radically from the one decreed by the functional relationship (see Fig. 4). Clearly, if the looseness in the system be decreased, τ decreases and the accuracy of functional computation improves. Conversely, accuracy can be improved by restricting the rate at which variables are permitted to vary and/or the frequencies at which the variables may oscillate. From the machine point of view this can only mean slowing down the computer. It follows that, for analogue computers, accuracy is limited by the intrinsic maximum permissible speed of computation.

In the discussion of Fig. 2 above, no attention was paid to resistor R_4, which is seen to connect the output of A_z to its own input. This is a feedback resistor introduced to decrease another source of inaccuracy by comparing the amplifier with its own input. When the adder was described above, it was assumed that the resistors r were small in comparison to the resistors R. Engineering difficulties prevent the direct realization of this assumption, but the use of feedback reduces the effective resistance of r to a satisfactory value. Feedback also serves to decrease intrinsic nonlinearity of amplifier, an additional source of inaccurate computation.

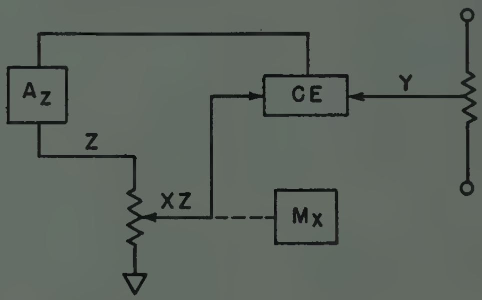


Fig. 5—Analogue divider.

The mechanization of division has now to be described. Advantage is taken of the fact that division is the inverse operation to multiplication so that if $z = y/x$, then $y = xz$. Thus, the heart of the analogue divider is a multiplier (Fig. 5) whose potentiometer arm is driven by x and whose input, z^*, should be but differs from the initially unknown z. The output of the multiplier, xz^*, is delivered to a comparison element CE whose other input is fed by the known instantaneous value of y. The output of CE, which is proportional to the error term, $y - xz^*$, is fed to amplifier A_z whose purpose it is to supply a voltage z to the multiplier to be fed back to CE. The system is arranged to seek the condition where the voltages at the two inputs to CE agree, i.e., where $y = xz$, as desired. Note that the divider unit is a feedback unit which incorporates another arithmetic unit, viz. the multiplier. This is the first instance of a principle which will be discussed at greater length below, namely, that the solution to an equation ($z = y/x$) must always incorporate one feedback loop around the arithmetic units. The combination of comparison unit and feedback system is called a servomechanism.

The square root can be mechanized by noting that $z = \sqrt{y}$ implies $y = z^2$. Thus in Fig. 5 if M_x is driven by z so that $x = z$, the output of the multiplier unit is z^2 and the feedback unit drives z^2 to agree with y as required.

One more unit remains to be discussed. Analogue computers are able to generate the derivative of a variable in a simple unit. For this purpose a motor-driven tachometer-generator is used, whose operation is based on the electromagnetic law that the voltage e generated in a wire moving with velocity v through a magnetic field is:

$$e = kv,$$

where k is a constant. The derivative unit is so designed that the motor M_x drives the tachometer simultaneously with x and in such a way that v is always proportional to dx/dt and thus that $e=dx/dt$. The mechanization of the derivative is easily extended to include integration by noting that if $y=\int^t x(\tau)d\tau$, then $x(t)=dy/dt$. By forming dy/dt and comparing with x through a servomechanism, y is obtained.

The physical unit required for analogue addition or multiplication or differentiation is a reasonably small package. In practice several such units may be incorporated into a space of about one-half cubic foot.

In contrast with the compactness of analogue units, an arithmetic unit for a digital computer requires an appreciable quantity of equipment and a correspondingly large space. In order to perform addition, a parallel digital machine calls for at least two $(n+1)$ single-digit adders requiring about four tubes per digit, and a small control unit to direct the addition process. The necessity for providing this wealth of equipment is imposed by the desire to perform the addition in one pulse time over $(n+1)$ parallel lines.

A serial machine requires three registers for addition, but it will be recalled that each register consists of only one binary cell in association with a compact memory unit having a capacity of only one number. Nevertheless in the case of low precision $(n+1\approx 10$, i.e., about $0.1\%)$, serial registers employ approximately as much equipment as do parallel ones. Moreover, the control unit is somewhat larger because it is called upon not only to direct the gross operation of addition but also to keep count of the flow of digits and to start and stop the process. Consequently, there is little choice between parallel and serial computers as regards quantity of equipment.

It would appear that addition in serial computers should take considerably longer than in parallel computers, but this is not necessarily true. In a parallel computer the addition of digits in corresponding columns of addend and augend requires only one pulse time, but a much longer interval is needed to allow for the propagation of the full carry from the lowest to the highest column.[1] On the other hand, in a serial computer the addition could proceed as the addend and augend emerge from the memory unit, so that execution of the addition does not increase computation time. Simultaneous memory read-out and addition is provided in some computers and is recommended when feasible. Other computers wait until both numbers are extracted before proceeding to add, and in this case an extra computation interval of $(n+1)$ pulse times is required. In general, $(n+1)$ pulse times is longer than the addition time for an equivalent parallel unit.

Both parallel and serial computers employ three registers for multiplication and for division, and both accomplish these arithmetic processes through a sequence of repeated additions or subtractions, respectively. Neither is able to claim any advantage as regards additional requisite equipment. However, the parallel computer is faster since $(n+1)$ additions in it require less time than $(n+1)$ additions in a serial machine.

Regardless of whether their internal organization is serial or parallel, virtually all digital computers employ at most one or two arithmetic units on account of the appreciable equipment involved, and these units can perform only $+$, $-$, $\times$, $\div$, and transfer. As a result the evaluation of the basic operations defining a function has to proceed sequentially rather than simultaneously as in analogue machines; in any case the nature of digital computation precludes simultaneous evaluation. For example, the function:

$$z = ax + bxy$$

is programmed as the following time-sequential routine:

$$z_1 = b \times x$$

$$z_2 = z_1 \times y = bx \times y$$

$$z_3 = a \times x$$

$$z = z_2 + z_3 = ax + bxy, \text{ as required.}$$

Discontinuities may be similarly programmed through the transfer instruction which permits the machine to make its own choice between two alternative routines.

Since the numbers in the memory unit are invariant (until erased) there is nothing in a digital machine to correspond exactly to compliance in an analogue machine. The evaluation of a function $f(t)$ at time t_1 yields $f(t_1)$ accurately so long as the data available are accurate. However, the digital machine is unable to calculate $f(t)$ continuously for all t; the calculation is limited to discrete values, t_k, spaced from each other at some (usually uniform) interval Δt. So long as Δt is small, the completely unknown values between the computed $f(t_k)$ may be assumed to be approximated closely by simple formulas derived for the purpose. On the other hand, if $f(t)$ is complex and requires a large interval Δt for its evaluation, the accuracy of these approximation formulas decreases. It follows that in real time simulation, the implicit accuracy of a digital computer is limited by the speed at which it can compute. Thus the interval Δt is responsible for objectionable effects in digital computation corresponding to those effects in analogue simulation for which the delay τ is accountable.

---

[1] For example, this occurs when 0000,0001 is added to 0111,1111 to yield 1000,0000 in an 8-digit computer $(n=7)$.

Feedback for analogue division and square-root has its digital counterpart, called iteration. Iterative division of y by x consists of (1) guessing at an approximate reciprocal z_1 for x, (2) repeatedly improving the guess by the recursion formula $z_{i+1}=z_i(2-xz_i)$, $i=1, 2, 3, \cdots$, until the result z_r equals $1/x$ to the requisite accuracy, and (3) multiplying z_r by y to obtain $z=yz_r=y/x$. Iterative square root differs only in the recursion formula used.

It was implied above that function evaluation must be performed as a sequence of basic operations. However, it is possible to incorporate function tables into a digital computer to yield some functions such as sine, cosine, exponential, polynomials, without the need for extended computation. Such function tables are excessively expensive to build if all computation is to be avoided; the saving effected by limited tables is questionable, particularly where low precision is acceptable.

The simplicity of analogue differentiation and integration unfortunately cannot be matched by digital mechanisms.

Mechanization of Solution of Equations

It is important to note at the outset that there are two possible interpretations of the sign of equality in expressions such as:

$$w = f(x) = x^5 - x \sin x. \tag{1}$$

On the one hand, this expression may be an identity which states that the dependent variable w is equal by definition to the function $f(x)$ of the independent variable x. In this case, x may take on any value x_k within its range of existence; the expression then prescribes the procedure for evaluating the corresponding w_k. On the other hand, w may be a constant. In this case the expression is an equation; moreover, it imposes a restrictive condition on x, limiting it to a set of discrete values whose magnitudes cannot be found through straightforward evaluation of a function.

It might be argued that on occasion the solution of an equation can be reduced to function evaluation, as in the following cases:

$$x^2 + 2ax + b = 0 \text{ implies } x = -a + \sqrt{a^2 - b}$$

$$\frac{d^2y}{dx^2} + k^2y = 0 \text{ implies } y = A \sin (kx + b).$$

In these cases the solution would be obtained in a computer by direct evaluation as described above. Unfortunately, these cases are the exception and in general other techniques must be employed.

In an analogue computer the solution of an equation is obtained by means of the comparison element (see Fig. 5). A schematic diagram for mechanizing (1) (with $w=0$) is shown in Fig. 6. The connections are observed to be of two distinct types: (1) the lower set of interconnections of many units, which serves to evaluate the function $x^5-x \sin x$, and (2) the comparison element CE, which directs x to cary until the function becomes zero. Clearly, this network is a servomechanism whose feedback loop embraces an appreciable number of analogue units. Consequently, there is a considerable delay around the loop. Assume that when the function is negative the CE is connected so as to increase x and vice versa, i.e., the function is assumed to increase with x in the neighborhood of the solution x_k as shown in Fig. 7(a). Then, if at time t_0 the indicated analogue value of x is less than x_k, the CE willl make x increase; however, because of the delay of transmission, τ, through the evaluating network, the CE will learn of the arrival of x at x_k only after x has exceeded x_k. Finally the CE will recognize its error, proceed to decrease x, with resultant "overshoot" on the low side. This sequence of trials during which CE hunts for the correct value x_k is depicted in Fig. 7(b).

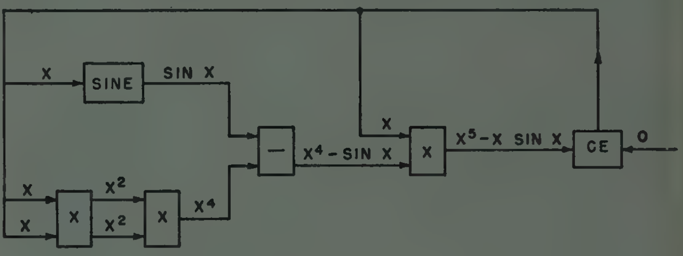


Fig. 6—Analogue equation solver.

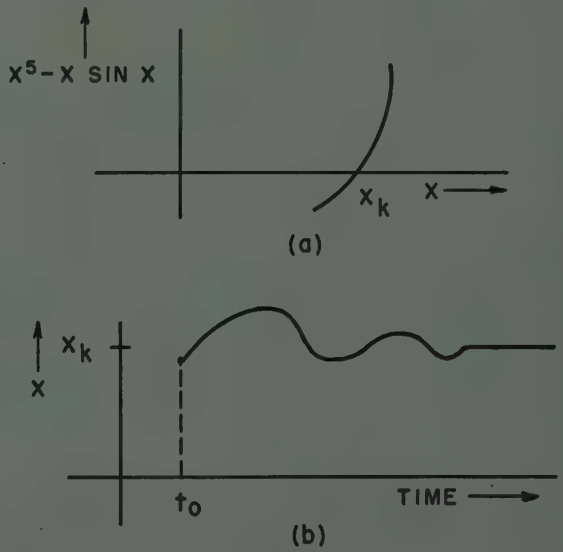


Fig. 7—An example of hunting.

Until now it was assumed that w was a constant and that x had ample time at its disposal to seek its solution. However, w could conceivably be a variable itself (and generally is), and the time available for x-hunting would then be determined by the rate at which w varies. Moreover, if w were to vary sinusoidally at a frequency comparable to the hunting frequency, the overshoot error in x would increase cumulatively. These cumulative overshoots cause the system to break into spontaneous oscillation or to behave in a manner which does not bear any immediate relationship to the solutions sought. Clearly, the system will be even more susceptible to this unruly behavior when the equation becomes complex (e.g., if $f(x)$ were a more complex function) and/or when many equations must be solved simultaneously.

To summarize, the solution of equations requires interconnections between units which involve feedback paths. This feedback may cause system instability even though all individual units are stable. The tendency toward instability increases with increasing complexity of the equations to be solved and with the number of feedback loops. It should be noted that the latter increase rapidly with the number of equations (roughly as the square).

Just as it was possible to improve the accuracy of function evaluation by slowing down the rate of analogue machine computation, so it is possible to restore stability when solving equations by increasing the solution time. On the other hand, the rate of computation in a real-time simulator is forced upon the analogue system by the characteristics of the device being simulated. It follows that there is an upper limit to the complexity which can be incorporated into an analogue simulator required to compute in real time.

In a digital computer the solution to (1) might be obtained by iterating using the recurrence relationship:

$$x_{n+1} = x_n - \frac{x_n^5 - x_n \sin x_n}{5x_n^4 - x_n \cos x_n - \sin x_n}, \quad n = 1, 2, 3, \cdots$$

where x_{n+1} is a closer approximation to the correct value x_k than the previous guess x_n. Clearly, each improvement on the preceding approximation involves considerable computation and hence an appreciable time interval. It follows that increased accuracy is obtained only at the expense of speed of computation. When w varies as x is being computed, the digital computer must clearly choose between (1) carrying the iteration procedure to its completion and falling behind in its computation, and (2) halting the iteration at low accuracy in order to keep up.

Finally, the iteration process is liable to develop oscillatory behavior similar to that developed by analogue servomechanisms. This is particularly true where real time considerations necessitate a large interval in the solution of a complex differential equation or of a set of simultaneous differential equations.

CONCLUSIONS

The preceding remarks may be summarized by the following enumeration of the relative merits of analogue vs. digital computers.

(a) *Basic Units.* The basic unit of a digital computer is restricted to a narrow set of operations, namely, addition, subtraction, multiplication, division and transfer, whereas the analogue computer utilizes basic units capable of performing not only these operations but also evaluation of monotonic functions, differentiation, and integration.

(b) *Size.* The size of the digital unit is many times greater than the size of any one analogue unit. On the other hand, the analogue machine is compelled by its mode of computation to include a separate unit for each and every basic operation; consequently each simulator must be judged separately before a statement of relative size of digital vs. analogue can be made. Where the computer is to simulate several similar devices, the digital machine may afford a saving through the use of a memory unit common to all. However, this possible saving requires further study.

(c) *Speed.* The inherent speed of the digital arithmetic unit appreciably exceeds that of any one analogue unit. On the other hand, the analogue simulator employs a multitude of units. Thus the speeds of the two systems are about equal for simulator use, at least at the present time.

(d) *Precision.* Digital machines are capable of unlimited precision whereas analogue machines are inherently low-precision devices. Where high precision is a prerequisite, only a digital system can be used. For most simulators, however, precision is not a serious factor.

(e) *Accuracy.* Analogue systems are parallel systems, performing all operations simultaneously through a large set of continuously varying units. Consequently, all parameters are available at all times; however, because of the multiplicity of interconnections, the computation of the parameters is generally somewhat inaccurate. Digital systems are sequential systems, performing all operations in time sequence through the one arithmetic unit. Consequently, all parameters are computed for discrete instants, at which points they are known as accurately as the component data allow; however, between these points the parameters are known only implicitly and generally must be assumed to agree with values obtained by means of approximation formulas.

(f) *Stability.* Both systems perform stably either where the computation is rudimentary or where a complex computation may be performed at indefinitely low speed. Similarly, both systems tend to instability when a complex computation must be performed in real time. The region of failure is a matter of study in each case as it arises. It is frequently necessary to simplify a complex computation for real time simulation.

(g) *Input-Output.* Information received by the computer is generally supplied in analogue form. Similarly, information transmitted by the computer is generally required in analogue form. Clearly the analogue simulator has the advantage here since it is prepared to accept and supply information in requisite form. The digital simulator must be provided with mechanisms for coding analogue parameters into digital form and vice versa.

(h) *Flexibility.* It is in this respect that digital systems show a marked superiority. In order to switch from one routine to another on analogue computers it is necessary to rearrange and/or replace a large number of physical components, requiring appreciable effort and time. In the case of digital computers each routine is represented by instructions and numbers recorded on an external storage device such as a punched or magnetic tape, and the tapes are conveniently filed away in compact form in a library of routines. Alteration of a routine (hence, the complete simulator) is effected by changing tapes.

It might be argued that in simulator use the process of switching a digital computer from the simulation of one device to another requires connecting the computer physically to a second unit for input-output purpose. But these connections are relatively few and probably would be handled through switches or multiple-contact plugs. In any case the same problem occurs of necessity using any simulation device, including analogue ones.

(i) *Future Possibilities.* The probability of marked mprovements in analogue computers is rather low, partly because analogue devices have already gone through many stages of development in the past, partly because modern improvements in speed and accuracy appear to depend on increased size of units. On the other hand, digital computers are still in their infancy and all indications point to smaller, faster machines in the not too distant future; it is particularly important to note that digital computation speed appears to improve with decreased size of units.

From the above, it follows that a choice between analogue and digital simulation is not clear cut. It is to be hoped that the results of projects which compare the capabilities of the two computer types for performing particular tasks, will bring to light and emphasize the relative advantages and disavantages of both.

ACKNOWLEDGMENT

The comparison of analogue and digital computers delineated above is part of a more detailed comparison set forth in connection with a project sponsored by Special Devices Center, Office of Naval Research.

The System Design of the IBM Type 701 Computer*

WERNER BUCHHOLZ†, MEMBER, IRE

***Summary*—In designing any new piece of equipment a choice has to be made from a number of alternatives. Rather than just enumerating the features incorporated in the IBM Type 701 Computer, an attempt is made to record the reasons for their choice. Emphasis is given to the features which are believed to be new. These include improved arithmetic and logical facilities, as well as the methods developed for controlling the extensive input and output equipment directly from the stored program.**

INTRODUCTION

A LARGE, GENERAL-purpose, electronic digital computer is probably the most complex equipment made which has to function as one coordinated, centrally controlled machine. Not only the equipment, but also the logic behind it is complex. For such a complex system to be successful, it is important that the proposed design first be thoroughly evaluated while it is only on paper and construction has not been started. A realistic appraisal of the system design can be obtained at that stage by writing actual programs for proposed applications. Weaknesses thus discovered may be removed and any unnecessary features eliminated. It is entirely uneconomical to make these improvements by building, testing, and scrapping several experimental models of such a large machine, and it has been found that small pilot models are not very useful because they do not exhibit many of the important characteristics of the full-scale machine. Computers with a stored program lend themselves readily to experimentation on paper since the program as written on paper completely determines the action of the computer. Hence this method of approach was used in arriving at the best system for the IBM Electronic Data Processing Machines Type 701 and Associated Equipment, the complete name given to the large-scale, high-speed electronic computer installations produced by the International Business Machines Corporation.

The development of the basic logic of a system as large as the Type 701 computer becomes a specialized effort which is distinct from, but must be closely integrated with, the design of the electronic and electromechanical equipment.[1-4] Engineers familiar with the

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 25, 1953.

† International Business Machines Corp., Engineering Laboratory, Poughkeepsie, N. Y.

[1] L. D. Stevens, "Engineering organization of input and output for the IBM 701 electronic data-processing machine," *Proc. Joint AIEE-IRE-ACM Computer Conference;* March, 1953.

[2] J. Logue, A. Brennemann, and A. Koelsch, "Engineering experience in the design and operation of a large-scale electrostatic memory," *IRE Convention Record;* March, 1953.

[3] C. E. Frizzell, "Engineering description of the IBM type 701 computer," PROC. I.R.E., pp. 1275–1287; this issue.

[4] H. D. Ross, Jr., "The arithmetic element of the IBM type 701 computer," PROC. I.R.E., pp. 1287–1294; this issue.

components and mathematicians having experience in using computers, both contributed at an early stage to the evaluation of the proposed system. There were many alternatives to be considered, and an attempt is made in this paper to set down the reasons for choosing the features incorporated in the final design. Many of these choices were interrelated, so that designing the system took on some of the aspects of solving a giant jigsaw puzzle. The complex nature of the puzzle may be obscured by the effort made to keep the logic of the computer simple. Rather than single out those features which are believed to be new, it is intended here to present them in the context of the over-all organization of the 701 system.

The 701 is a parallel binary computer designed primarily to solve large problems in scientific and engineering computation. It is the first such system to be manufactured in quantity. The computer is controlled by a stored program of single-address instructions. It has a large internal high-speed memory, large even by present-day standards as set by its immediate predecessors. This storage is further supplemented by the lower-speed, but higher-capacity, magnetic drum storage and by magnetic tape. There is a complete set of input-output components in the system, including punched cards and a line-at-a-time printer, as well as the magnetic tapes, all of which are under the direct control of the computer program. The number of such input-output devices can be varied to suit the requirements of individual installations.

The arithmetic speed of the 701 compares well with that of other fast computers. In the 701, however, high speed is combined with high storage capacity and fast input and output. On large problems, therefore, where the internal capacity must be supplemented by external devices, the 701 can produce results faster than any other computer in existence. The 701 was specifically designed to tackle problems which extend beyond the range of existing computers. But the versatility of the input-output also permits the 701 to be used efficiently on small problems when they occur in large numbers in an organization with central computing facilities.

Providing such extensive input-output facilities necessitated the development of effective techniques for their control which are considered to be new. The internal logic of the computer has also been refined, as compared with computers preceding the 701, and a number of features have been incorporated which greatly simplify its programming.

GENERAL DESIGN PHILOSOPHY

Throughout the design of the system the philosophy has been to keep the equipment to a minimum, to make that equipment fit a simple logical pattern, and to avoid special-purpose devices. An effort has been made to keep the instructions as simple as possible and to avoid obscure restrictions and overlapping between the functions of different instructions. While the equipment was being designed there existed a strict regime of discarding any frill which would not be of benefit in more than one type of application.

Avoiding special-purpose equipment not only decreased the cost but also increases the reliability. For the same reason, standard, well-tried components are used as much as possible, especially for input and output. By providing high-speed card readers and punches, existing punched-card equipment becomes available as an auxiliary to the computing installation. Standard keypunches, for instance, can be used to punch and print on cards for the purpose of introducing new programs and original data in a convenient, accurate, and readable form.

THE INTERNAL SYSTEM

Number System

The internal operation of the 701 is entirely in the binary system, but the input and output equipment will handle decimal and alphabetic, as well as binary, data. Thus the input-output advantages of a decimal machine are combined with the simplicity and low cost inherent in a binary computer. The simplicity of binary operation is particularly evident in multiplication and division. A further advantage of the binary system is that any other code system can readily be re-coded in terms of binary numbers; for instance, punched cards can be read and analyzed in the 701 regardless of whether they are punched in decimal, alphabetic, or any other code including any form of control punching.[5] A decimal-binary translation is, of course, required at the input and output, but the translation program can overlap with the operation of the card reader, punch, or printer, so that the time taken for translation does not normally slow down the input and output.

In order to achieve the high internal speed needed for scientific computing, the bits (binary digits) of a number or word are handled in parallel. "Word" is the term usually used to include numbers as well as instructions and other non-numeric information; the maximum number of bits in a word, including the sign bit if any, is called the word length. The proper choice of word length, and hence the number of parallel channels required in the computer, presents a question which cannot be answered lightly. If the word length is too short there will be many applications for which a single word is not enough to carry all the bits needed to represent a number. Because of the accumulation of unavoidable rounding and truncation errors, it may become necessary to carry more bits during a calculation than are retained for the answers. Hence too short a word length leads to the necessity of using two or more words for each number, and simple additions or multiplications must be replaced by very much more complicated, space- and time-consuming, "multiple-precision" operations. As a result much of the high speed and storage capacity of an otherwise good computer is nullified.

---

[5] M. M. Astrahan and N. Rochester, "The logical organization of the new IBM scientific calculator," *Proc. Assn. for Computing Machinery;* May, 1952.

Too great a word length is also bad. The time for carrying and shifting increases, and thus the speed goes down. The cost of the arithmetic circuits and registers, and the cost for a given number of words of storage go up. Only a few applications will need the full word length; hence there will be a strong tendency to pack several numbers into one word so that the cost may be reduced by keeping the amount of storage to a minimum. Unpacking these numbers requires instructions and time, and the effective speed and storage capacity would be cut still further.

Thus with a given set of applications there will be an optimum word length for which the speed is at a maximum or the cost is at a minimum. The relation between the variables is, of course, far from simple, and a compromise is needed in any case. For the 701 a survey of proposed applications was made, and it was found that the range of word lengths between 10 and 12 decimal digits would be satisfactory. There exists a broad peak of efficiency in this range. Below 10 digits there are too many problems requiring double-precision arithmetic, and there are not enough problems which could make effective use of more than 12 digits. Numbers of 10 or 12 decimal digits with sign can be represented in binary form by a minimum of 35 or 41 bits, respectively, including sign. Hence the survey showed that the word length of the 701 should be in the range of 35 to 41 bits.

Several other factors then quickly narrowed down the choice of word length. The single-address type of instruction, with the number of operations and the memory size being considered, required a minimum length of 18 bits, so that for the most efficient packing of instructions in memory the word length should be a multiple of 18. For engineering reasons the magnetic tape was to be provided with up to six parallel information channels; hence words could be recorded on tape most efficiently if the word length was to be a multiple of 6. The desire to reduce the bulk and the cost of the computer further prompted a choice near the bottom of the range of 35 to 41 bits. The final choice of 36 bits fills all these specifications.

Types of Storage

The 701 has three types of high-speed storage: electrostatic, magnetic drum, and magnetic tape. (Cards are also a form of storage, but they do not share the high speed and the possibility of rereading, or erasing and rewriting, previously recorded information without manual intervention.) The three storage media complement each other in their properties. Electrostatic storage is the fastest and has the shortest time of access to any one storage location. For that reason it functions as the internal working memory. But at the present stage of development it is still a fairly bulky and costly form of storage when considering the volume and cost per bit stored. Magnetic tape, though slower, is quite a fast medium when information can be organized on tape in the order in which it is to be used. But the time to gain access to any one item stored on a tape reel at *random* is counted in minutes instead of microseconds. On the other hand, the volume and the cost of tape storage are extremely low. Tape and electrostatic storage together thus take care of the two extreme requirements of high storage capacity and low access time. Drums were provided as a third medium to bridge the rather wide gap between the other two. Drums are useful for auxiliary programs or tabular data which may be needed in random order but not so often that a delay of a few tens of milliseconds would seriously affect the over-all computing time.

The electrostatic type of working memory was chosen because it makes practical a combination of high operating speed and adequate storage capacity. Although it shares these properties with memory devices of the recirculating type which have been used in many computers, electrostatic memory has yet a further advantage. Its short access time permits instructions to be stored at any location and in any order without affecting speed or performance. Thus there is no need for elaborate efforts to attain speed and efficiency by optimum programming. The random-access property also makes it easier to operate input, output, and external storage devices out of synchronism with the central computer. Memory can receive or supply information on only a few microseconds' notice; yet it can wait indefinitely if an external unit is not ready. Hence just a minimum of buffer storage is needed to tie the various units together. Most of the external units use a single one-word buffer register, namely, the multiplier-quotient register which is already there for arithmetic purposes. Tape requires an extra 6-bit register, the only special-purpose buffer storage in the machine.

Electrostatic memory, as used in the 701,[2,3] requires regeneration at regular intervals since it is a volatile type of storage. It needs adequate regeneration just as it needs an adequate supply of power in order to retain information. This could be done by interrupting operations and regenerating all of memory in one lump, whenever necessary. Instead it was decided to regenerate memory whenever it is not used for other purposes and to satisfy the need for further regeneration by attaching a number of extra regeneration cycles to each instruction, the number depending on how hard that instruction uses memory. In this way it becomes possible (see Table I, right) to determine exactly how much time each instruction takes, a necessary step when one wants to save time by overlapping internal and external operations, as will be discussed later on. Memory was designed according to the specification that regeneration should be adequate to avoid any restrictions on how usable programs may be written. Regeneration in a computer, like the supply of power, is not something active with which the user should have to concern himself.

TABLE I

LIST OF 701 INSTRUCTIONS WITH BRIEF EXPLANATIONS

Code	Short Name	Time[6]	Full Name and Explanation[7]
00	*Stop*	—	*Stop and Transfer* Stop, and prepare to transfer to x (see *Tr*) when the computer is started again.
01	*Tr*	48 (24)	*Transfer* Take the next instruction from half-word address x.
02	*Tr Ov*	48 (24)	*Transfer on Overflow* Transfer to x only if the overflow indicator is on; then reset the overflow indicator.
03	*Tr+*	48 (24)	*Transfer on Plus* Transfer to x only if the accumulator sign is plus; the other accumulator positions are ignored.
04	*Tr 0*	48 (24)	*Transfer on Zero* Transfer to x only if the accumulator contains zero; the accumulator sign is ignored.
05	*Sub*	60 (36)	*Subtract* Subtract the contents of x from the accumulator.
06	*R Sub*	60 (36)	*Reset and Subtract* Reset the accumulator to zero before subtracting.
07	*Sub Ab*	60 (36)	*Subtract Absolute Value* Subtract the absolute value of the contents of x from the accumulator.
08	*No Op*	48 (24)	*No Operation* Do nothing.
09	*Add*	60 (36)	*Add* Add the contents of x to the accumulator.
10	*R Add*	60 (36)	*Reset and Add* Reset the accumulator to zero before adding.
11	*Add Ab*	60 (36)	*Add Absolute Value* Add the absolute value of the contents of x to the accumulator.
12	*Store*	60 (24)	*Store* Store the accumulator contents (except the two overflow positions) at x, replacing the previous contents; the accumulator is left unchanged.
+13	*Store A*	60 (24)	*Store Address* Store the contents of bit positions 6 through 17 of the accumulator in place of the rightmost 12 bits at half-word address x. Note: Instruction must have + sign part.
−13	*Extr*	60 (24)	*Extract* Wherever an accumulator bit position contains a zero (or +), store a zero (or +) in the corresponding position at memory address x; leave all other bits in memory unchanged. Note: Instruction must have − sign part.
14	*Store MQ*	60 (24)	*Store Number from MQ Register* Store the contents of the *MQ* register at x.
15	*Load MQ*	60 (24)	*Load MQ Register* Load the contents of x into the *MQ* register.
16	*Mpy*	456	*Multiply* Multiply the contents of x by the contents of the *MQ* register. The most significant 35 bits of product are left in accumulator and the others in *MQ* register, in place of their previous contents.
17	*Mpy R*	456	*Multiply and Round* The same as *Mpy* followed by *Round*, giving a rounded 35-bit product.
18	*Div*	456	*Divide* Divide contents of the accumulator and *MQ* register, taken as a unit, by the contents of x. Contents of x must exceed in magnitude the accumulator contents. The resultant quotient appears in the *MQ* register, and the remainder is left in the accumulator.
19	*Round*	48 (24)	*Round* Increase the magnitude of the accumulator contents by one in position 35, if there is a one in position 1 of the *MQ* register. The *MQ* register is not changed.
20	*L Left*	48 (24)[8]	*Long Left Shift* Shift both the accumulator and *MQ* register contents as a unit to the left by x places (x not greater than 255). The accumulator sign is set to that of the *MQ* register.
21	*L Right*	48 (24)[8]	*Long Right Shift* Shift both accumulator and *MQ* register contents as a unit to right by x places. *MQ* register sign is set to that of the accumulator.
22	*A Left*	48 (24)[8]	*Accumulator Left Shift* Shift accumulator contents to left by x places. Sign is not changed.
23	*A Right*	48 (24)[8]	*Accumulator Right Shift* Shift the accumulator contents to the right by x places. The sign is not changed.
24	*Read*	48 (24)[9]	*Prepare to Read* Prepare to read one unit record from the input component specified by x. Start mechanical movement forward if necessary.
25	*Read B*	48 (24)[9]	*Prepare to Read Backward* (For tape only.) Same as *Read* except tape is moved backward.
26	*Write*	48 (24)	*Prepare to Write* Prepare to write one unit record on the output component specified by x. Start mechanical movement forward, if necessary.
27	*Write EF*	48 (24)[9]	*Write End of File* (For tape only.) Write an end-of-file gap on the tape unit specified by x.
28	*Rewind*	48 (24)	*Rewind Tape* (For tape only.) Rewind tape unit specified by x to starting point.
29	*Set Dr*	48 (24)	*Set Drum Address* (For drum only.) Set up x as the drum address of the first of a sequence of words to be read or written on the drum specified by the last preceding *Read* or *Write* instruction.
30	*Sense*	48 (24)	*Sense and Skip, or Control* If x specifies an input, sense input line for a signal; if a signal is present, skip the next instruction. If x specifies an output, send out a control signal; do not skip.
31	*Copy*	60 (24)[9]	*Copy and Skip* 1. If reading, store one word arriving from the input at memory address x. At the end of a unit record, skip *two* instructions. At the end of a file (i.e. after the last record is read), skip *one* instruction. Otherwise do not skip. 2. If writing, send one word from memory, address x to the output; do not skip.

---

[6] The normal time is given first. The time in parentheses applies only if this is one of 12 instructions immediately following *Mpy*, *Mpy R*, or *Div*.

[7] x denotes the address part of an instruction.

[8] These are minimum times. Time to shift $= 12(1+K)$ microseconds where K is smallest integer $\geq x/8$, provided this exceeds the minimum of 48 (24) microseconds.

[9] These times may increase if input-output synchronization requires a delay.

While the power is on, regeneration is the normal state of rest.

Storage Capacity

A high-speed, stored-program computer cannot be used efficiently unless the number of words available in the working memory is large enough. The size of the 701 memory was determined from a study of several proposed applications. The memory had to be able to accommodate the data and instructions for those sections of a problem which consume most of the calculating time.

Memory sizes of 2^{10}, 2^{11}, and 2^{12} words were considered, these numbers being convenient choices for binary addressing systems. On the basis of experience obtained prior to 1951, the time of the application study, it was concluded that 2^{10} words would not be enough, but that 2^{11} or 2048 words of 36 bits would be an adequate memory size for the sample problems. One reason for this rather large size, by present standards, was the policy of replacing control circuits by subprograms, as will be discussed in later sections. Sufficient memory space had to be allowed for these subprograms, but the memory assignment is quite arbitrary and the extra memory adds considerable flexibility at relatively low cost when compared with a design of less memory and more special-purpose control circuits.

The 1951 study also indicated, however, that there would be little advantage in making the working memory much larger than indicated above. Once a certain size is reached, additional high-speed memory does not contribute much. Big problems which do not fit can then be split efficiently into smaller sections which do fit. The sections not in current use are stored on drum or tape, depending on the frequency with which they must be called into electrostatic memory. Drums and tape are successively larger storage reservoirs which back up the working memory; tape has the further property that it is an output medium which can be removed for safekeeping and used as an input at any later time to reintroduce data or instructions into the computer. Because of the long initial access times of tape and drum storage, information should be moved into and out of memory in large blocks. No attempt has been made to provide convenient access to individual words of data or instructions in these auxiliary storages. Before instructions stored on tape or drums can be executed, an entire program or block of instructions must first be placed into electrostatic memory. The high speed inherent in the 701 would not be effective otherwise.

Because of the choice of 2048 words as the electrostatic memory capacity, drum storage has also been split into logical blocks of 2048 words. Thus, if desired, the entire memory could be unloaded into one block of drum storage. For structural reasons, four such logical blocks were placed into one physical package of drum storage. Hence drum storage comes in increments of 8192 words. Tape provides an even larger jump in capacity. About 115 blocks of the size of memory can be stored on one reel of tape. Tape drives are built in pairs, again for engineering reasons. Four tape drives are considered a standard complement. Four are sufficient for many applications, and this number of tapes also permits sorting of data by repeated merging. The amount of tape and drum storage provided can be changed, however, depending on individual requirements.

Arithmetic and Program Control

The arithmetic elements of the 701 are described elsewhere,[4] and the methods used internally for adding, subtracting, multiplying, and storing the results will not be discussed here. The external characteristics of these operations are apparent from the brief list of instructions in Table I. For ease of reference, Fig. 1 shows the information paths of the 701 in schematic form. The arithmetic system is noteworthy for its simplicity. No more than three registers are needed: the memory register, the accumulator register, and the multiplier-quotient register (*MQ* register). Of these three, the memory register serves purely internal functions, such as holding the multiplicand during successive cycles of multiplication so as to avoid repeated access to memory. The accumulator and *MQ* registers are the only ones which need to concern the programmer since they participate actively in arithmetic and other operations. The *MQ* register also doubles as a buffer register for external units, as has been mentioned. The *MQ* register thus is the only link between the internal information paths and the outside world.

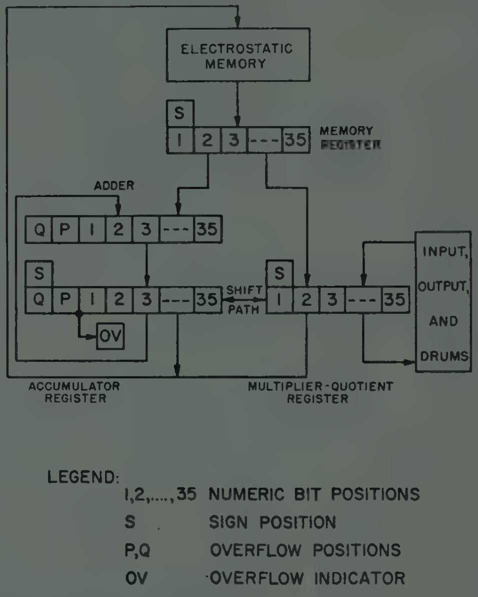


Fig. 1—Block diagram of information paths.

The block diagram of Fig. 2 shows the registers required to execute a program stored in memory. The *instruction counter* keeps track of the location of the next instruction to be executed. Normally it advances by one step for each instruction. Instructions called from memory first go to the memory register already mentioned. From there the various components of an instruction—the sign, the operation part, and the address part—are switched to the *sign register*, the *operation register*, and the *address register*. These registers are used to set up the memory deflection and the appropriate switching paths required for the execution of the instructions.[3]

Single-Address Instructions

The 701 employs a single-address system of instructions. Only one address in memory or one external unit may be specified with one instruction, in addition to the operation which is to be carried out. The single-address system is the simplest of the various systems possible, some of which may be more economical in storage space and computer time. These savings were not considered worth the extra equipment needed with multiple-address systems.

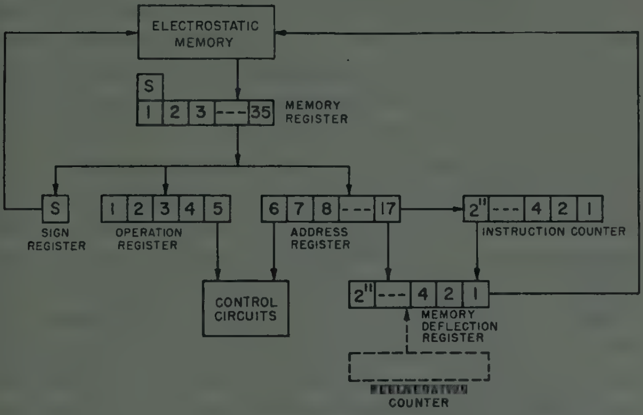


Fig. 2—Block diagram of program control paths.

One instruction is represented by 18 bits which are made up of the sign bit, 5 bits for the operation part, and 12 bits for the address part. The 5 bits of the operation part provide for 2^5 or 32 different operations. A 33rd operation, *Extract*, was added by making use of the sign bit. The 33 operations are listed in TABLE I together with short explanations. It will be seen from this table that the abbreviated names, which are recommended for writing out a program, are not just arbitrary codes surrounded by an aura of mystery. They are derived from, and immediately suggest, the full names of the operations which, in turn, were carefully chosen to be meaningful English phrases. These abbreviations make it much easier for a person to read a program which he did not write himself. Attention to such detail has been found most valuable in introducing newcomers to the computing field.

Full-Word and Half-Word Addressing

Since one instruction is made up of 18 bits, a 36-bit word can hold two instructions. Thus an important property of the 701 is that any full word of 36 bits (or 35 numeric bits and sign) can be split into two half words of 18 bits (or 17 numeric bits and sign), each half word being separately addressable. This greatly simplifies programs which must modify instructions and doubles the memory capacity for storing data which do not require more than 18 bits, the equivalent of about 5 decimal digits and a sign. The capacity of electrostatic memory is thus 2048 full words or 4096 half words, or an intermediate number if they are mixed.

TABLE II

SUMMARY OF 701 SYSTEM CHARACTERISTICS

General:
- Parallel operation.
- Binary notation internally.
- Control by stored program.

Word Size:
- Either 36 bits or 18 bits, including sign; approximately equivalent to 10 or 5 decimal digits and sign.
- Accumulator has two extra bits for overflow.

Instructions:
- Single-address system.
- 33 distinct operations.
- Instructions are 18-bit words.

Computing Speed:
- Multiplication or Division: 0.456 millisecond.
- Addition or Subtraction: 0.060 millisecond.

Electrostatic Storage:
- Capacity—2048 words of 36 bits each.
- Each full-word location may store a pair of 18-bit words.
- 72 tubes, 1024 bits per tube.

Magnetic Drums:
- Four drums, each with a capacity of 2048 words of 36 bits each, in basic system.
- Average access time to first word of block—40 millisceonds.
- Reading or writing rate—800 words per second.

Magnetic Tapes:
- Four magnetic tape units in basic system.
- Material: Oxide-coated plastic tape, ½ inch wide.
- Recording in 7 parallel channels, 6 for information and 1 for redundancy checking.
- Tape may be written forward, read forward, or read backward under program control.
- Density within a unit record: 200 words per foot.
- Distance between unit records—1 inch.
- Maximum tape length on reel—1400 ft.
- Access time to start of unit record—approx. 10 milliseconds.
- Reading or writing rate within unit record—1250 words per second.

Page Printer:
- Rate—150 lines per minute.
- Prints numeric, alphabetic, and special characters.
- Prints at full speed in decimal form using simultaneous conversion program.
- Prints 72 characters in any of 120 character positions on one line, more at reduced speed.
- Automatic line spacing or skipping, under control of stored program.

Card Reader and Card Punch:
- Reads or punches any 72 of the 80 card columns.
- Reading rate—150 cards per minute.
- Punching rate—100 cards per minute.
- Reads or punches cards in standard IBM decimal code at full speed using simultaneous conversion program.
- Reads or punches cards in binary form at full speed with 24 words of 36 bits each to a card.

Full and half words are addressable independently in a manner which puts the assignment of specific areas in memory to either size of word entirely under the control of the programmer. Addresses are designated by 12-bit binary numbers and a sign. This allows for 2^{12} or 4096 different addresses, and each of the 4096 half words has its own address. Full words are designated by even addresses only. For those instructions which can refer to either full or half words, the sign part is used to indicate whether the address part specifies a full word (minus) or a half word (plus). For example, a full word of 36 bits (S, 1, 2, 3, . . . 35) may have the address -1962. If the same 36 bits were used to store two half words, their addresses would be $+1962$ for the left 18 bits (S, 1, 2, . . . 17) and $+1963$ for the right 18 bits (18, 19, 20, . . . 35). Bit 18 of the full word becomes the sign bit (S) of half word $+1963$, bit 19 becomes bit 1, and so on.

With this system there is no doubt as to whether a given space in memory has already been assigned, because the numbers designating the addresses of full words and of the corresponding half words are alike, except for the sign and the even-odd part of the units digit. Another advantage of this addressing system is that the locations in memory of successive instructions, each of which occupies a half word, are numbered consecutively. It is also possible to transfer control directly to any instruction, regardless of which position in a full word it occupies.

The distinction between full and half words is made solely in electrostatic memory. Only full words, which may, of course, represent pairs of half words or instructions, are transmitted to and from input-output devices or stored on the drums. When a half word is entered from memory into the computer it is treated as a full word, of which the left 18 bits (including sign) are the specified half word and the right 18 bits are zeros. This is so regardless of whether the half-word address was even or odd. Similarly, on storing numbers from the accumulator or *MQ* register, the contents of the left half (bits S, 1, 2, . . . 17) can be stored at any half-word address in memory.

The rather arbitrary choice of moving the half word to the left end of the computer registers was intended to make the multiplication of full words and half words consistent with each other. The computer arithmetic acts as if all numbers were fractions with the binary point immediately to the left of the leftmost bit (bit 1). Because of the shifting facilities there is no difficulty, however, in handling numbers with the binary point in different positions.

Absolute-Value Representation

Positive or negative binary numbers are always stored as absolute values with a separate bit indicating the sign. Although the complement of a number may appear in the accumulator during a subtraction, the number will be re-complemented immediately to restore the answer to the absolute-value form at the end of the operation. The reason for insisting on an absolute-value representation of negative numbers in the 701 does not become evident until one goes beyond simple addition and subtraction to such processes as multiplication, division, shifting, and overflow control. It is then seen that permitting complements to appear in the accumulator at the end of an operation—or, worse yet, in memory—results in a long chain of complications whenever negative numbers are involved. Having negative numbers represented in absolute-value form is a feature well worth the extra re-complementing step which must be provided internally for addition and subtraction.

A property of complement systems is that two numbers having the same absolute value but opposite signs are represented by two different arrays of numeric bits. They differ, in the complement system commonly used for parallel binary machines, by having ones and zeros interchanged. This duality is objectionable when doing non-arithmetic operations. The absolute-value system of the 701 provides the same numeric representation for numbers of opposite signs. On the other hand, there is a possibility in the 701 of the number zero having either a plus or a minus sign. An effort was made in the early stages of design to avoid a schizophrenic zero by incorporating "watch-dog" circuits which would force all zero results to have a plus sign. None of the schemes, however, were entirely consistent and they only led to a confusion of rules and exceptions. It was finally decided to permit either sign.

The difficulty, if any exists, is really one of logic and is not one introduced by the machine designer. In common usage, zero means "nothing," and there is no meaning to a sign of zero. In computer language, however, a zero must be represented by some configuration of bits including the sign bit which does not have, in addition to + and −, a third state of "no sign." The ordinary rules of arithmetic give no clue as to the choice between the two signs, and the only sensible thing to do is to establish an additional rule for the sign which the machine will attach to a zero result. The 701 has a "sticky sign" rule for addition or subtraction: When the result in the accumulator is zero, the sign previously in the accumulator sticks to that result. For multiplication and division the rule to be used is obvious; for example, $(+0)(-1)=-0$.

Actually, in the language of the machine, $+0$ and -0 are two different configurations of bits, and if -0 were arbitrarily suppressed by a special circuit the machine would be blind to one of the 2^{36} configurations of 36 bits. This would be a serious drawback in attempting to perform logical operations on non-numeric information. The machine would be unable to recognize, for example, the existence of a hole in only the sign column of a decimally punched card if that was the only hole in that row of the card.[1]

Multiplication and Division

For scientific computation the most important characteristic of the 701 is the high speed at which it multiplies or divides full words. If one adds together the time taken to obtain and execute a *Multiply* or *Multiply and Round* or *Divide* instruction, one obtains a total of 456 microseconds. However, the actual increase in the overall operating time for each multiplication or division inserted into the program of any real problem is, in general, very much less than that. The reason is that, following one of the instructions *Mpy* or *Mpy R* or *Div*, a number of regeneration cycles are omitted during the execution of the next 12 instructions. Thus these 12 instructions take considerably less time. (If the 12 instructions should include another *Mpy* or *Mpy R* or *Div*, the count of 12 starts over again.[3]) If we credit this saving against the *Mpy* or *Mpy R* or *Div* instruction which initiated it, we can state that the multiplication or division time has been reduced correspondingly below the norm of 456 microseconds. The theoretical minimum is 24 microseconds, although this is only reached if the 12 subsequent instructions happen to be of the *Store* instruction type. The actual time for a particular program can be calculated with the aid of TABLE I. In a practical program the effective time for each multiplication or division is usually observed to be around 150 microseconds.

Division should be the inverse of multiplication. Since multiplying two full-word (35-bit) factors generates a double-length (70-bit) product in the accumulator and *MQ* register, division has been similarly arranged to start with a double-length (70-bit) dividend stored in the accumulator and *MQ* register. This appears to be an elementary piece of logic, and it is surprising that a double-length dividend has not been provided in other computers of this type. A double-length dividend makes it much more convenient to program the division of integers or of mixed numbers (see section on *Shifting*). It becomes possible also to obtain a properly rounded 35-bit quotient without resorting to time-consuming double-precision techniques. It may be seen that, before starting to divide, one need only add one-half the divisor (that is, the divisor shifted one place to the right) to the low-order 35 bits of the dividend.

After a division without rounding, the proper remainder, with the sign of the dividend, is available in the accumulator. This is of great value for double-precision calculations as well as for certain logical operations.

Shifting

The four shift operations provide very flexible facilities for both arithmetic and logical purposes. The two accumulator shifts, *Accumulator Left* and *Accumulator Right*, cause the contents of the accumulator to be shifted to the left or right by the number of places specified in the address part. Excess bits at one end of the accumulator are dropped, and zeros are entered in the vacated places at the other end. The accumulator sign remains unchanged. There is no shifting into or out of the sign position.

The two long shifts, *Long Left* and *Long Right*, treat the accumulator and *MQ* registers as one long register with bit 1 of the *MQ* register joined immediately to the right of bit 35 of the accumulator register. Again the desired number of places by which the contents of the two registers are shifted jointly is specified by the address part. The signs of the two registers are made to agree: During *Long Left* the accumulator sign is set to agree with the *MQ* sign, during *Long Right* the *MQ* sign is set to that of the accumulator.

The long shifts are useful not only for moving entire words between the accumulator and *MQ* registers without going through memory, but also for positioning the binary point before a multiplication or division. Regardless of where the point is located in the fixed-point representation of two numbers, the 701 can multiply them and position the point in the final result in only four steps:

Load MQ
Mpy
Long Left or *Long Right*
Store

Rounding would take only one additional instruction. Division is equally easy, but the shifting is done before dividing instead of after.

For floating-point computations it is desirable to be able to calculate the difference of two exponents and then to shift a number of places equal to this difference. Since the difference can be quite large at times, the shift instructions have been arranged to accommodate shifts by as many as 255 places, although the result of a shift by a large number of places is, of course, just a string of zeros. The point is that, by providing for such a large number, a foreknowledge of the actual magnitude of a shift, which is to be calculated by the machine, is not needed to guard against exceeding the capacity.

At the other end of the scale, it is possible to specify zero places of shift. *Long Left* 0000 and *Long Right* 0000 do no shifting, but they do set the signs as described above. This feature provides a useful aid in programming.

Overflow Control

What to do about an overflow resulting from an arithmetic operation was recognized as a problem very early in the design of the 701, because known methods of dealing with an overflow were considered clumsy and inadequate. The method finally adopted for overflow control crystallized over a period of time, from ideas contributed by many different people, to become what is thought to be one of the most useful novel features in the 701 arithmetic.

As shown in Fig. 1, the accumulator capacity has been extended by providing two extra bit positions to the left of bit 1 which are not found elsewhere in the machine. These two overflow positions, labeled *P* and *Q*, have the same carrying, adding, and shifting facilities as the other 35 numeric bit positions of the accumulator, but they cannot receive information from memory nor store their contents in memory.

The overflow positions greatly simplify double-precision arithmetic. Double-precision addition, for instance, is reduced to the following steps:

1. Add the two lower halves and store the sum.

2. Shift the accumulator contents to the right by 35 places.
3. Add the two upper halves to the accumulator contents and store the sum.

Any overflow during step 1 is shifted to the right in step 2. It is thus automatically carried into the addition of step 3, regardless of the signs of the numbers.

The second overflow position was provided to take care of double-precision multiplication where, after four double-length partial products have been generated, one must accumulate up to three components of these partial products. This will give rise in some cases to a second overflow.[10]

Just providing storage for overflow bits is not enough; in many programs there has to be a way of recognizing that an overflow occurred. For this purpose an overflow indicator is provided (Fig. 1). The indicator is turned on by carries from bit 1 to bit P; it is also turned on when a binary one is shifted to the left out of bit position 1. The state of the indicator is tested by means of the *Transfer on Overflow* instruction (which then turns off the indicator). This permits the program to be altered, if desired, after an overflow. On the other hand—and this is just as important—the occurrence of an overflow can also be ignored. The 701 does not stop as a result of an overflow unless it is programmed to do so.

It should be noted that the overflow indicator does *not* indicate the contents of the overflow positions P and Q; rather it shows whether a binary one was carried or shifted out of bit position 1. Successive carries or a shift may have moved the one-bit well beyond the P and Q positions so that it is lost, but the indicator remains on. Also subsequent operations, other than *Transfer on Overflow*, will not turn off the indicator even though the P and Q positions may have been cleared. If overflows can occur at several stages of a program, the indicator may have to be tested only once at the end of a program.

It is important to have available both the overflow indicator and the overflow positions in the accumulator. The indicator provides a simple test to signal that an overflow occurred, the result without the overflow may be stored in memory, and yet the overflow bits can be recovered from the overflow positions merely by a shift to the right. It is worth pointing out that the two extra positions in the accumulator are not equivalent to building a 38-bit machine. Having two extra bits in the accumulator which cannot be stored in memory is perhaps more useful than increasing the capacity of the entire machine by two bits.

Rounding

Numbers have an unfortunate tendency to grow in length during the course of a calculation. To keep from losing the most significant bits at the left end of a number which has outgrown the capacity of the registers, the programmer may have to arrange for shifting numbers to the right at intervals. Thus, in order to save the most significant bits on the left, some of the least significant bits must be dropped on the right. This causes the numbers to be slightly in error, the error being cumulative unless it is compensated for. The programmer may reduce this error to a minimum by modifying, or "rounding," the remaining part of the number so as to compensate for the loss of the bits which were dropped.

This well-known problem in numerical analysis has no single solution. Different calculations may require different methods of rounding in order to reduce the residual rounding error to an acceptably low level. However, for the majority of applications a simple adjustment applied to the lowest remaining bit of the number to be rounded is sufficient, and it was decided, therefore, to provide a general-purpose *Round* instruction in the 701. More elaborate rounding must be programmed explicitly.

Two alternative methods of built-in rounding were considered. One was the short cut, found in many binary computers, of forcing a binary one in the lowest position which remains. The second, and somewhat more complicated, approach consists of adding a binary one in the highest position to be discarded and propagating carries, if any, to the left into the remaining portion of the number. The second alternative was adopted because the maximum possible rounding error is only half of that of the first method and because it is familiar to us as the binary equivalent of the rounding process commonly used in decimal hand-computing. For both methods successive rounding errors tend to cancel. If we deal only with numbers whose bits are randomly distributed, the probable error, obtained by averaging the errors of all possible bit combinations, is the same for both rounding methods and decreases as the number of bits to be dropped increases. The probable error vanishes if those numbers can have either sign at random, provided the rounding process is applied to the absolute value of the numbers. The absence of a strong bias to produce cumulative errors is an important criterion in the choice of a rounding process.

---

[10] The fact that three product components must be added is a necessary, but not a sufficient, condition to prove that a second overflow will actually occur. The proof will be supplied by an example: Assume that the product (01 11)(01 11) is to be formed by double-precision multiplication on a machine which, for convenience, has been reduced from 35 bits to a word length of 2 bits, excluding sign:

(01 11)(01 11)				Factors
		10	01	Partial Products
	00	11		
	00	11		
00	01			
	12	1		Carries
00	11	00	01	Product

The double overflow occurs when adding the 2-bit numbers in the second column from the right, so that two carries into the third column are needed. The same example can be applied to a 35-bit machine by adding 33 zeros at both ends of each factor.

In the 701 the *Round* instruction was designed to work in conjunction with the *Long Right* shift: *Long Right* places the bits to be dropped into the *MQ* register; *Round* then leaves a rounded number in the accumulator. Actually, the *MQ* register is not changed by the *Round* instruction. Its highest bit position is merely *tested*; if it contains a one, then a one is added to bit position 35 of the accumulator. The combination of just two instructions, *Long Right* and *Round*, provides a rounded right shift after the detection of an overflow. Because rounding after multiplication is even more common, a separate *Multiply and Round* instruction has been included. It does the same thing as *Multiply* followed by *Round* but needs no extra time for rounding.

Store Address and Extract

The *Store Address* instruction is used for the common logical process of changing the address part of an instruction. The contents of bits 6 to 17 of the accumulator are stored in memory in the corresponding part of the specified half word which would be the address part of an instruction. The other bits are left unchanged.

In some applications it is desirable to have a more general method of changing selected bits of a word in memory. The operation *Extract* has been provided, an operation somewhat different, however, from what is commonly known as "extract." In the 701 the *Extract* operation causes the specified full word in memory to be modified by changing every bit in memory to a zero (or + for the sign), if the corresponding bit in the accumulator is a zero (or +); wherever the accumulator has a one (or −), the corresponding memory position remains unchanged. Another way of putting it is that the operation causes every bit at the specified memory address to be replaced by the logical product of the bit previously there and the corresponding bit in the accumulator.

Extract is especially useful when storing more than two numbers, each of less than 18 bits, in a single full word, and when doing things such as counting the number of binary ones in a word. Non-arithmetic applications of this type may be rather limited, but the equipment required to incorporate *Extract* into the 701 turned out to be surprisingly simple.

Sense

The *Sense* instruction is a special means of communication between the computer and the outside world. It is used in a variety of ways to control input-output equipment and to turn on signal lights on the operator's panel. The pluggable control panels for the card reader, card punch, and printer have terminals which can be sensed or actuated by the *Sense* instruction. Of particular interest is its use in conjunction with six "sense switches" on the operator's panel.

Each of the switches can be addressed individually by the *Sense* instruction. If the switch is up, nothing happens and the program continues to the next instruction. If the switch is down, however, the program skips the next instruction. Thus *Sense*, followed by an unconditional *Transfer*, can provide the operator with a set of alternative programs under control of the front panel switches.

For example, one switch might be used to stop the computer at the next convenient break-point. Another switch might be set up to cause the machine to print selected data for the purpose of diagnosing troubles, the printing being normally suppressed to save time. The six switches have no pre-determined functions; the programmer may use them in any manner to the limit of his ingenuity.

Checking

In the absence of complete agreement among mathematicians as to the proper methods of checking scientific and engineering calculations, and because of the cost of building checking facilities of doubtful value, the policy adopted was to provide only very little built-in checking. The engineering effort, which would have been spent on designing extra equipment, was diverted to increasing the reliability of the functional parts of the computer. The experience already gained in running the laboratory model of the 701 as a full-fledged computing installation has amply justified this policy. It has confirmed the belief that the best approach is to rely almost entirely on programs to discover errors from any source, including the computer, the data, and the programs themselves.

EXTERNAL SYSTEM

Program Control of External Units

Card readers, card punches, printers, magnetic tape units, and magnetic drum units represent a wide variety of input-output and external storage devices, all of which are under control of the stored program. Control is accomplished by a basic procedure which is common to all these external units. Only the instructions *Write*, *Read*, and *Copy* are required, as well as *Set Drum* for the drums. To this basic procedure are added a few special functions required by the tape units.

We need to define here a few terms which are convenient in describing the operation of the 701. It is to be hoped that they will be found useful enough to become standard terms in the computer field.

Writing consists of moving information from electrostatic memory to an output or storage unit (card punch, printer, tape, or drum).

Reading consists of moving information from an input or storage unit (card reader, tape, or drum; also checking pulses from the printer) to electrostatic memory.

A Unit Record is a sequence of full words, which are read or written as a unit during a limited period of time or between starting and stopping of the appropriate input-output device. Specifically, for a card reader or punch, a unit record is the information contained on one card. For a printer, a unit record corresponds to one line of printing. On tape, a unit record is written as a continuous sequence of bits, the end of which is marked by an *end-of-record gap*. Thus two unit records on tape are always separated by an end-of-record gap which is long enough to permit stopping and starting the tape safely between records. (In the 701 the number of words in a unit record is variable and is determined by the program.)

A File is a sequence of unit records intended to be used together. It may be a deck of related cards or a page of printing. A file on tape consists of all the unit records on one reel starting at a standard point near the beginning of the reel and ending with an end-of-file gap. Any information beyond the end-of-file gap, which has been left unerased from previous use of the reel of tape, is not part of the file and is not read. The length of a file on tape is arbitrary, except that it cannot exceed the capacity of a reel of tape.

(It may be noted that the word "transfer" is being meticulously avoided in connection with moving information. To avoid confusion, the word "transfer" has been reserved exclusively for the function of transfer of control for which there appears to be no satisfactory alternative terminology.)

The instruction *Write* is used to specify the desired output unit and to prepare it for writing. Furthermore, it starts the mechanical motion of card punches, printers, or tape units; drums do not need starting since they are in continuous motion. Since punching, printing, and writing on tape are sequential operations, there is no need to define where to start writing on punches, printers, and tape units. Drums, however, require a separate instruction, *Set Drum*, to define the address on the drum at which writing is to start. *Set Drum* follows a *Write* which specifies the desired one of several drums.

After *Write*, and if necessary *Set Drum*, a sequence of *Copy* instructions is given. Each *Copy* specifies an address in electrostatic memory from which the next word is to be copied for the purpose of writing. As many *Copy* instructions are given as there are words in the unit record to be written. When the unit record is finished, the program proceeds to other operations. The lack of further *Copy* instructions causes the output unit to stop automatically. Before another unit record can be written on this or any other output unit, another *Write* instruction must be given. Thus *Write* always signals the start of a new record, and there is no doubt about whether a given *Copy* instruction was intended for the old or the new record.

Reading is similar to writing. A *Read* instruction selects an input unit and starts it if necessary. For drums *Set Drum* again specifies the starting address on the selected drum. A series of *Copy* instructions is then needed, one for each word to be read. Each *Copy* specifies where in electrostatic memory the word just read is to be stored. Again, each *Read* instruction indicates that a new record is to be started.

During reading it is necessary to be able to sense when the end of a record or a file occurs. This is done by placing two *Transfer* instructions immediately after the *Copy* instruction. The computer may then skip one or both *Transfer* instructions: one at the end of a file, two at the end of a record. Thus the program can be arranged to follow an appropriate course of action. In the middle of reading a record, there is no skipping after *Copy*.

Thus the basic series of instructions for writing or reading one unit record is:

Write or *Read*
(*Set Drum* for drums only)
Copy
Copy
Copy
.
.
.

Actually, the sequence of *Copy* instructions is usually replaced by a short iteration loop containing only one *Copy* instruction. The skipping feature mentioned was designed particularly for ease of interrupting such a loop at the end of a record or file.

When manipulating tape the above set of basic instructions is supplemented by three more: *Read Backward* for the purpose of reading a unit record on tape backward, *Write End of File* for writing the end-of-file gap previously mentioned, and *Rewind* for rewinding a reel of tape all the way back to the starting point. The printer uses the basic instructions in a rather special way when the printing is to be checked.[1]

Variable Record Length

From the above description it is evident that each word to be moved requires the execution of a separate *Copy* instruction which specifies the memory location of that word. Since an arbitrary number of *Copy* instructions can be given following *Read* or *Write*, the number of words in a unit record is likewise arbitrary within wide limits. The upper limit of the record length on tapes or drums is set by the capacity of the tape reel or the drum, which is far beyond practical requirements. The lower limit is one word. On cards the upper limit is set by the medium itself since no more than 12 rows and 80 columns are available. Actually, up to 24 words can be punched in binary form, covering all the rows and 72 of the 80 columns. Having a variable record length is particularly convenient in handling programs, since successive programs on a single program tape may be of widely different lengths. It also becomes unnecessary to fit data stored on tapes or drums into blocks of a fixed length. For instance, in matrix calculations each row (or column) of a matrix of any size can be arranged to be a unit record of appropriate length, and the complexity of the program is not affected by the order of the matrix.

The fact that external units are controlled by the program on a word-by-word basis has other advantages. It is not necessary to store words in memory in a fixed sequence; the program can be arranged to handle words in ascending or descending sequence, or in no sequence at all. Also a considerable amount of equipment for controlling external units was saved.

Overlap of Internal and External Operations

Following the execution of a *Copy* instruction there is time for the execution of several other instructions before the next *Copy* must be given. The computer is fast enough to go through the short iteration loop previously mentioned, which calculates the address for the next word, even at the high word rate of magnetic tape. The time intervals between successive words are much longer with mechanical card equipment and printers, so that it is possible to proceed with binary-decimal conversion programs in the intervals which occur during card reading, punching, and printing. There is, of course, a limit on the time available for computer operation in the interval between words, the limit depending on the equipment being used. Since the timing of an external unit cannot be changed once the unit has been set in motion, it is up to the computer to synchronize operations and to wait for the external unit whenever necessary. Programs are written with these limits in mind.

Fortunately, it is not necessary for the average programmer to concern himself with these details. He can use already prepared subprograms which are known to work and which he may not even understand. All he needs to specify is which unit, where in memory, how many words, etc. Adequate input-output subprograms were devised along with the design of the equipment to make sure that the projected design would work well. Developing the subprograms was really part of the design of the 701 system. The input-output subprograms are an alternative to having more equipment which would perform similar functions. There is one important difference, however. The people who designed the original subprograms had no doubts that ingenious users would later devise much better subprograms which would make the same computer a better machine. With built-in equipment such improvements can be made only with great difficulty. This feature has already paid dividends in that many new and improved input-output subprograms have been written since the 701 design was completed.

Self-Loading Procedure

Another area where the programming facilities of the computer have successfully replaced physical hardware is in the loading of a new program into the computer. There is a load button and a selector switch on the machine, but they do just barely enough to get the process started. The rest is accomplished by a technique sometimes called the "bootstrap technique." The switch determines whether the program is to be loaded from tape, cards, or drum. Pushing the load button then causes one full word to be loaded into a memory address previously set up on the address entry keys on the operator's panel, after which the program control is directed to that memory address and the computer starts automatically. In effect, the load button has executed the short program:

```
+Read       x
+Set Drum   0000 (applies to drums only)
-Copy       y
+Tr         y
```

where x is the identification of the input unit set up on the load selector switch and y is the (even) memory address set up on the address entry keys. So far one full word has been entered into memory, nothing more. The full word may, however, consist of two instructions of which one is a *Copy* instruction which can pull another full word or pair of instructions into adjacent addresses. The new pair may contain another *Copy* instruction to continue the process as long as necessary. For each *Copy* placed in memory another instruction is gained, so that one can rapidly build up a program loop which is capable of loading the actual operating program.

```
              Location  |  Instruction
              ----------+----------------------------
                0000    |  -Copy      0002
                0001    |  +R Add     0003
          |→    0002    |  +Add       0000*
Loading   |     0003    |  -Copy      (0004)†---¦ End-of-
Loop      |     0004    |  +Store A   0003      ¦ record
          |—    0005    |  +Tr        0002      ¦ skip
                0006    |  Start of operating ←-¦
                0007    |  program to be loaded.
                  .     |
                  .     |
                  .     |
                  .     |
```

* This instruction adds the contents of location 0000 to the contents of location 0003, which in effect adds 0002 to the address part of the *Copy* instruction at 0003 every time around the loading loop.

† The parentheses indicate that the address part will be modified during the execution of the program. 0004 is the initial value loaded by the first *Copy*.

Fig. 3—A self-loading program.

The self-loading technique is illustrated in the program of Fig. 3 where the starting address y is, for convenience, taken to be 0000. The first six instructions constitute the self-loading procedure. They are followed immediately by the instructions of the program to be loaded. The complete set of instructions forms a unit record which may be punched on a card or written on tape or drum. Pushing the load button causes the first pair of instructions to be loaded into addresses 0000 and 0001. The *Copy* instruction at 0000 loads the next pair into 0002 and 0003. The process may be seen to be self-sustaining. When the entire program has been loaded, an end-of-record signal is obtained which, as was mentioned earlier, automatically causes a skip from the *Copy* at 0003 to the start of the operating program at 0006. The above self-loading procedure is one of several in current use.

Tape Programming

The last section showed how a new program may be loaded from tape, drums, or cards. Tape and drum are similar in that they permit programs to be entered into memory at high speed. If repeated reference must be made to different parts of a long program which exceeds the capacity of electrostatic memory, these parts may be stored on drums and called into memory as needed. The drums must, however, be loaded first from an external source, that is, from tape or cards. In many computer installations a good deal of effort has gone into creating libraries of standard programs designed to simplify the programmer's task. Even a large library can be stored compactly on a single reel of magnetic tape. With the high speed of tape little time is wasted in skipping over unwanted programs in order to pick out the programs needed for a given job. For a large problem it may be more efficient to assemble a special program tape, particularly when the program may have to be re-entered on many different occasions. The effort required to prepare the tape once is repaid in the saving of operating time.

It will be noted that no equipment has been provided to key new programs by hand directly on tape. Such equipment would be simple enough to build, but the nature of a continuous medium like tape and the invisible method of recording make it a difficult problem to correct errors made by the key-recording operator. Inserting a set of missing instructions would be especially awkward. Instead, new programs for the 701 are first punched on cards in decimal form, one instruction to a card, using standard equipment to punch and print the program. Corrections can be easily made at that stage by substituting or inserting cards. Once the program is known to be correct, it may be translated to binary form and transcribed on tape in a brief preliminary run on the computer.

Card Programming

For short programs it may be more convenient to have the computer condense the decimal cards, on which a new program has been punched, to binary cards. A binary card can hold more than 40 instructions. A program of several hundred instructions thus occupies only a few cards and is loaded into the computer in just a few seconds; such a program is manipulated more easily on cards than if it were condensed even further on a few inches of tape. Many programmers prefer to keep their own private library of program cards, modified to fit their special requirements. While at his desk the programmer may then assemble into a single deck of cards some prepunched library programs together with cards especially punched for the problem to be solved. He need only give the assembled deck to an operator who may then combine it with other program decks to run off a whole series of problems as time becomes available on the computer. Thus by assembling his cards complete with auxiliary loading programs, etc., each programmer has control over the machine as far as his program is concerned, and operating errors are held to a minimum even when the machine is being run by relatively inexperienced operators. All the operator usually has to do is to insert the tapes, if any, and press the load button.

This technique has been found useful even when using longer programs which are stored on tape. Cards may be employed to sequence the programs and to introduce auxiliary programs. For instance, when troubles arise, different program cards may be inserted to print out indicative information, to modify the program, and to make corrections. The manual controls available on the operator's panel could be used to do all these things, but it is much too easy to push the wrong button. A far safer procedure is to rely on the prepunched cards which give the operator a chance to double-check what he is going to do. Thus the card reader can serve as an extension of the manual controls. For that reason a card reader has been placed within easy reach of the operator when he is seated at the operator's station.

Operator's Panel

The manual controls which are used most often by the operator are very few in number. They include the load controls already mentioned, controls to start, stop, and reset the computer, and buttons to turn the power on and off. The sense switches described earlier also fall into this category. The other controls are more likely to be used by the engineer servicing the machine. Instructions can be executed directly from the operator's panel, by-passing the stored program. For this purpose a set of 18 instruction entry keys are provided to enter an instruction into the program registers. Another set of 18 keys, the *MQ* entry keys, may be used to enter a half word into the *MQ* register. Neon lights are provided to display the contents of all registers, and the contents of any memory address may be inspected by the use of controls which bring the desired word into the memory register.

When maintaining the machine, the engineer may want to analyze a certain part of a program. For that purpose he may start the program at high speed until the instruction counter neon lights show that the desired point is being approached. He may then interrupt the machine and slow it down to a rate of about 5 instructions per second by holding down the multiple-step key. This is slow enough to permit him to stop within one or two instructions of the goal. By pressing the single-step key he can then proceed one instruction at a time, observing the results on the neon lights. High-speed operation can be resumed at any time by pressing the start button.

A considerable design effort was made to simplify the operator's panel and the associated circuits. Whenever feasible, circuits already required for other purposes were utilized and elaborate sequencing circuits were avoided. For instance, there is no special equipment for obtaining direct access to memory from the operator's panel. Information can only be entered directly into the *MQ* register; to store the information in memory, a *Store MQ* instruction must then be executed manually. The program loading procedure previously described is another example. The simple, yet effective, arrangement of the operator's controls was made possible by the decision to plan the operator's panel right at the start, along with the other input-output devices.

V. CONCLUSIONS

The primary characteristics of the new IBM Type 701 Computer, which are summarized in TABLE II, are high speed, large storage capacity, and an unusually complete array of input and output equipment. The 701 also includes a number of other new features which were described in this paper. Among them are:

1. Independently addressed half words and full words, providing direct access to each single-address instruction.
2. High-speed multiplication and division, requiring in effect only about 150 microseconds in many practical applications.
3. Division with double-length dividend and proper remainder.
4. Improved shift instructions.
5. Flexible control of arithmetic overflow.
6. Provision for altering a program manually in a manner predetermined by the program.
7. Integration of all input-output equipment with the computer.
8. Line-at-a-time printer capable of printing numeric and alphabetic characters.
9. Variable record length for input, output, and external storage.
10. Provision for flexible program control by tape or cards.
11. Programs substituting for equipment whenever possible, to achieve greater reliability and flexibility.

When taken together, these individual contributions to the art of building computers constitute a major improvement in the usefulness of such machines for scientific and engineering calculations.

ACKNOWLEDGMENTS

The logical system design of the 701 was primarily the responsibility of an engineering group, headed by N. Rochester, which included M. M. Astrahan, J. H. Holland, R. W. Murphy, and the author. Another and larger group of engineers under the direction of J. A. Haddad, produced the engineering design of the 701, and W. F. McClelland was in charge of a group of mathematicians responsible for the mathematical planning and application studies; both of these groups made substantial contributions to the ideas reported here. Generous assistance was received during the preparation of this paper from many members of the IBM Engineering Laboratory in Poughkeepsie, N. Y.

Engineering Description of the IBM Type 701 Computer*

CLARENCE E. FRIZZELL†, ASSOCIATE, IRE

Summary—**The IBM Electronic Data Processing Machines Type 701 and Associated Equipment constitute a large scale electronic digital calculator. These machines, which incorporate the newest devices for input, output, and storage, are currently in production at the IBM Plant 2, Poughkeepsie, N. Y. This paper presents a general engineering description of the 701 with emphasis on what are believed to be new techniques and concepts.**

INTRODUCTION

THE IBM ELECTRONIC Data Processing Machines Type 701 and Associated Equipment constitute an electronic digital calculator designed primarily for large scale scientific and technical computing. The calculator operates internally in the binary number system and is controlled by means of a stored program. The outstanding features of the machine include large capacity high-speed storage, dynamic sequential control, and a flexible input and output system.[1,2]

This paper presents a general engineering description of the IBM Electronic Data Processing Machines. The characteristics and functions of the computer are described with emphasis on what are believed to be new techniques and concepts.

A typical 701 installation, shown in Fig. 1, consists of the following units:

(a) Analytical Control Unit
(b) Electrostatic Storage Unit
(c) Magnetic Tape Readers and Recorders
(d) Magnetic Drum Reader and Recorder
(e) Punched Card Reader

---

* Decimal classification: 321.375.2. Original manuscript received by the Institute, June 25, 1953.

† International Business Machines Corp., Engineering Laboratory, Poughkeepsie, N. Y.

[1] M. M. Astrahan, and N. Rochester, "The Logical Organization of the New IBM Calculator," IBM Corp.; 1952.

[2] L. D. Stevens, "Engineering organization of input and output for the IBM 701 electronic data-processing machine," (Review of input and output equipment used in computing systems)—*Joint AIEE-IRE-ACM Computer Conference*, pp. 81–85; March, 1953.

Fig. 1—A typical 701 installation.

(f) Alphabetical Printer
(g) Punched Card Recorder
(h) Power Distribution Unit
(i) Power Units.

The full length word used throughout the machine consists of 35 binary digits and a binary sign digit. The calculator uses a single address system which is capable of calling for 36-bit full words or either of two 18-bit half words, which may be stored in a full word location. In fact, all machine instructions are half words and include a 5-bit operation part, a 12-bit address part and a sign bit. The sign bit indicates whether an operation is to affect a full or half word. A full word, a half word, and the arrangement of the three parts making up a machine instruction are illustrated in Fig. 2.

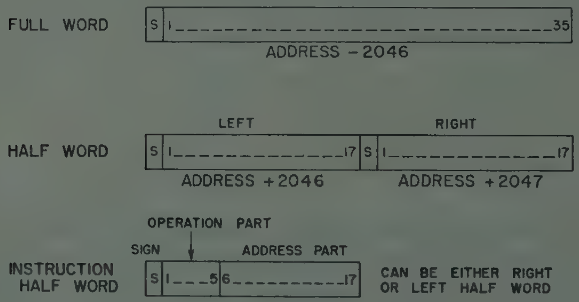


Fig. 2—Organization of words.

The high operating speed is made possible by the use of parallel transmission and arithmetic systems in conjunction with the rapid random-access Electrostatic Storage. Instructions are stored in the Electrostatic Storage and any one is available to the computer in one 12-microsecond machine cycle.

The calculator is capable of executing 33 different operations[3] as shown in Fig. 3. Twenty-five pertain to arithmetic operations, including shifts, transfers, and a programmed stop. The remaining eight control the various input and output units.

ARITHMETIC OPERATIONS

ADD
RESET AND ADD
ADD ABSOLUTE
STORE
STORE ADDRESS / EXTRACT
MULTIPLY
MULTIPLY ROUND
LONG LEFT
ACCUMULATOR LEFT
TRANSFER
TRANSFER ON PLUS
STOP AND TRANSFER

SUBTRACT
RESET AND SUBTRACT
SUBTRACT ABSOLUTE
LOAD M-Q
STORE M-Q
DIVIDE
ROUND
LONG RIGHT
ACCUMULATOR RIGHT
TRANSFER ON ZERO
TRANS ON OVERFLOW
NO OPERATION

INPUT/OUTPUT OPERATIONS

PREPARE TO READ
PREPARE TO WRITE
REWIND TAPE
COPY AND SKIP

PREPARE TO READ BACKWARDS
WRITE END OF FILE
SET DRUM ADDRESS
SENSE AND SKIP

Fig. 3—Calculator operations.

Program Control

The Program Control section of the 701 consists of the following logical blocks, which are shown in Fig. 4: Instruction Register, Instruction Counter, Operation Decoder and a Memory Deflection Register. The Instruction Register receives an instruction from the Electrostatic Storage, via the Memory Register. The Operation Part provides coded information to the Operation Decoder (diode matrix) whose output line (one of 32) conditions all control circuits required to execute the current instruction. The Sign Part is normally directed to the Electrostatic Storage control circuits to indicate either a full or half word operation. (In one instance the Sign Part is used to distinguish between two operations using the same Operation Part, *Store Address/Extract.*) The Address Part is used to specify an Electrostatic Storage location when reading or storing. It is also used to specify an Input-Output Unit, a drum address or the number of columns to be shifted.

The Address Part of the Instruction Register (12 column) consists of a four position trigger register (high order end) and an eight position binary counter. Coded address information is stored in these two parts and may be transferred to the Memory Deflection Register to select the desired Electrostatic Storage location.

The Address Part is also used to specify a particular Input-Output Unit when it is associated with a general Input-Output select instruction such as *Read* or *Write.*

---

[3] W. Buchholz, "Systems design features of the IBM type 701 computer," Proc. I.R.E., pp. 1262–1275; this issue.

The address is decoded by a Class Selector Matrix which energizes a specific select line.

The Address Part of *Shift* instructions is used to specify the number of columns to be shifted. This information is read into the eight position address counter (lower eight positions provide a maximum shift of 255 places) which counts down in synchronism with the shifting operation. A count of zero indicates the completion of the operation.

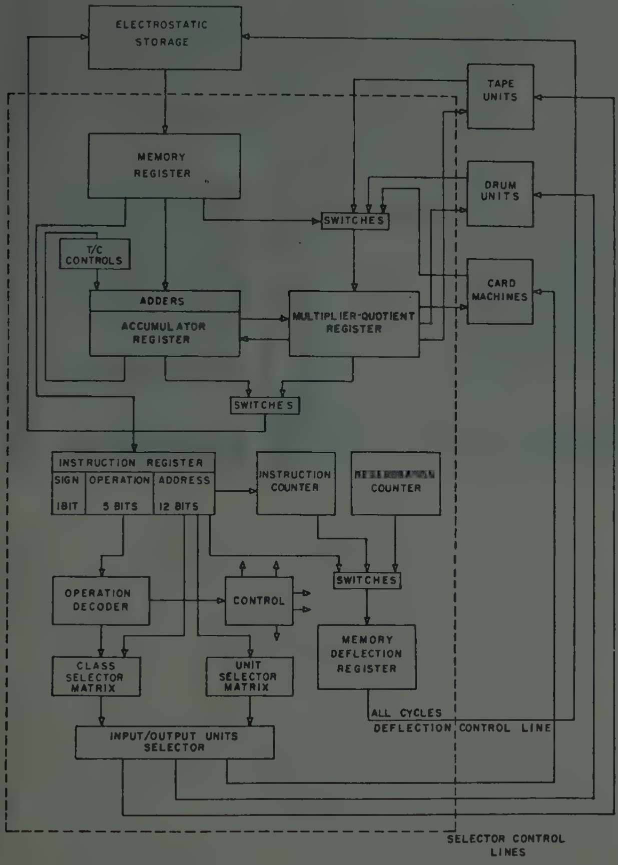


Fig. 4—Simplified block diagram of the IBM 701.

The Instruction Counter is a 12-position binary counter that may be advanced serially or read into in parallel. This counter contains the Electrostatic Storage location of the next instruction and is advanced by one at the end of each operation. Transfer instructions are executed by reading the 12-bit address from the Instruction Register into the Instruction Counter in a parallel manner.

The Memory Deflection Register, at all times, provides address information to the Electrostatic Storage Deflection Circuits. This information is obtained from the Instruction Counter, the Instruction Register or the Regeneration Counter. The Regeneration Counter provides the address of the next two full words to be regenerated. It is advanced by one, each regeneration cycle.

ARITHMETIC SECTION

All arithmetic is performed in the binary number system. All numbers transmitted throughout the calculator or stored in the Electrostatic Storage are true numbers. Ones' complement numbers are used when subtracting and the resulting difference, if it is a complement, is automatically converted to true form. The sign bit is then set in accordance with algebraic laws.

Addition is accomplished at the rate of one each 60 microseconds or 16,666 per second. This includes the time for obtaining the instruction to be performed and the number to be operated upon. This rate of performing addition also includes the Electrostatic Storage regeneration associated with the instruction and is discussed more fully in the section on Timing and Control Functions.

Multiplication is performed by the process of repeated addition and shifting. Division is performed by repeated subtraction and shifting. The time required for either operation is 456 microseconds. Furthermore, the net time required to execute a section of program, consisting of *Add* or *Store* or other instructions, is considerably reduced when this section of program immediately follows *Multiply*. (This technique is described in detail in the section on Timing and Control Functions.)

The principal elements of the Arithmetic Section, shown in the block diagram (Fig. 4), are as follows:

(a) Memory Register
(b) Accumulator Register
(c) Multiplier/Quotient Register
(d) Binary Adders
(e) True/Complement Controls.

The three registers used in the Arithmetic Section consist of Microsecond Delay Units[4] which were developed by B. L. Havens of the Watson Scientific Computing Laboratory. Each unit may be considered as a storage element whose output voltage level, during each one-microsecond period, is maintained at the same value as the input voltage level for the *preceding* one-microsecond period. Thus each unit will continuously store information when its output is connected to its input. These units may be conveniently used to form a one-megacycle shifting register by electronically switching the output of one unit to the input of an adjacent unit.

The delay feature is especially useful in the Accumulator Register. Here the Accumulator Register outputs serve as one set of inputs to the Adders and the Memory Register outputs serve as the other set. Each Adder is a germanium diode, matrix type, requiring static inputs to provide a sum at its outputs. In addition to providing information to the two inputs, time must be provided for carries to propagate and the resulting sum to reach a steady state. The delay feature, which enables the unit to read-in and read-out simultaneously, is used here to provide static Accumulator Register outputs to the Adders for a one-microsecond period while the Accumulator Register inputs are connected to the Adder outputs to read-in the sum. At the start of the next one-

---

[4] H. D. Ross, "The arithmetic elements of the type 701 computer," Proc. I.R.E., pp. 1287–1294; this issue.

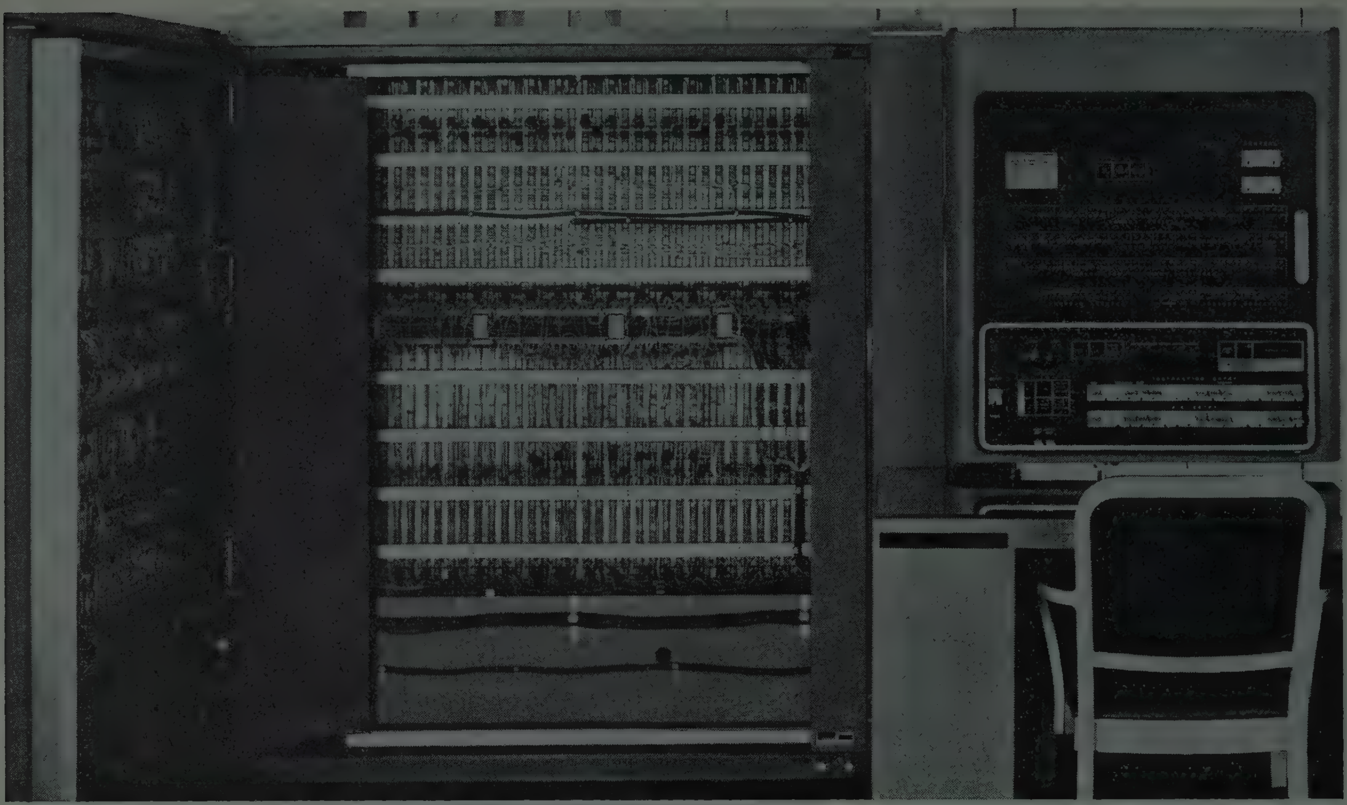


Fig. 5—Analytical control unit.

microsecond period the sum will appear in the Accumulator Register.

The Accumulator Register, having a capacity of 37 bits and a sign bit, stores the sum in the case of addition or the difference in the case of subtraction. It is also used as a shifting register, as product storage when multiplying, and as the dividend register when dividing. The Accumulator Register and Multiplier/Quotient Register are frequently coupled automatically to form a 72-bit register. In the case of multiplication, a 70-bit product may be developed with the most significant half (35 bits) appearing in the Accumulator Register, and the least significant half in the Multiplier/Quotient Register. The Accumulator Register is 38 bits long instead of 36 because it contains two additional positions on the left called Overflow positions. These are never stored directly but participate in arithmetic and shifting operations.

The Memory Register, having a capacity of 35 bits and a sign bit, functions as a storage register for all information coming from the Electrostatic Storage. In arithmetic operations this register stores the addend, subtrahend, multiplicand and the divisor.

The Multiplier/Quotient Register, having a capacity of 35 bits and a sign bit, serves many functions. It possesses shifting properties when coupled to the Accumulator Register. During multiplication, it is used to store the multiplier factor, which is eventually replaced by the least significant half of the 70-bit product; during division it stores the quotient as it is developed. The multiplier/Quotient Register also serves as a storage register for the asynchronous input or output devices.

Timing and Control Functions

The Analytical Control Unit, shown in Fig. 5, contains all master timing circuits, the arithmetic circuits, and the general controls required by the calculator.

The pulse repetition rate at which the computer functions is one megacycle per second. A twelve-stage ring of trigger circuits is used to generate the 12 one-microsecond pulses which together constitute one basic machine cycle. Since this is a synchronous machine, the selection of the basic cycle duration was based chiefly on timing requirements for the Electrostatic Storage.

The regeneration requirements of this type of memory may be met in a number of ways. In the 701, regeneration is considered a part of each instruction and is therefore distributed throughout the execution of a program. This is accomplished by assigning specific functions to each of four types of basic machine cycles: Instruction, Execution, Execution/Regeneration, and Regeneration. (These will be referred to as I, E, E/R and R cycles.) Since the major functions to be performed are the reading and interpretation of an instruction, the execution of an instruction and the regeneration of the electrostatic memory, the functional assignment by type of cycle is as follows:

(a) During an Instruction cycle (I) the next instruction is obtained from the Electrostatic Storage location specified by the Instruction Counter and set into an internal register called Instruction Register (Via the Memory Register). From here instruction is interpreted by a decoding matrix.

(b) During an Execution cycle (E) a reference is made to the Electrostatic Storage at the address specified by the address part of the current instruction. The instruction determines whether a number will be stored or read out.

(c) During an Execution/Regeneration cycle (*E*/*R*) action is taken to execute the current instruction and simultaneously one spot on each of the 72 cathode-ray tubes is regenerated (the location is specified by a Regeneration Counter). This type of cycle is used for the execution of an instruction (follows *I* cycle for instructions such as *Transfer* and *Shift*) when no additional information is required from the Electrostatic Storage. It is also used, following the read-out of data from the Electrostatic Storage, when additional time is required to complete the execution operation. (This is described in the following discussion of the operation *Add*).

(d) During a Regeneration cycle (*R*) one spot on each of the 72 cathode-ray tubes is regenerated just as during an *E*/*R* cycle. This type of cycle is used to complete the regeneration associated with each instruction or to preserve the contents of the Electrostatic Storage when the machine is in a ready or stop status. The method of associating *R* cycles with each instruction is described later.

Each of the 33 machine operations consists of a predetermined pattern of these basic cycles. The type of cycles, the number of cycles required and their sequence depends upon the nature of the operation to be performed. The cycle pattern for four typical operations is shown in Fig. 6.

TRANSFER I,E/R,$\underline{\text{R,R}}$ = 48 MICROSECONDS

ADD I,E,E/R,$\underline{\text{R,R}}$ = 60 MICROSECONDS

STORE I,E,$\underline{\text{R,R,R}}$ = 60 MICROSECONDS

MULTIPLY I,E,E/R—36 E/R CYCLES=456 MICROSECONDS

Fig. 6—Cycle pattern for four typical operations.

An *Add* operation consists of the following sequence of cycles: *I*, *E*, *E*/*R*. These are usually followed by two *R* cycles, as will be described later. During the *I* cycle the instruction is obtained from the Electrostatic Storage and the operation part is decoded by the Operation Decoder as the operation *Add*. The combination of the two conditions, *I* cycle and the Operation Decoder output *Add*, is used to call for an *E* cycle next. It should be noted that all machine operations are initiated by a similar combination of conditions.

The 12 one-microsecond timing pulses which make up all basic cycles are used as an additional condition to specify the time within a cycle for an operation to take place, For example, the call for the *E* cycle just mentioned occurs at the end of the *I* cycle. This is accomplished by mixing the *Add* condition with the twelfth (or last) timing pulse of the *I* cycle to generate a *Go To E* cycle signal. Similarly, during the *E* cycle, the word to be added is obtained from the Electrostatic Storage and placed in the Memory Register. Since insufficient time remains to complete the addition, the *Add* Operation Decoder output is mixed with the *E* cycle and last timing pulse to generate a *Go To E*/*R* cycle signal. During the *E*/*R* cycle addition is completed, and the sum placed in the Accumulator Register. Simultaneously, regeneration automatically occurs.

The regeneration requirements of an instruction are maintained by a circuit known as the Regeneration Control. This circuit assures the Electrostatic Storage of a minimum of three regeneration (*E*/*R* or *R*) cycles per instruction executed. This amount of regeneration is sufficient to insure reliable operation with any program.

Since each instruction is made up of a predetermined pattern of *I* and *E* or *E*/*R* cycles and since the pattern differs for various instructions, a signal must be generated to indicate the completion of an operation. This signal is generated at the end of the last cycle of the execution operation and is called the End of Operation pulse. It is used to sample the status of the Regeneration Control unit to determine whether the calculator may proceed to the next Instruction cycle or call for a Regeneration cycle. Should the fixed cycle pattern of the instruction just completed embody a minimum of three *E*/*R* cycles, the Regeneration Control circuit would permit the calculator to call for an Instruction cycle and read out the next instruction. However, if an instruction such as *Add*, whose cycle pattern is *I*, *E*, and *E*/*R*, was the one just completed, then two Regeneration cycles will be required before proceeding to the next instruction. The Regeneration cycles underscored in Fig. 6 are those called for by the Regeneration Control circuit to meet the requirement of three Regeneration cycles per instruction executed.

It will be noticed that 36 *E*/*R* cycles are shown as part of the cycle pattern for the instruction *Multiply*. Since this number of cycles greatly exceeds the normal regeneration requirement, the Regeneration Control circuit permits the following twelve instructions to be executed at a reduced rate of regeneration. This function is popularly called the "Twelve Free Games" feature. It means that the only regeneration performed dur-the twelve instructions following a *Multiply*, *Multiply and Round*, or *Divide* instruction (all three instructions have the same cycle pattern) is that which is provided by the *E*/*R* cycles.

The significance of the Free Games feature is that the instruction *Multiply*, which alone requires 38 machine cycles (456 microseconds), speeds the execution of the following twelve instructions so that, in effect, the multiplication time is reduced. This may be illustrated by assuming that the instruction *Multiply* is followed by six *Store* and six *Add* type instructions (see Fig. 6 for cycle pattern of each). The total time required for these 13 operations, without the Free Games feature, would be $456+6(60)+6(60)$ or a total of 1176 microseconds. However, since the reduction of the regeneration requirement associated with each instruction is the basis of this feature, the Regeneration Control circuit does not require the execution of the three R cycles following each *Store* instruction (see Fig. 6) or the two R cycles following each *Add* instruction.

By this means the time required to execute 30 machine cycles, at 12 microseconds each, is saved. This represents a decrease of 360 microseconds in the time specified (1176 microseconds) to perform the 13 operations. Since this time saving is achieved by performing a multiplication it is reasonable to subtract the 360 microseconds from the 456 microsecond multiply time which results in an effective multiplication time of 96 microseconds.

To summarize, the effective multiplication time is a function of the 12 instructions which follow and may vary from 24 microseconds (a rather unlikely situation requiring 12 following instructions such as *Store*) to 456 microseconds in the case where *Multiply* is followed by *Multiply*.

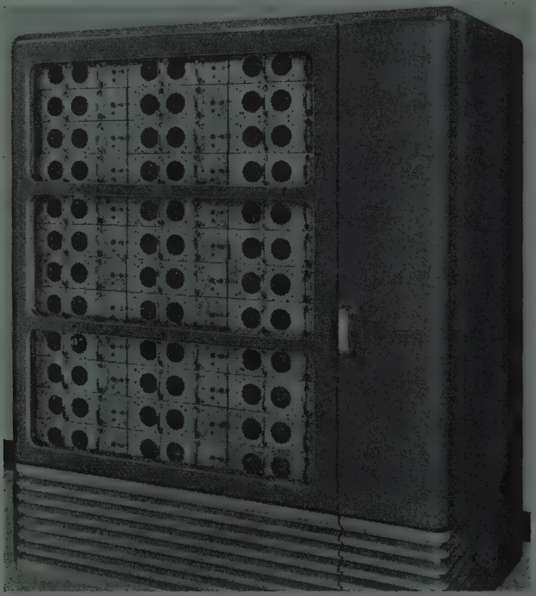


Fig. 7—Electrostatic storage unit.

ELECTROSTATIC STORAGE

The Electrostatic Storage Unit shown in Fig. 7 serves as the high-speed working memory and is an integral part of the 701. Instructions and data frequently required by the program are stored here, and all information transmitted between the various input and output units must pass through the Electrostatic Storage. The principle of storage used is essentially the dot-dash technique as described by F. C. Williams[5] and the access time may be considered to be one 12-microsecond machine cycle. The storage density is 1024 bits per c-r tube for a total high-speed storage capacity of 2048 full words. This is equivalent to approximately 20,480 decimal digits.

An Electrostatic Storage Unit consists of thirty-six pluggable Storage Drawers (see Fig. 8), a Deflection Gate, and special power supplies. Each Storage Drawer contains two 3-inch IBM-85 c-r tubes. This type is an improved version of the IBM-79 described by W. E. Mutter.[6]

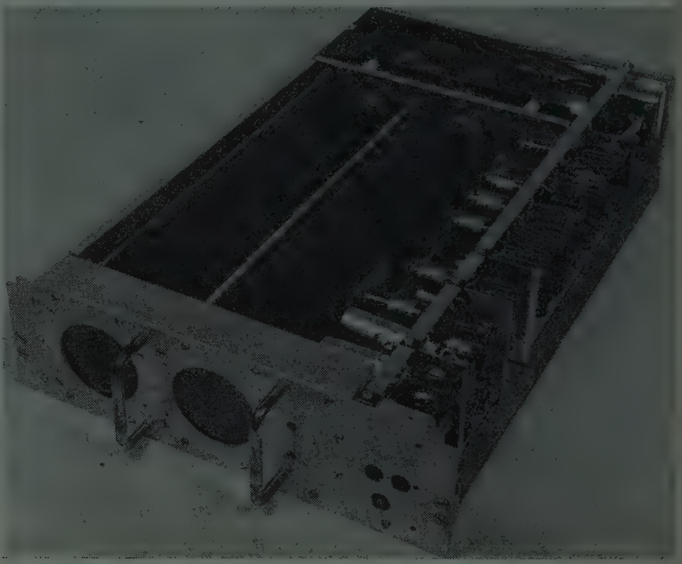


Fig. 8—Storage drawer.

One of the most serious difficulties encountered when using electrostatic storage is that of spill. Briefly, spill is the degeneration of the information stored on the face of a c-r tube as a result of repeated references to information in adjacent storage locations. In the 701 the effect of spill has been greatly reduced by the use of improved c-r tubes and by means of extensive address scattering.

The deflection system is common to all 72 c-r tubes and the selection of information is accomplished by control of the c-r tube beam-unblanking circuits. The assignment of address locations in the deflection system is arranged so that consecutively addressed half words, such as instructions, require the unblanking of a given c-r tube only once for each four instructions. That is, four consecutive address locations progress from left tubes (Storage Drawers S through 17), to left tubes (Storage Drawers 18 through 35), to right tubes (Storage Drawers S through 17), to right tubes (Storage Drawers 18 through 35).

Further scattering of addresses within the 1024 bit raster, as indicated in Fig. 9, provides a total of sixty-four consecutively addressed references before a reference is made to an address located adjacent to one previously used. For example, address 64 and address zero are adjacent and in the same tubes.

---

[5] F. C. Williams, and T. Kilburn, "A storage system for use with binary-digital computing machines," *Proc. IEE* (*London*), vol. 95, pp. 183–202; December, 1948.

[6] W. E. Mutter, "Improved cathode-ray tube for application in Williams memory system," *Elec. Eng.*, vol. 71, pp. 352–356; April, 1952.

This address scattering so distributes the I-cycle references that it is possible to neglect their contribution to spill. The *E*-cycle references are a direct function of the program. That is, the number of references to a given address and the address location is determined by the programmer; no restrictions have been placed on his decisions. Therefore, in the calculation of the required storage-tube read-around ratio, only the *E*-cycle references must be considered. The most severe loop that is possible by programming makes 342 references to a specific address before all adjacent addresses have been regenerated.

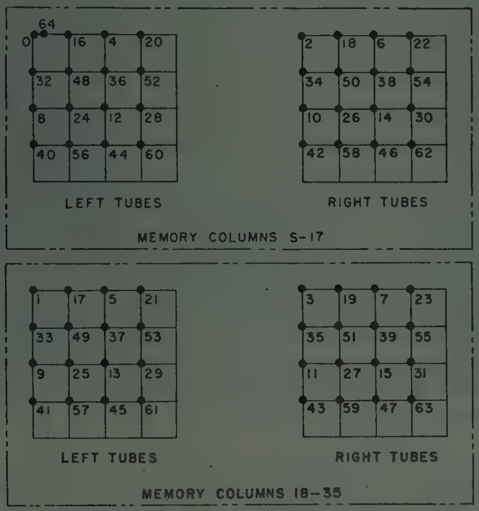


Fig. 9—Conventionalized view of storage tube rasters showing half-word address scattering.

The process of regenerating the Electrostatic Storage in the 701 has been speeded by the employment of two read-out pulses during each 12-microsecond Regeneration cycle. These read-out pulses unblank first the 36 left tubes and then the 36 right tubes. The resulting information is stored in triggers located in each Storage Drawer. At dash time, the time designated for writing, the storage triggers determine whether a dash is to be written or the existing dot is to remain. By this process two full words are regenerated each 12-microsecond Regeneration cycle, and only one video amplifier[7] is required for each two cathode-ray tubes.

The reduction in regeneration time afforded by improved cathode-ray tubes, address scattering and regeneration of two full words per regeneration cycle has greatly enhanced the efficiency of this computer. This reduction in regeneration time has been obtained while maintaining completely satisfactory operation of the Electrostatic Storage. The programmer is therefore not burdened by having to limit his demands on the Electrostatic Storage.

MAGNETIC TAPE SYSTEM

The Magnetic Tape Reader and Recorder, shown in Fig. 10, serves two functions in the 701 system. It may be used as either an intermediate speed, large-capacity storage for programs and data or it may serve as a high-speed input unit for information previously recorded on a reel of magnetic tape.

A Magnetic Tape Reader and Recorder contains two independent magnetic tape units. Each unit contains an 8-inch reel capable of holding up to 1200 feet of one-half inch, oxide-coated, non-metallic tape.

Recording is at a density of 100 bits per linear inch using the non-return-to-zero type of recording.[8] Seven parallel channels are recorded, six of which are information tracks and one is an odd-even check track. One full word is recorded in six groups of six bits per group, and information is transmitted between the Tape Unit and the Calculator in a serial-parallel manner. Since zero in a non-return-to-zero system is indicated by the absence of a pulse, the "one" bit recorded in the check track will insure that the arrival of an information group is indicated.

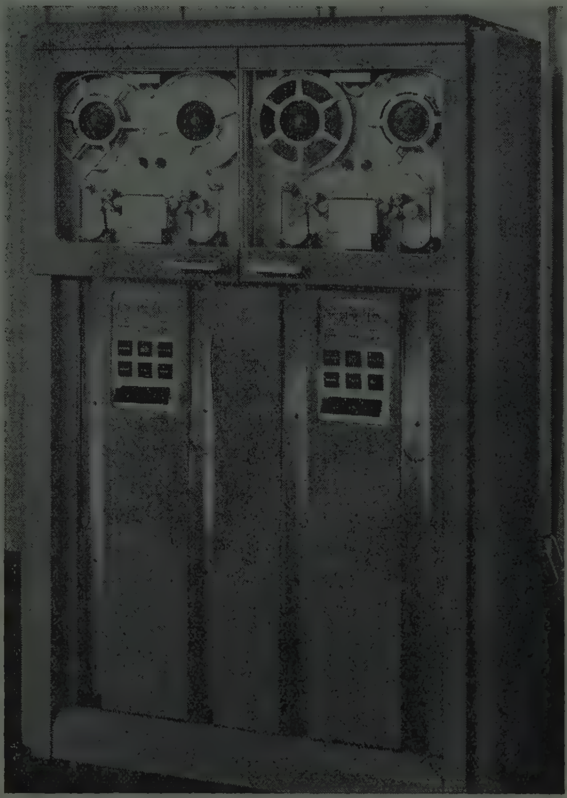


Fig. 10—Magnetic tape reader and recorder.

Two seven-bit registers are provided to serve as a temporary storage for each six-bit information group and the check bit. These registers consist of conventional trigger circuits. Their principal function is to compensate for time differences in the arrival of recorded bits due to tape skew. Since they have static outputs they also serve the valuable function of charging and discharging the capacitance of the signal cable between the tape unit and the calculator. After a suitable delay the seven signal lines are sampled and their status is read into columns S through 5 of the Multiplier/Quotient Register. The check bit is read into a Check Bit Trigger.

---

[7] J. C. Logue, A. E. Brennemann, and A. C. Koelsch, "Engineering experience in the design and operation of a large scale electrostatic memory," *IRE Convention Record*; 1953.

[8] H. W. Nordyke, "Magnetic tape recording techniques and performance," (Review of input and output equipment used in computing systems)—*Joint AIEE-IRE-ACM Computer Conference*, pp. 90–95; March, 1953.

Since the 701 is a 36 bit, parallel machine, and the transmission of information between all other units is on a 36 bit parallel basis, it is desirable to assemble the six 6-bit groups of a full word, received from the Magnetic Tape Units, into this form. The function is performed conveniently by the Multiplier/Quotient Register. This register is inherently a high-speed shifting register; by connecting the output of column S to the input of Column 35, a six bit group is ring-shifted six columns to the left and temporarily rests in the Multiplier/Quotient Register columns 30 through 35.[9]

Successive six-bit information groups are read-in to columns S through 5 and ring-shifted left until six such groups have been received. Recognition that a full word is now located in the Multiplier/Quotient Register will initiate an immediate transfer of this word to the Electrostatic Storage, providing a *Copy* instruction is waiting. This will be discussed below.

During the shifting operation the number of one bits are counted and the result is compared with the status of the Check Bit Trigger. If this check fails a Tape Check light is turned on.

It will be remembered that the Multiplier/Quotient Register functions as a storage register for all information coming from input or output devices. A *Copy* instruction is required to transfer this information between the Multiplier/Quotient Register and the Electrostatic Storage. The twelve bit address part of this instruction specifies the Electrostatic Storage address at which the word is to be stored or read. In general *Copy* is a synchronizing instruction that acts as a buffer agent between the asynchronous input-output units and the synchronous calculator. It is supplied by the program at the rate required by the input-output unit in use.

The process of recording on magnetic tape is the reverse of the reading operation except that the Multiplier/Quotient Register columns 30 through 35 are used as outputs to the Magnetic Tape Unit.

The initial access time to information recorded on tape is set at ten milliseconds, with succeeding full words being available each 800 microseconds. Tape operating speed is 75 inches per second,[10] which makes available to the calculator 1250 full words per second. This is equivalent to approximately 12,500 decimal digits per second.

MAGNETIC DRUM SYSTEM

The Magnetic Drum Reader and Recorder, shown in Fig. 11, serves as additional storage for programs or data which exceed the capacity of the Electrostatic Storage. This unit contains two physical drums, which are functionally organized into four logical drums, each capable of storing 2048 full words. The total storage capacity is 8192 full words which are equivalent to approximately 82,000 decimal digits.

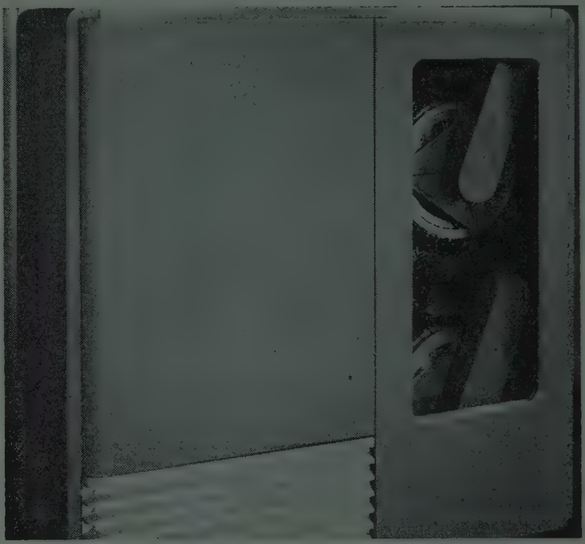


Fig. 11—Magnetic drum reader and recorder.

Each physical drum is a forged aluminum cylinder 13 inches in diameter, which is wound with Cunife (copper, nickel, iron) wire and ground to provide a true surface having the desired magnetic properties. The speed or rotation is 2929 rpm to obtain a surface speed of 2000 inches per second. A logical drum contains 36 information tracks, one index track and one timing track. The center to center spacing between tracks is 1/16 inch.

Each physical drum is enclosed in an aluminum housing containing 76 removable read/record heads which incorporate spring-loaded coil and lamination assemblies. A differential screw arrangement provides a vernier adjustment when setting the head to drum surface clearance.

Discrete pulse type of recording is used at a linear density of 50 bits to the inch and a drum timing track, consisting of 2048 recorded pulses, is used to locate the storage cells around the periphery of the drum.

The addressing system used consists of an eleven stage binary counter and a zero recognition circuit. After selecting one of the four logical drums by means of the instruction, (*Read Drum* or *Write Drum*) a *Set Drum* instruction may be given to specify the address of the first full-word to be read or recorded. Omission of the *Set Drum* instruction starts the reading or recording operation at drum address zero. The address part of this instruction is set into the eleven stage counter in parallel and programming may continue until the specified full-word is required. At this point in the program a *Copy* instruction must be given which, upon receipt of the index pulse, gates drum timing pulses to the address counter. This counter is connected so that it counts down and a count of zero denotes the arrival at the specified address.

---

[9] See footnote 2, p. 1275.

[10] W. S. Buslik, "IBM magnetic tape reader and recorder," (Review of input and output equipment used in computing systems)—*Joint AIEE-IRE-ACM Computer Conference*, pp. 86–90; March, 1953.

Thirty-six bits of information are read simultaneously and set into a drum register. From this point on the process is similar to the Magnetic Tape operation previously described except that the full-word (36 bits) is set into the Multiplier/Quotient Register in parallel. From there it is stored in the Electrostatic Storage by the *Copy* instruction.

An additional feature of this addressing system is that a second zero recognition circuit is connected to the lower seven stages of the address counter. A count of zero occurs here every 1280 microseconds and it denotes the arrival of the next higher address (The drum addressing system is arranged so that consecutively-addressed storage locations are separated by 127 actual locations). By this means the programmer is provided with sufficient time to allow the machine to calculate the next electrostatic storage address and provide another *Copy* instruction. This type of operation provides a variable record length, by programming, which is limited only by the number of *Copy* instructions given and the capacity of the drum (0 to 2048 full-words).

Since four 36 track logical drums are located in one frame, relay switching is employed so that 36 amplifiers and 36 writing circuits can accommodate the 144 information tracks. The write circuits are switched at their outputs. The amplifiers are switched at the cathode of a preamplifier in the reading circuits.

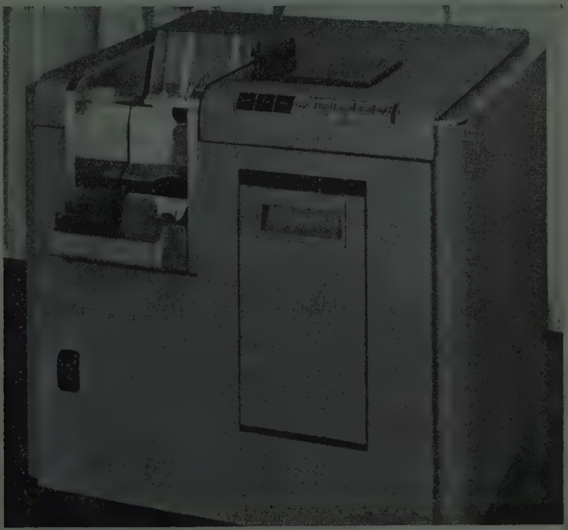


Fig. 12—Card reader.

PUNCHED CARD READER

Initial input to the calculator is by way of the Card Reader, which is shown in Fig. 12. Seventy-two columns of a punched card are read by brushes a row at a time. One such row of 72 columns constitutes two 36-bit full words, if binary punching is used. Thus a 12 row IBM card can contain 24 binary full words.

Cards are always read as though they contain binary punching and 24 full words, but if the information is punched in any other system, such as the familiar decimal punching, the calculator can be easily programmed to perform the conversion. The 72 columns can be read and converted, if necessary, at the rate of 150 cards per minute.

The signals from the brush circuits are set into Key Triggers. Key Triggers are flip-flop circuits having an integrating input for use with manual key switches and electromechanical devices such as brushes, cam operated contacts, and relay operated contacts.

Selection of the Card Reader is by means of the input/output instruction *Read* (Card Reader address), which sets the card feed in motion. Once selected, the program may continue for a maximum of 50 milliseconds, at which time the first row of the card has reached the reading brush station. One row of punched-hole information is automatically transferred to the 72 Key Triggers which are located in the Analytical Control Unit. Two *Copy* instructions are required to transfer this information, via the Multiplier/Quotient Register, to the Electrostatic Storage. Each group of 36 bits (one full-word) requires a *Copy* instruction to effect the information transfer and to designate the storage address. A period of 540 microseconds is available for programming between the first and second *Copy* instructions, thus permitting the modification of the *Copy* instruction address part. By this means loading may be accomplished by the use of a loop containing one *Copy* instruction and the few instructions required to modify its address part.

The time between information rows on the IBM punched-card allows the programmer complete freedom in programming for 15 milliseconds following the execution of the second *Copy* instruction. If the information being read is punched in a system other than binary, this period of time may be utilized to program the conversion.

A Control Panel is available on the Card Reader to provide facilities for the rearrangement of input data. Selective changes are made possible by the inclusion of selection relays which have multiple transfer contacts.

PRINTER

The line-at-a-time Printer, Fig. 13, is capable of printing 120 columns of information at a rate of 150 lines per minute. The transfer of information to the Printer is controlled by select (*Read* or *Write* Printer) and *Copy* instructions in a manner similar to that discussed in the section on the Card Reader. One basic difference is that information to be printed is transferred, via the Multiplier/Quotient Register, to 72 thyratrons (2D21). These thyratrons are located in the Analytical Control Unit and are used to energize either the print magnets, when printing, or the punch magnets, when the Card Recorder is the selected output unit. The Card Recorder is discussed in the next section.

Data to be printed are usually results of calculations which have been stored in the Electrostatic Storage. However, information recorded on a magnetic tape or a magnetic drum may be printed by first transferring it to the Electrostatic Storage Unit. The arrangement of these data in the desired sequence for printing may be performed during the transfer.

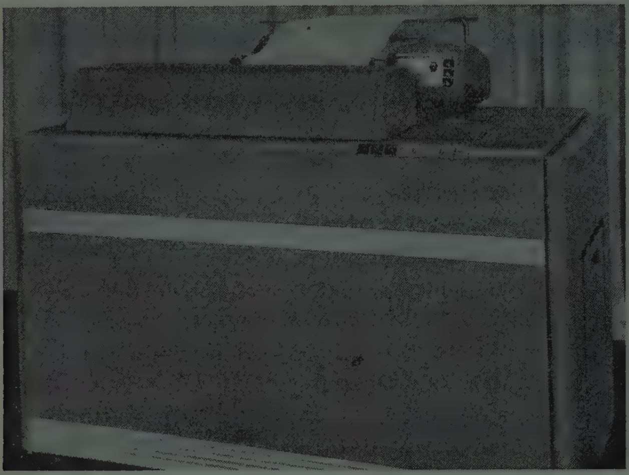


Fig. 13—Printer.

Conversion of the binary data into decimal form, as required by the Printer, is accomplished by programming. In order to reduce the lost time inherent in electromechanical input/output devices, the control circuits permit unrestricted programming for a period of 58 milliseconds after executing the Select Printer operation. This period is sufficient to convert by programming, seven binary full-words to seven 10 decimal digit numbers. At the conclusion of the 58 milliseconds period the program must provide two *Copy* instructions, in close succession, to effect the transfer of the first row (two words) of information to the Printer.

Checking of the actual printing is accomplished through the use of echo pulses which are generated by type-wheel contacts. These pulses indicate the time at which the type-wheel was set into motion, which determines the character to be printed. To perform this checking operation the select instruction *Read* (Printer address) and additional *Copy* instructions must be provided. The additional *Copy* instructions are required to transfer the echo information to the Electrostatic Storage where it may be compared by programming, with the information originally transmitted to the Printer.

Papers forms are handled by a punched-tape controlled carriage. However, all functions of this unit are available to the programmer and can be controlled by the program. Ten *Sense* exit lines from the calculator may be energized by *Sense* instructions to provide carriage control information.

CARD RECORDER

The Card Recorder, shown in Fig. 14, is a high-speed punch capable of punching information (usually decimal or binary) at the rate of 100 cards per minute. Operation of this output unit is similar to that of the Printer previously described. A *Write* (Card Recorder address) instruction is required to select this unit and set the card feed into motion. Following the execution of the select instruction, 70 milliseconds are available for programming before the first pair of *Copy* instructions are required. This time may be used to perform a binary to decimal conversion or other general programming. Two *Copy* instructions are required to transfer the information to be punched into each card row. Again the time between card rows is made available for unrestricted programming. When using the Card Recorder, this time is 31 milliseconds.

A maximum of 72 columns may be punched from the calculator exit busses. If desired, the remaining 8 columns may be used to gang-punch indicative information such as program code number.

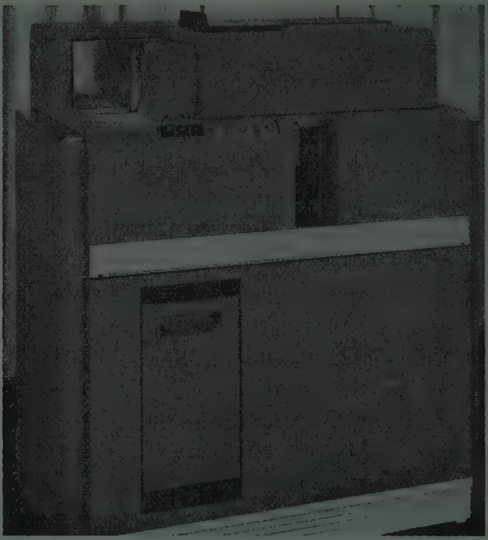


Fig. 14—Card recorder.

OPERATOR'S PANEL

The Operator's Panel is located at the Analytical Control Unit of the calculator and is shown in Fig. 15. Considerable attention has been given to the selection of controls and indicators and their arrangement on the panel. Simplicity has been stressed. Yet versatile and powerful control over the calculator is at all times possible.

Facilities are available for the visual inspection of any full word stored in the Electrostatic Storage by use of the Memory Register neon lamps. The panel also contains neon lamps for the purpose of automatically displaying the contents of the Accumulator Register, Multiplier/Quotient Register, Instruction Register and Instruction Counter. In addition, lights are provided to indicate the status of calculator controls which are of interest to the operator.

Buttons and key switches are available for manual entry of data or instructions, execution of any instruction, slow-speed, step-wise operation, and program alteration. Power *On* and Power *Off* Controls are also located here for the operator. In addition to the above, a Machine Cycle key switch and *DC ON* and *DC OFF* controls are available for the Calculator Engineer.

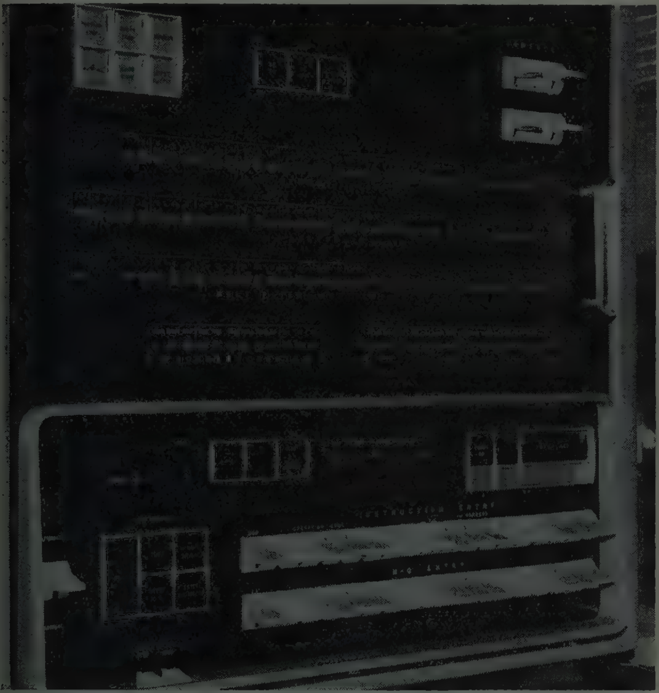


Fig. 15—Operator's panel.

POWER SUPPLY AND DISTRIBUTION UNIT

The Power Supply for the Type 701 was designed and built to IBM specifications by an outside source. It operates from a 208-volt, 3-phase, 4-wire, Y-connected, 60-cycle power source. The calculator is rated at 88kva.

The direct voltages used throughout the calculator are as follows:

+500 volts
+220 volts
+150 volts
+15 volts
−30 volts
−100 volts
−250 volts

The Power Distribution Unit, shown in Fig. 16, houses control relays, contactors, circuit breakers, fuses, timers, and a power control panel. In general it contains the equipment for the control and distribution of ac and dc power throughout the calculator.

All direct voltages are monitored at the Power Distribution Unit by ±5 per cent Sensitrols. These voltage monitoring devices protect the calculator components such as tubes, diodes, and resistors. This protection is accomplished by turning off all direct voltages in the event of a failure in one of the power supplies. A switch is provided on the Control Panel for each Sensitrol. These switches may be used to disable individual Senistrols so that a particular direct voltage may be varied in excess of ±5 per cent for the purpose of marginal checking.

Fuses are all located in the Distribution Unit and are of the spring-plunger type. When a fuse is blown it will turn off all alternating or direct voltages, depending upon the circuit in which the fuse is located. The decision to place all fuses in the Power Distribution Unit was made for the protection of the inter-frame ac and dc service voltage cables. That is, all service voltages are fused at the distribution point rather than at the load. A secondary benefit is the convenience of having only one place to look for a blown fuse.

Voltages are sequenced on in five voltage groups for protection of the vacuum tubes and to reduce the line surge. A fast-discharge circuit is used to bring all voltages down simultaneously and the discharge time constant of each supply is adjusted to maintain the correct voltage ratio.

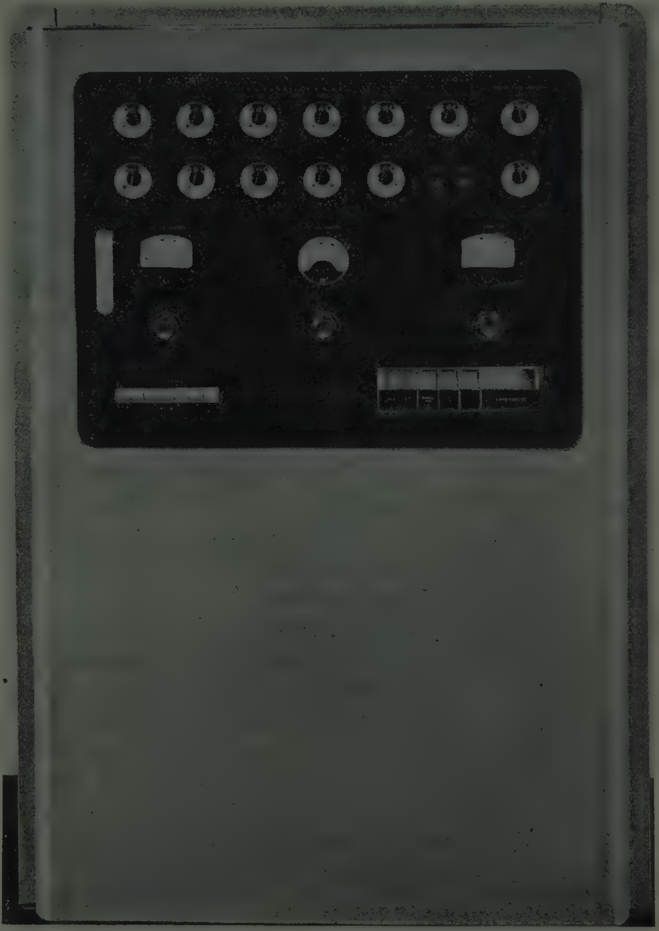


Fig. 16—Power distribution unit.

CONSTRUCTION AND DESIGN DETAILS

The calculator was designed and built on a unitized basis to facilitate the production, testing, shipping and installation operations. The dimensions of all units have been restricted so that every unit can be moved easily through conventional doorways and elevators and can be transported with normal trucking or aircraft facilities.

The unitized construction was also extremely helpful during the initial testing phase of the project. Individual test units were constructed for the Electrostatic Storage Unit, the Magnetic Tape Units, and the Drum Unit. A combined test unit was also constructed for the Card Reader, the Card Recorder and the Printer. These test units enabled engineering groups to work independently on all units. This speeded the testing operation and further assured a maximum degree of success when the units were initially coupled as a calculator.

The design of the calculator falls more or less naturally into two broad areas, the system planning and the engineering design, although obviously each was modified by the other. Of particular value to the circuit design engineers was an Operators Manual outlining the logical system. This manual was completed before circuit work was begin. In other words, before circuit work was started a manual was prepared describing in detail how the calculator was to operate when completed. The circuit designers therefore had well defined goals.

The engineering design was started by selecting carefully considered service voltages and tube types to be used, as well as developing a standard circuit philosophy. The latter was supplemented by development of particular circuit elements such as a high-speed trigger, grounded grid amplifiers and cathode followers. A Circuit Design Manual was prepared for the use of all engineers doing design so that all circuits developed would be compatible.

For instance, the signal level used throughout the calculator is +10 to −30 volts and all panel wiring and cables are driven by cathode followers. Circuits are constructed in 8-tube pluggable units such as those shown in Fig. 17. Signal levels within the unit may be at a high or low impedance level, but all signals leaving a unit via panel wiring must be at grid level +10 to −30 volts and cathode follower driven.

The calculator contains approximately 4000 tubes and 13,000 germanium diodes. Approximately 60 per cent are 5965 twin triodes and 15 per cent are 5687 twin triodes. The distribution of the remaining 25 per cent is too great to describe here. The 5965 features a relatively large interelement spacing between grid and cathode and has very stable emission and cut-off characteristics with life. Originally intended for use in the 701, it is applied in a wide variety of circuit functions and has thus far demonstrated the required freedom from intermittent shorts and leakage normally encountered in long life applications of this type. On the basis of defective tubes analyzed from operations to date (5000 hours) a failure rate of 0.3 per cent per 1000 hours has been established. This figure is expected to materially reduce as additional machines increase the population under study.

Two classes of germanium diodes are used in the 701. Class A diodes, those having a back resistance greater than 400,000 ohms at 50 volts, are the primary switching circuit components. Class B diodes, those having a back resistance greater than 200,000 ohms at 50 volts, are used as protective clamping on the signal lines throughout the calculator. They are also used in switching circuits where the lower back resistance is satisfactory.

Protection is provided for the many diodes used in switching functions by means of +15 and −30 volt lines throughout the machine. These protective voltage lines are connected, through Class B clamping diodes, so as to limit the upper and lower voltage level of all cathode follower outputs. Since cathode followers are the only driving source for diode switching circuits, a maximum back voltage no greater than approximately 45 volts will ever exist across switching diodes should any combination of the dc power supplies fail.

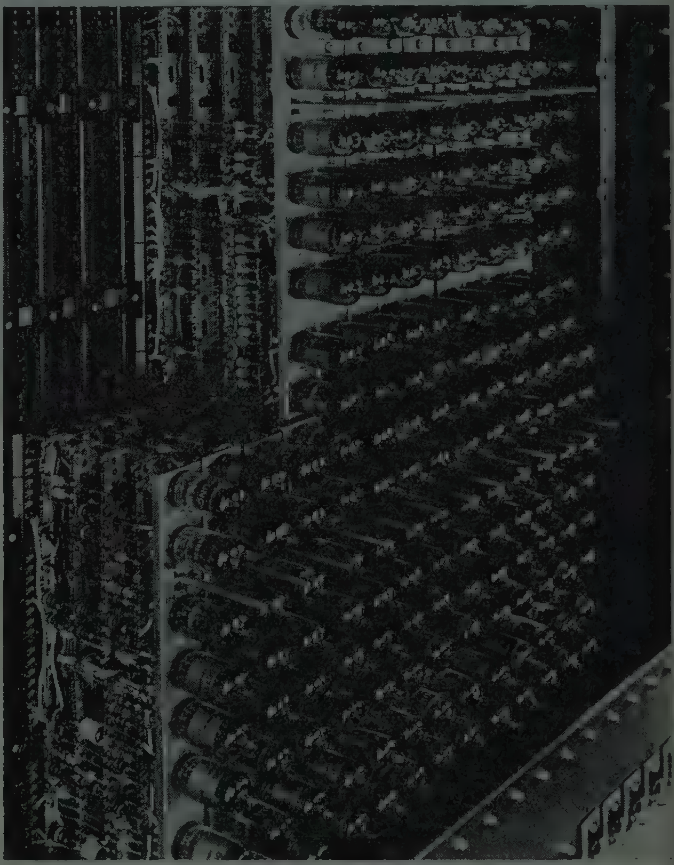


Fig. 17—Pluggable units.

This clamping action is required for only a short period of time since automatic voltage sensing through the use of plunger-type fuses and Sensitrols will immediately turn off all dc power. By means of this protection there has never been a loss of large quantities of switching diodes, as a result of their exposure to excessive back voltage.

All inter-frame cabling is laid in ducts beneath the floor. Signal cables are terminated in pluggable connectors and dc service cables are connected to screw-type terminal strips.

The machine is cooled by means of blowers located at the bottom of each gate or frame. The input air to these blowers must be maintained below 85°F by the use of air conditioning.

Machine Maintenance

The problem of maintaining a large-scale electronic calculator is one worthy of extensive planning. It is felt, by the engineers associated with this project, that regularly-scheduled preventive maintenance is the best approach to the problem at this time.

To facilitate the location of incipient troubles, the 701 has the following features:

(a) Direct coupling is generally used throughout, thus permitting static checking of signals.
(b) All dc power supplies may be varied approximately ±10 per cent for the purpose of marginal checking.
(c) The basic pulse repetition frequency (normally 1 mc) may be varied from 600 kc to 1.2 mc.
(d) The Machine Cycle key switch located on the Operator's Panel permits the execution of an instruction, one machine cycle (12-microsecond period) at a time. For example, the instruction *Multiply* would require 38 depressions of the Machine Cycle key switch and in doing so would permit analysis of the partial product as it is being developed.
(e) Facilities are also available to permit the high-speed repetitive execution of any instruction. This type of operation is extremely important when a timing problem or an intermittent condition exists.

In addition to the above, a large number of diagnostic programs[11] have been prepared which may be used to test thoroughly the performance of selective portions of the 701 system. Errors that occur during these tests are recognized by means of the program and reported to the engineer by means of lights, punched cards or printed results. Sufficient data may be stored and printed at a high rate of speed to permit an easy analysis of the difficulty.

A complete set of manuals (16) have been prepared covering the installation, operation, programming and maintenance of the calculator.

Conclusions

The IBM 701 is a large-scale, high-speed, electronic digital computer that is adaptable to a wide variety of problems. It incorporates the latest development in three principal types of storage and provides sufficient storage capacity to accommodate the many complex problems existing today.

A versatile input-output system using magnetic tapes, magnetic drums, the proven punched card and a line-at-a-time Printer, provides rapid communication between the machine and the operator. These features make possible the efficient use of a high-speed computer on problems containing large quantities of input data and resulting in many pages of printed results.

Acknowledgments

The Type 701 was developed at the IBM Engineering Laboratory, Poughkeepsie, N. Y. by groups under the direction of N. Rochester and J. A. Haddad.

The author wishes to acknowledge the assistance rendered by his associates in the preparation of this paper.

---

[11] L. R. Walters, "Diagnostic programming techniques for the IBM type 701 electronic data-processing machine," *IRE Convention Record;* 1953.

The Arithmetic Element of the IBM Type 701 Computer*

HAROLD D. ROSS, Jr.†, associate member, ire

Summary—**The arithmetic element of the IBM Type 701 Computer contains a number of innovations, both in circuits and in logic, which distinguish it from that used in other high-speed, parallel, binary computers. The most significant of these is the storage element used in the arithmetic registers, in place of the more usual flip-flop or trigger circuit. Use of this new element enables a number of simplifications to be introduced in the methods of executing instructions.**

Introduction

A NUMBER OF large-scale, parallel, binary digital computers are now in operation and the circuits and logic used in their arithmetic units include a variety of techniques. Most of these machines make use of the flip-flop or trigger circuit as the basic storage component in arithmetic registers and at least one uses a re-circulating pulse type of storage device.

A still different type of storage is employed in the arithmetic element of the IBM Type 701 Electronic Data Processing Machines and Associated Equipment, the large scale, high-speed, electronic computer installations now in production by the International Business Machines Corporation.[1,2] This dynamic type circuit has the property that its output level during each one-microsecond interval is the same as the input level during the previous one-microsecond period; that is, there is a one-microsecond delay through the unit. The output bears a marked resemblance to that of a flip-flop in that it is essentially a dc signal at one of two different levels. This circuit is used in conjunction with dc-coupled diode switching in order to achieve a number of simplifications in arithmetic processes.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 23, 1953; revised manuscript received July 23, 1953.

† International Business Machines Corp., Engineering Lab., Poughkeepsie, N. Y.

[1] C. E. Frizzell, "Engineering description of the IBM type 701 computer," Proc. I.R.E., pp. 1275–1287, this issue.

[2] W. Buchholz, "System design features of the IBM type 701 computer," Proc. I.R.E., pp. 1262–1275, this issue.

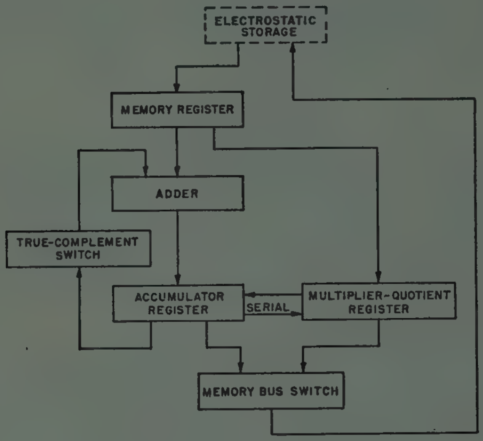


Fig. 1—Type 701 arithmetic element.

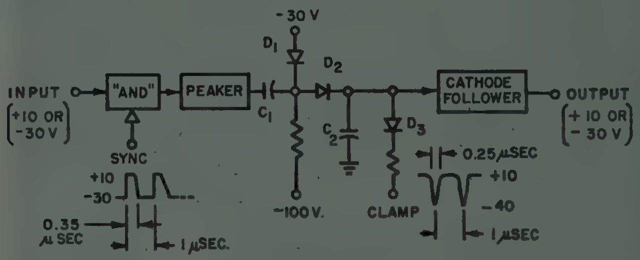
Arithmetic Element Block Diagram

A simplified block diagram of the arithmetic element appears in Fig. 1. In this diagram the major components are shown, with the paths of information flow during execution of an operation. The characteristics of the several units which make up the arithmetic element are:

1. Memory register. In executing an instruction requiring a word from memory, the word first appears in this register. It is not capable of shifting.
2. Multiplier-quotient register. This register may be entered from the memory register directly, or from the accumulator register by shifting. On input-output operation it acts as a buffer register. It is capable of shifting to the left or right. It holds the multiplier during multiplication and receives the quotient during division.
3. Accumulator register. In such operations as addition, this register holds one of the two operands and is connected to the adder by true-complement switching. It is capable of shifting to the right or left, either alone or in conjunction with the multiplier-quotient register.
4. Adder. This unit is mainly a switching array in which the outputs of the accumulator and memory registers are added together and the sum fed back to the accumulator register. It is described more fully in a later section.
5. Memory bus switching. This unit contains the switches necessary to connect the output of either the accumulator or multiplier-quotient registers to the electrostatic storage unit in order to store a word. Either the entire contents or only the more significant half of each register may be stored.
6. True-complement switching. This consists of an inverter and switching for each column of the accumulator register to permit either the true or inverted accumulator register output, or neither, to be connected to the adder unit.

Microsecond Delay Unit

The three arithmetic registers make use of a new storage unit called the microsecond delay unit. This circuit stores binary information in a dynamic fashion but its output appears as substantially a dc level of either +10 or −30 v, depending upon the binary digit stored. When suitable input switching is provided, information may be entered from one of several sources, such as another register or from the adjacent columns of the same register. When new information is not being entered, the status of the unit is maintained by an external feedback connection from its output to its input. As used in the 701, the output does not assume the new level until one microsecond after the input signal is applied.



(a) BLOCK DIAGRAM

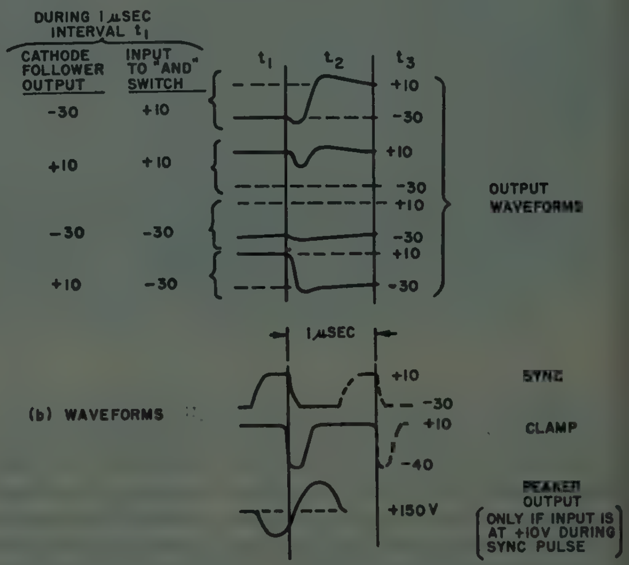


Fig. 2—Microsecond delay unit.

A simplified diagram illustrating the operation of this circuit is shown in Fig. 2a (a schematic diagram of the delay unit is given in Fig. 12). To facilitate understanding the operation of the circuit it is divided into four parts which are (1) an "and" switch in which the level of the input signal, either +10 or −30 v, is sampled by a sync pulse of about 0.35 μsec duration; (2) a vacuum tube peaker circuit driven by the "and" switch; (3) a capacitor (and associated circuits) which stores the pulse energy from the peaker circuit for one μsec; (4) an output cathode follower driven by the capacitor.

Circuit Operation

In describing the operation of this circuit, there are four possible conditions to consider. These possibilities are listed in Fig. 2b. It should be pointed out here that the output continues unchanged until one μsec after the new input is applied, hence the table of Fig. 2b shows the various combinations of input and output that may be present simultaneously. Considering the first of these conditions, the input signal during t_1 is at +10 v and is applied to the diode "and" switch together with the sync pulse. Under these conditions, the sync pulse is gated through to the peaker tube which will conduct for the duration of the pulse. At this time a negative pulse will be coupled over to the junction of C_1, D_1 and D_2 but will go no farther because D_1 will conduct, holding this point to −30 volts. After the peaker tube is cut off, a positive pulse will be produced, of about 0.5 μsec duration, which will be coupled to the storage capacitor C_2 via C_1, D_1, and D_2. Since the output of the unit was assumed to be −30 v, this was the charge on C_2 (consideration of how this is done will be postponed momentarily). The positive pulse from the peaker charges C_2 to +10 v. The upper level is limited by conduction of D_3 when the normal +10 v upper level of the clamp signal line is exceeded. The voltage across C_2 is directly coupled to the output cathode follower stage. Fig. 2b shows the waveforms mentioned above.

The process just described began with the output of the unit being a −30 v level; consider now the process when the output is initially +10 v. An input level of +10 v will again gate the sync pulse through to the peaker tube, causing it to conduct and generate a negative pulse followed by a positive one. Once again the latter pulse proceeds via C_1, D_1 and D_2 to charge C_2 to +10 v. In the present case C_2 was already charged to +10 (except for leakage through the back resistance of D_3). The +10 v charge is renewed and the output simply continues at +10 v with this reservation: occurrence of the clamp pulse causes partial discharge of C_2, coming as it does during the initial portion of the positive peaker output pulse. Since the peaker output is of longer duration than the clamp, in the end it prevails and charges C_2 to +10 v as shown in Fig. 2b.

Both of the above descriptions assumed an input signal level of +10 v at the time the sync pulse occurred. Consider now the action if the input level is −30 v; coincidence will not occur in the "and" switch and the peaker tube will not conduct, consequently no charging pulse will be generated. If the charge on C_2 had previously been −30 v, it might have leaked off to some extent, through the back resistance of D_3 to the +10 upper level of the "clamp" signal. Fall of the clamp to −40 v will restore the charge. If, on the other hand, C_2 had previously been charged to +10 v by the process described, and no positive charging pulse is generated by the peaker, the clamp pulse will return the charge on C_2 to −30 v. These processes are illustrated by the last two output wave forms of Fig. 2b.

The delay feature is thus due partly to the action of the peaker circuit and partly to the storage capacitor, C_2. The usefulness of this delay is that the 0.6 μsec period while the sync pulse is at −30 v may be used to switch the input of the unit between several sources, one of which is ordinarily the output of the delay unit itself. When the unit is so connected, it maintains its dc signal level at either +10 or −30 v until this connection is interrupted and a new source connected to the unit. This connection is made for one μsec, following which the delay unit input is connected back to its output in order to retain the new information. The only requirement in switching the delay unit input is that the new input signal must have reached its final dc level by the time the sync pulse appears.

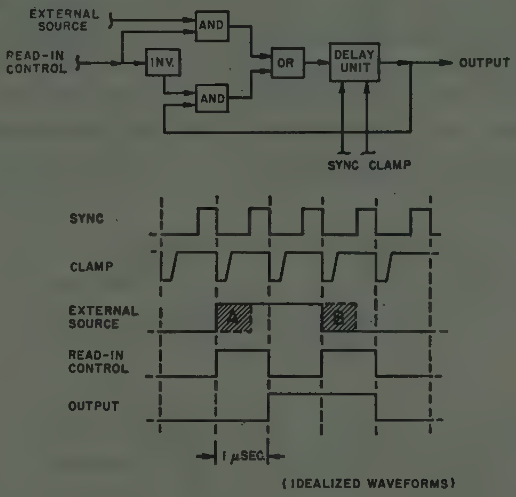


Fig. 3—Delay unit input switching.

Input Switching Associated with the Delay Unit

Fig. 3 shows a simple block diagram of a delay unit with the switching required to maintain continuously a +10 or −30 v level or to enter new information from an external source. Normally the "read-in" control line is at −30 v. When it is desired to enter new information into the delay unit this line is raised to +10 v for one μsec. Since the read-in line is normally at −30 v, the inverter output is normally +10 v, the lower "and" switch is conditioned and the delay unit output is connected to its input. Pulsing the read-in line for one μsec conditions the upper "and" switch and de-conditions the lower, effectively breaking the connection from the delay unit output. As the result of this one-microsecond "look" at the external source, the unit assumes the status of that source and at the end of the read-in signal, goes back to reading its own output. The occurrence of the read-in pulse is suitably timed with respect to the sync and clamp pulses as shown in Fig. 3. In this figure, the delay unit initially stored a −30 v level (corresponding to a binary zero). The first read-in pulse caused the unit to store a +10 v level (corresponding to a one). Two μsec later a second read-in pulse occurred. At this time the external source presented a −30 v level and hence a zero was stored by the delay unit.

Another function performed by the action of the delay unit is that of re-timing; this is indicated by the shaded areas of the external source waveforms in Fig. 3. The shaded area *A* indicates that the rise of the waveform may occur anywhere within this interval and still give the output change at the time shown. Similarly, area *B* indicates that the fall of the waveform may take place anywhere within this interval and yet give correct operation. The re-timing is due to the fact that the input waveform is sampled by the sync pulse and effectively compensates for the effect of small accumulated delays.

Delay Unit Shifting Registers

If the "external source" for the circuit shown in Fig. 3 was the output of the adjacent delay unit of a register, a shifting register would result. A simple shifting register or ring, having no input switching, is shown in Fig. 4 with actual waveforms at several points. A pattern of two ones and a zero is shown, with the displacement of the pattern at successive stages by one microsecond, being evident.

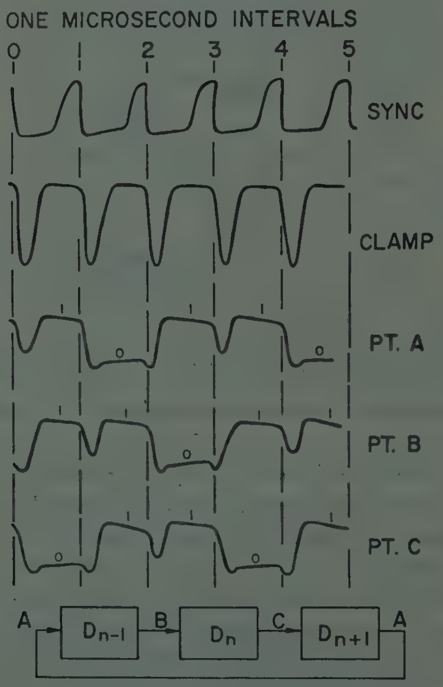


Fig. 4—Waveforms in a delay unit ring.

Fig. 5 shows three columns of a register, capable of shifting to the right or left as well as holding information statically. Each column consists of a delay unit with a three-way switch enabling it to read the output of the unit to the left, read its own output or that of the unit to the right. The function to be performed depends on the condition of the "shift right" and "shift left" control lines at the bottom. Normally these lines are at −30 v, de-conditioning the left and right "and" switch in each column. However, the center "and" switch is conditioned by way of the two-input "or" switch and inverter at the lower left. The output of this circuit is called the "hold" control line, since it conditions the center "and" switches which cause each delay unit to "hold" their status for an indefinite period. Shifting to the left by one column occurs if the "shift left" control line is pulsed to +10 v for one μsec at the proper time with respect to the sync and clamp pulses, in the same manner as the read-in control in Fig. 3. Pulsing either shift control line will cause the "hold" control line to go negative for the same period. A two μsec pulse will cause a shift of two places, and so on.

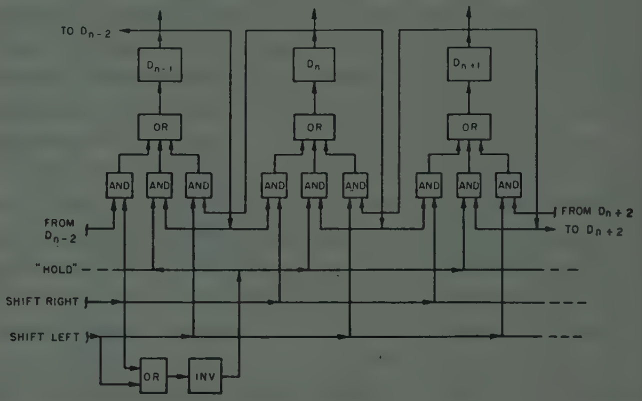
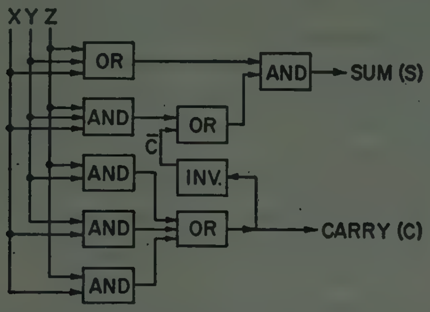


Fig. 5—Shifting register switching.

The circuit shown in Fig. 5, with up to six different inputs per column, forms the basis of the arithmetic registers used in the 701. It is felt that a high order of reliability, logical flexibility and freedom from close timing conditions has resulted from its use. Some of these points will be discussed further in the sections to follow.

PARALLEL BINARY ADDER

The means for performing addition in the 701 makes use of logical adders which are passive diode switching circuits of the type shown in Fig. 6. Also shown there is the "truth table" for this circuit. In both the circuit and the table *X*, *Y*, and *Z* are the three inputs, representing one digit each of the addend and augend, together with the carry to the next more significant column. The outputs are of course the sum and the carry from the next less significant column. From examination of the truth table it is evident that a carry is generated whenever there are signals present on two or more inputs and this fact is set forth in Boolean notation by the first logical equation. Further examination shows that a sum of one will be produced under two conditions: if there are signals present at all three inputs and if there is a signal present at one and only one input. This second condition may be re-phrased as follows: a sum of one will occur if there is a signal present at at least one of the inputs provided there is no carry output generated. This will also be evident from examination of the table. This last condition is exemplified by second Boolean equation in Fig. 6. Having these expressions for sum and carry, circuit follows at once.


XYZ
OR
AND
SUM (S)
AND
OR
C̄
AND
INV.
AND
OR
CARRY (C)
AND

(a) LOGICAL ADDER

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$C = XY + YZ + XZ$$

$$S = (X+Y+Z)(XYZ+\bar{C})$$

(b) "TRUTH TABLE"

Fig. 6—Three-input binary adder.

It should be mentioned that the circuit as shown in Fig. 6 contains logical elements only; cathode followers required to drive the diode circuits have been omitted. As a result of including the necessary cathode followers a loss in signal amplitude is encountered resulting in a rise in the lower level of the carry signal of about three volts per follower. It thereby becomes necessary to introduce means for restoration of signal amplitudes and these means, which involve over-driven stages, introduce delays into the circuit operation.

Inasmuch as the 701 performs addition in parallel upon 37 columns (35 bits plus two accumulator overflow positions) the delay mentioned above accumulates so that for a full length carry about 3.5 μsec are required. Actually about five μsec are allowed for this process. Since facilities for addition, but not subtraction, are built into the computer, provision must be made to complement one of the operands in order to carry out the latter operation. Complementing is performed on but one of the two factors, namely the one from the accumulator register and a simple diode switch and inverter are required in each column to connect the adder to the accumulator register contents either as a true or a complement number.

Logical Aspects of the Operation "ADD"

In the 701 all numbers are represented as magnitudes with signs. Furthermore, means are provided to obtain the complement of only the accumulator register contents in subtraction, it having been determined that the occurrence of zeros of either sign was not only acceptable but desirable. Fig. 7 contains examples to illustrate the rules by which the form of the result of an arithmetic subtraction is determined. In case 1, the ones' complement of a positive number in the accumulator register is added to a larger negative number in the memory register. An end-around carry results, indicating that the result is in true form and that the sign of the accumulator register must change. In case 2, the magnitudes are reversed and the absence of an end carry indicates a result in ones' complement form and that the accumulator register sign will not change. In order to put the result into true form, a re-complementing process is undergone. Cases 3 and 4 are similar except that, since the magnitudes of the factors are alike, the result will be zero in each case. Here, the sign of the zero result is the initial sign of the accumulator register.

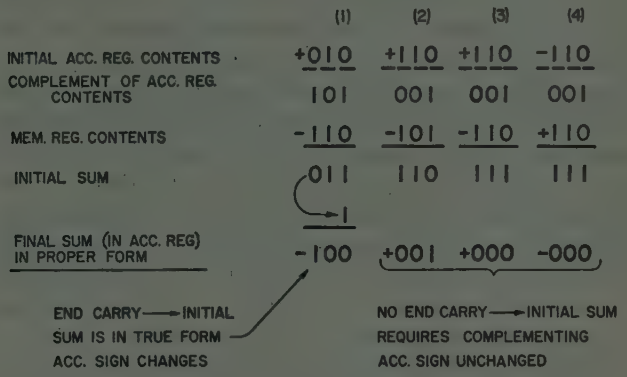

(1)
(2)
(3)
(4)
INITIAL ACC. REG. CONTENTS
+010
+110
+110
-110
COMPLEMENT OF ACC. REG. CONTENTS
101
001
001
001
MEM. REG. CONTENTS
-110
-101
-110
+110
INITIAL SUM
011
110
111
111
1
FINAL SUM (IN ACC. REG) IN PROPER FORM
-100
+001
+000
-000
END CARRY—→INITIAL SUM IS IN TRUE FORM ACC. SIGN CHANGES
NO END CARRY—→INITIAL SUM REQUIRES COMPLEMENTING ACC. SIGN UNCHANGED

Fig. 7—Examples of ones' complement arithmetic when only accumulator operand can be complemented.

The ones' complement system, while causing a certain inconvenience in having to deal with end-around carries, makes the re-complementing process less painful, in that no carries are produced. The twos' complement system would have required allotting time for possible lengthy carries in re-complementing, as illustrated in Fig. 8. In other words, re-complementing in the ones' complement system consists simply of inversion, a process requiring little time, whereas in the twos' complement system a complete addition is involved. The table in Fig. 9 summarizes the situations that may arise in adding two numbers of varying sign and magnitude.

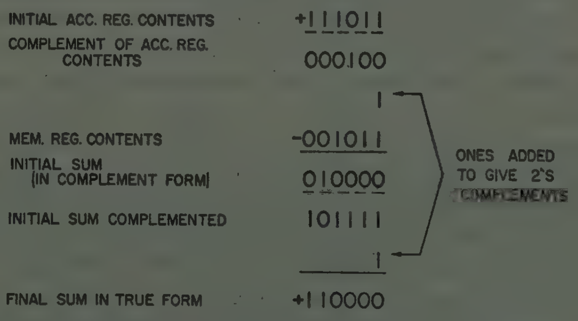

INITIAL ACC. REG. CONTENTS
+111011
COMPLEMENT OF ACC. REG. CONTENTS
000100
1
MEM. REG. CONTENTS
-001011
INITIAL SUM (IN COMPLEMENT FORM)
010000
INITIAL SUM COMPLEMENTED
101111
1
FINAL SUM IN TRUE FORM
+110000
ONES ADDED TO GIVE 2'S COMPLEMENTS

Fig. 8—Example showing occurrence of long carry in changing a twos' complement sum to a true number.

SIGN OF FACTOR IN ACCUMULATOR	SIGN OF FACTOR IN MEMORY	RELATIVE MAGNITUDES	FORM OF INITIAL SUM	IS RECOMPLEMENTING REQUIRED?	SIGN OF FINAL, TRUE SUM
+	+	——	TRUE	——	+
−	−	——	TRUE	——	−
−	+	$\|M\| > \|A\|$	TRUE	NO	+
−	+	$\|M\| < \|A\|$	COMPL.	YES	−
−	+	$\|M\| = \|A\|$	COMPL.	YES	−
+	−	$\|M\| > \|A\|$	TRUE	NO	−
+	−	$\|M\| < \|A\|$	COMPL.	YES	+
+	−	$\|M\| = \|A\|$	COMPL.	YES	+

Fig. 9—Logic of sum generation and addition.

Control and Timing of the Operation "ADD"

The timing of the various commands necessary for the execution of the operation ADD is illustrated in Fig. 10. Execution of any operation begins when the output of the operation decoder assumes its new value, near the end of an *"I"* (Instruction) cycle. In this particular case, the output was the one signifying the operation ADD, hence an *"E"* (Execution) cycle is desired next. An *E* cycle is required whenever a reference to memory is needed, either to store a number or to withdraw one from memory. After nine microseconds, the word from memory is available to be entered into the memory register. There being insufficient time remaining in the cycle for the commands yet to come, an *"E/R"* (Execution/Regeneration) cycle is next called for. In this cycle, two full words of the electrostatic memory are regenerated while the actual addition is done. Addition begins by connecting the memory register to the adder and the accumulator register to the adder in true or complement form as required. After five μsec, the output of the adder is sampled and set into the accumulator register in place of the operand originally there. Depending on the relative magnitudes and signs of the operands, the result at this point may be in complement form as described in the preceding section. If so, the complement of the new accumulator register contents is connected to the adder for two μsec; the other adder input is left disconnected and represents a row of 35 zeros. After one μsec the new adder output is sampled and the result, now in true form, returned to the accumulator register. Finally, the sign of the accumulator register is set, according to the table in Fig. 9, and a signal sent out indicating the execution of the operation is complete. This last pulse also advanced the program counter one step in preparation for obtaining the next instruction. Following the *E/R* cycle, two *"R"* (regeneration only) cycles may be called for to satisfy the regeneration requirements of electrostatic memory.

For different operations, the sequence of cycles will vary, depending upon the need for a reference to memory, and upon the amount of time needed for manipulation of words by adding, shifting, and so on.

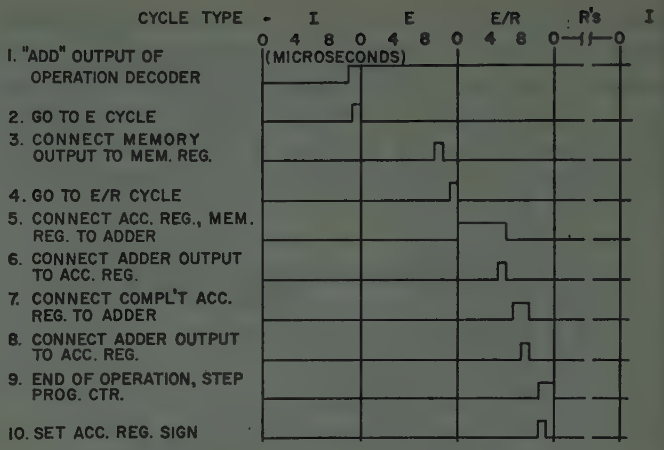

CYCLE TYPE - I E E/R R's I
0 4 8 0 4 8 0 4 8 0 0
(MICROSECONDS)
1. "ADD" OUTPUT OF OPERATION DECODER
2. GO TO E CYCLE
3. CONNECT MEMORY OUTPUT TO MEM. REG.
4. GO TO E/R CYCLE
5. CONNECT ACC. REG., MEM. REG. TO ADDER
6. CONNECT ADDER OUTPUT TO ACC. REG.
7. CONNECT COMPL'T ACC. REG. TO ADDER
8. CONNECT ADDER OUTPUT TO ACC. REG.
9. END OF OPERATION, STEP PROG. CTR.
10. SET ACC. REG. SIGN

Fig. 10—Timing for the operation "ADD."

The arithmetic speed is limited by timing requirements of electrostatic storage rather than by arithmetic circuits themselves. Advantage was taken of this where possible to avoid using faster, more elaborate circuits.

The Control of Shifting

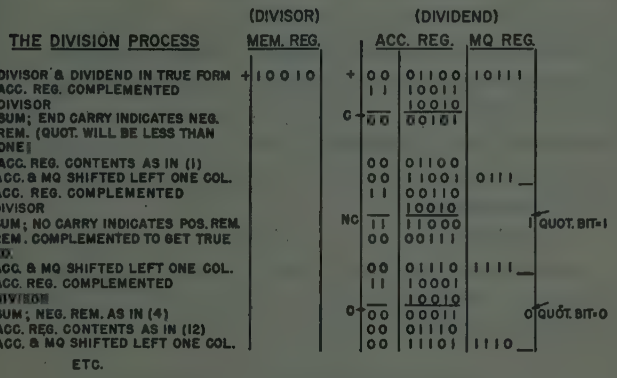
The number of places by which the contents of the accumulator register or the combined accumulator and multiplier quotient registers are to be shifted, is controlled by a counter into which the address part of the shift instruction is entered. As shifting proceeds, pulses are sent to this counter, causing it to count down in synchronism with the shifting process. When the contents of the counter reach zero, this fact is sensed by an "and" switch and the shift gate to the registers involved is terminated. Shifting takes place at a one megacycle rate and up to eight places may be traversed within a 12 μsec cycle. A variable number of cycles is required for the execution of a shift depending upon the length of the shift. The maximum length of a shift is 255 places; such a shift, while resulting in a string of zeros in the registers affected, facilitates the programming of floating-point computations.

Multiplication

Multiplication in the 701 consists of repeated addition and shifting, the addition being under control of the currently least significant multiplier digit. Thirty-six successive 12-μsec *E/R* cycles are required for the 35×35 multiplication, following the *I* and *E* cycles used to obtain the instruction itself and the multiplicand. During each *E/R* cycle one addition of the multiplicand may occur together with a shift of the accumulator and *MQ* registers to the right. These functions require but little more than half the 12 μsec allotted; the actual time taken for multiplication might have been reduced by packing the successive additions closer together but in practice as the additional time is used to regenerate the electrostatic storage, the time expended is recouped in that succeeding instructions may be executed in less time. By using the 12-μsec ADD-type *E/R* cycle, control of multiplication is simplified.

DIVISION

One of the consequences of the use of dc coupled diode adders and delay unit registers is that division becomes somewhat simpler than would otherwise be the case. A system which is superior to either the restoring or nonrestoring scheme is used; it is made possible by the ability to examine the result of a subtraction before discarding the original number. Thus, if the result of a subtraction is an overdraw, this result may be ignored (that is, not put into the accumulator register) and the previous remainder retained and shifted left, whereupon another subtraction may be tried. If the subtraction resulted in a remainder of unaltered sign, the result will be in complement form and must be complemented prior to shifting left. In the former case a quotient digit of zero is inserted into the lowest order multiplier-quotient register column prior to shifting and in the latter case a quotient digit of one is inserted. This is repeated in successive cycles, so that the quotient builds up in the *MQ* register on the right as the less significant part of the dividend is shifted out into the accumulator register on the left.



THE DIVISION PROCESS	(DIVISOR) MEM. REG.		(DIVIDEND) ACC. REG.		MQ REG.	
1. DIVISOR & DIVIDEND IN TRUE FORM	+10010	+	00	01100	10111	
2. ACC. REG. COMPLEMENTED			11	10011		
3. DIVISOR				10010		
4. SUM; END CARRY INDICATES NEG. REM. (QUOT. WILL BE LESS THAN ONE)		C	00	00101		
5. ACC. REG. CONTENTS AS IN (1)			00	01100		
6. ACC. & MQ SHIFTED LEFT ONE COL.			00	11001	0111_	
7. ACC. REG. COMPLEMENTED			11	00110		
8. DIVISOR				10010		
9. SUM; NO CARRY INDICATES POS. REM.		NC	11	11000	1	QUOT. BIT=1
10. REM. COMPLEMENTED TO GET TRUE NO.			00	00111		
11. ACC. & MQ SHIFTED LEFT ONE COL.			00	01110	1111_	
12. ACC. REG. COMPLEMENTED			11	10001		
13. DIVISOR				10010		
14. SUM; NEG. REM. AS IN (4)		C	00	00011	0	QUOT. BIT=0
15. ACC. REG. CONTENTS AS IN (12)			00	01110		
16. ACC. & MQ SHIFTED LEFT ONE COL.			00	11101	1110_	
ETC.						

Fig. 11—The division process.

The process just described is illustrated in Fig. 11. Here a typical division is shown using abbreviated binary numbers of five-bit length (the signs are handled separately). The repeated subtraction cycle is shown for two different cases in steps 6–10 and 11–15. In the first case the result of subtraction was a positive remainder; this fact is indicated by the absence of an end carry which therefore causes the adder output to be inserted back into the accumulator register. In the second case a carry appeared and so the adder output was ignored, the previous remainder shifted to the left, and a new subtraction started, thus it is seen that no restoration is necessary. A further point is illustrated by the example: namely, the method of testing for a quotient less than one. The first four lines illustrate this; the divisor is subtracted from the dividend with no preliminary shift. An end carry in this process indicates an overdraw and consequently a quotient of less than one. If no carry were obtained, an alarm would be generated and calculation stopped. In making this test the end carry is the only result desired, the sum is not put in the accumulator register. Actual division then begins with a shift to the left of the original accumulator register contents together with the *MQ* register.

The complementing cycle mentioned above, which is required when subtraction did not cause a sign change, could have been avoided by use of additional switching but there was little to be gained by the increase in speed, as ADD-type cycles of the sort described previously are made use of here without change in timing. Thus 36 cycles are required for the complete operation, resulting in a surplus of regeneration for the electrostatic memory. This surplus usually enables some regeneration to be dispensed with in the operations immediately following so that a portion of the time spent in dividing is usually made up elsewhere.

TESTING FOR ZERO IN THE ACCUMULATOR

The incorporation of the operation "Transfer on Zero" requires a method for detecting whether the accumulator register contains zero. The contents of the accumulator register are to be unchanged as a result of this test and this requirement is easily complied with by the scheme described below. Once again, the use of delay units in the accumulator register simplifies the process.

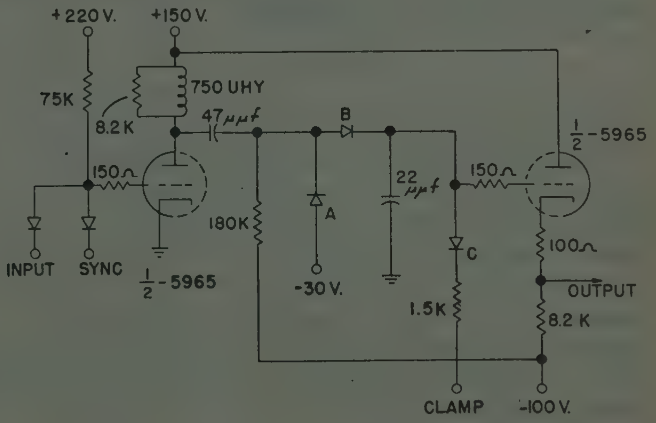


Fig. 12—The delay unit circuit.

The process consists of adding the complement of the accumulator register contents, to zero (obtained by leaving the memory register disconnected from the adder) and adding one in the lowest order. If the contents were initially zero, a full length carry will result, giving a carry from the highest order. This carry is used to cause the next instruction to be taken from the address specified in the Transfer on Zero instruction. The adder output is not set into the accumulator and hence the contents are undisturbed. This ability to examine the adder output without putting it into the accumulator register is facilitated by the one-microsecond delay in the delay units and the use of dc coupled diode adders.

CONCLUSION

The arithmetic element of the IBM Type 701 Computer makes use of a new electronic storage circuit, the microsecond delay unit, whose output may be either of two dc levels, yet uses dynamic pulse storage techniques. Through the use of this device, in conjunction with dc coupled diode adding circuits, important simplifications are realized in shifting registers, and in the execution of division and testing for zero in the accumulator.

ACKNOWLEDGMENT

The microsecond delay unit described herein was developed by B. L. Havens of the Watson Scientific Computing Laboratory. His support, encouragement, and assistance contributed greatly to the success of the 701 project and his kind permission to describe this unit is greatly appreciated by the author. The author also acknowledges the valuable assistance of other members of the project in the preparation of this paper.

The SWAC-Design Features and Operating Experience*

H. D. HUSKEY†‡, ASSOCIATE, IRE, R. THORENSEN†, ASSOCIATE, IRE, B. F. AMBROSIO†, ASSOCIATE, IRE, AND E. C. YOWELL†

Summary—**The SWAC is an ultra-high-speed digital computer utilizing a Williams tube memory, an auxiliary magnetic drum memory and a punched card input-output system. A general description of the functional organization of the computer is given together with a brief discussion of the various commands and how they are executed.**

Some of the special engineering features of the computer are described, in particular those relating to the electrostatic and magnetic drum memories.

Finally a short survey of the types of problems solved by the computer during the last year is presented.

INTRODUCTION

THE NATIONAL BUREAU OF STANDARDS Western Automatic Computer (SWAC), located in Los Angeles at the Institute for Numerical Analysis of the National Bureau of Standards, is a digital computer utilizing a Williams tube memory,[1] an auxiliary memory in the form of a magnetic drum,[2,3] and a punched card input-output system. A primary feature of the SWAC is its high speed, which, for handling the binary equivalent of eleven decimal digit numbers, is greater than that of any other computer now in operation.

The SWAC stores in its high-speed memory the numbers involved in the computation and also all the instructions necessary to perform the calculation. This makes it possible for the calculator to utilize fully the speed of the Williams tube memory, doing complete arithmetic operations in a few microseconds. Instead of handling numbers as a train of pulses, there are parallel circuits in the SWAC which transfer numbers almost instantly (actually the transfer takes place in the width of a pulse which in some cases is one-tenth μsec). This transferring of numbers in parallel makes it possible to do computations at many times the speed of serial computers (for example, acoustic delay-line machines) without having excessively high pulse rates on the lines of the computer.

The SWAC is the first of the Williams tube computers to be completed in this country. At present it is producing useful results during seventy per cent of the time that its power is turned on.

BRIEF DESCRIPTION OF THE SWAC

The Williams tube memory in the SWAC stores 256 words (numbers or instructions). The various digits of a particular number are stored in corresponding positions on each of 37 cathode-ray tubes. A word in SWAC is 37 binary digits long, which is the equivalent of about 11 decimal digits. A Williams tube memory requires regeneration. To accomplish this, time is divided into 8-μsec intervals. During one of these intervals a particular number in the memory may be regenerated, read out into the arithmetic unit, or replaced with a new number. The regeneration takes place during alternate 8-μsec intervals with the whole memory being regenerated once each 4,096 μsec. The other 8-μsec periods are called action intervals, and it is during these periods that numbers may be transferred between the memory and the arithmetic unit.

The SWAC uses eight basic commands: add, subtract, multiply (rounded-off answer), product (two word answer), compare, extract, input, and output. The compare command has a variation which compares absolute values. There is a special form of input used for initially inserting the information into the computer. Normally the source of the next command is an address in the memory which is specified by the command counter in the control circuits, but three of the commands—add, subtract, and multiply—have variations consisting of special four address forms wherein the source of the next command is specified by the fourth address. In normal add and subtract commands, the fourth address specifies the source of the next command only if the operation overflows. The command system used in the SWAC is called a modified four address system.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 8, 1953; The preparation of this paper was sponsored (in part) by the Office of Scientific Research, U. S. Air Force.

† National Bureau of Standards, Los Angeles.

‡ Wayne University, Detroit, Michigan.

[1] F. C. Williams, and T. Kilburn, "A storage system for use with binary digital computing machines," *Proc. IEE*, Part III, pp. 81–100; March, 1949.

[2] R. Thorensen, "Design Features of a Magnetic Drum Memory for the National Bureau of Standards Western Automatic Computer (SWAC)," *Proc. Electronic Computer Symposium;* April 30, May 1–2, 1952, Los Angeles, Calif.

[3] A. A. Cohen, "Magnetic Drum Storage for Digital Information Processing Systems," Mathematical Tables and Other Aids to Computation, vol. IV, No. 29, pp. 31–39; January, 1950.

The execution of each command involves (except in the case of input and output) at least four references to the memory. Since one reference can be made during each action period, it is seen that the minimum time for the execution of a command is 64 μsec, and in fact, the computer executes any arbitrary sequence of addition, subtraction, and compare commands at the rate of about 16,000 complete operations per second.

To see what happens in the 64 μsec that are required to execute one of these commands, consider an addition command. In the *first* action period, the first operand is found in the memory and transferred to the arithmetic register where it is complemented with respect to 2^{37} if it is negative. During the *second* action period, the second operand is found, complemented if negative, added to the number in the arithmetic register, and if the result is negative it is complemented, so that, in the *third* action period the answer can be placed back in the memory. In the *fourth* action period, the next command is found in the memory and transferred to the command register in preparation for the next following step in the computation.

The only event that takes a substantial amount of time in the above operation is the actual addition process. Here time must be allowed for the carry to propagate through the thirty-seven binary positions of the numbers. This carry (and the no-carry which may occur after a complementation) propagates in approximately 3 μsec, but for safety, a time of 5 μsec is allowed.

The multiply command which produces a rounded-off answer also requires four accesses to the memory. The actual multiplication is performed as thirty-six shifts and possible additions, each taking a total of 8 μsec per addition and shift. Thus, a multiply command actually needs a minimum of 64 plus 288 μsec. However, for purposes of simplicity in the control circuitry, each command must take a multiple of 64 μsec, making a multiply command require 384 μsec. A product command produces a double-length answer, and thus requires five accesses to the memory, but it, too, takes only 384 μsec.

The so-called extract command is actually a combination of two processes: (a) the selection of any specified set of the 36 binary digits of a number, and (b) the shifting of the result a specified amount to the right or the left. This command has many logical applications and is used, for example, to store two or more numbers in one memory location, to increase the effective capacity of the memory, or to operate in a "floating point" number system. The execution time for this command depends upon the amount of shift involved and takes from 128 to 384 μsec.

The simple compare command is a special sort of subtraction command in which the sign of the difference determines whether the SWAC shall proceed to the next command or shall obey another specified command instead. This useful command is executed in 64 μsec.

The input and output commands control the transfer of information between the high-speed memory and the input and output typewriters, the tape reader and tape punch (Flexowriter), the punched-card reader (collator) and the card punch (summary punch), and the magnetic drum. The typewriters and tape equipment accept and transmit data one base-sixteen digit at a time, operating at about eight characters per second.

For card input, twenty numbers may be placed on a standard eighty column card as binary punches with two numbers on each row of the card. This still leaves room for a serial or problem number on the cards for identification purposes. One command places the two numbers from one row on the card in any two addresses in the high-speed memory. In a similar fashion, one command can cause two numbers to be punched on one row of a card in the card punch. Once a card is started in either the collator or the punch, all ten rows must be handled in order. However, several milliseconds elapse between any two rows on the card so that actual computing (like binary-to-decimal conversion) may be done in the interim.

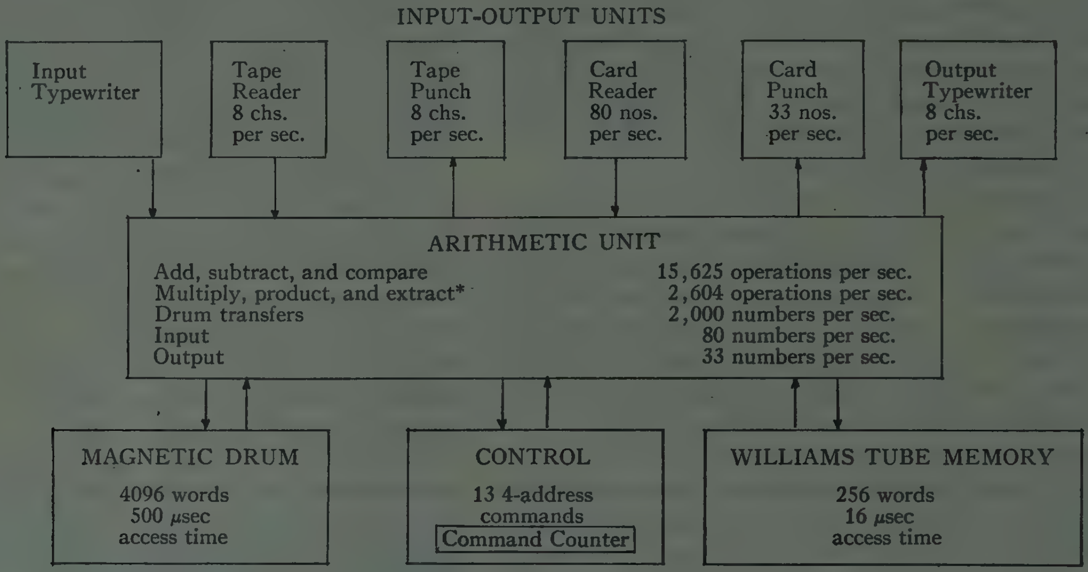
The transfers to and from the drum are most efficiently handled in blocks of thirty-two words, which is precisely the number of words on any one track of the drum. A word in position P of track T on the drum is transferred into address $A+P$ in the high-speed memory where A and T are specified in the command. This makes it possible to begin the transfer with the first number that becomes available, and to know that the transfer persists for precisely one revolution time of the drum. The drum rotates at 3,600 revolutions per minute; so thirty-two words are transferred in approximately 17,000 μsec. Since there is no wait time, the access time per word on the drum (when handled in blocks of thirty-two words) is about 500 μsec.

Under some circumstances it may be desirable to transfer less than thirty-two words at a time, to or from the magnetic-drum memory. The drum-transfer command has therefore been made flexible enough to allow also for block transfers of sixteen words and eight words. In these cases the specific portion of the track to be transferred is also specified in the command. The time required, however, for a block transfer of 8 words is the same as that required for a block transfer of 32 words, or just one revolution of the drum. Therefore whenever possible, a block transfer of thirty-two words is used.

Thus, the SWAC has a 256 word high-speed memory with an access time of 16 μsec, and an auxiliary 4,096 word memory with an access time of 500 μsec.

The chart gives a summary of SWAC characteristics:

Crystal diode gating is used extensively in the arithmetic unit, and 6AS6 vacuum tube gates with crystal mixing are used elsewhere. The more recent drum circuits use 7AK7 gates.


INPUT-OUTPUT UNITS
Input Typewriter
Tape Reader 8 chs. per sec.
Tape Punch 8 chs. per sec.
Card Reader 80 nos. per sec.
Card Punch 33 nos. per sec.
Output Typewriter 8 chs. per sec.
ARITHMETIC UNIT
Add, subtract, and compare 15,625 operations per sec.
Multiply, product, and extract* 2,604 operations per sec.
Drum transfers 2,000 numbers per sec.
Input 80 numbers per sec.
Output 33 numbers per sec.
MAGNETIC DRUM
4096 words
500 μsec
access time
CONTROL
13 4-address commands
Command Counter
WILLIAMS TUBE MEMORY
256 words
16 μsec
access time

* Note: Up to 5,208 extract operations per second.

SPECIAL ENGINEERING FEATURES

The SWAC proper occupies a floor space of about 4 by 12 feet. The drum occupies a space of 2 by 7 feet. Figs. 1, 2 and 3 illustrate various units of the SWAC and associated equipment. There is an operating console on a standard office desk in addition to punched card and paper tape input-output units. All of the above units are located in a room 20 by 30 feet. The power-supply equipment comprises a regulated alternator, a set of selenium rectifier dc power supplies, and a control cabinet housing regulators, heater transformers and high-voltage power supplies. The power equipment occupies a total space of about 60 square feet.

A blower system moves about 4,800 cubic feet per minute of outside air through an air conditioner heat exchanger, through the computer, and back outside. The air conditioner cools the air to 40 degrees F., and reheats it to 60 degrees to control the humidity. The exhaust air is approximately 90 degrees F.

All the electronic components of the computer proper are mounted on removable plug-in chassis. As there are spares for almost all types of chassis used in the SWAC, it is rare that a fault cannot be cured by replacing a bad chassis with a good spare. Laboratory test equipment has been constructed so that faulty chassis can be repaired in the laboratory without use of computer time. The majority of the pluggable chassis carry, on the average, ten tubes each; however, the magnetic-drum circuits are built of much smaller units, usually of one tube each.

There are high- and low-speed flip-flops in the computer. The high-speed ones are based on circuitry developed at the Massachusetts Institute of Technology.

In all, there are about 2,600 tubes and 3,700 crystals in the SWAC system, and the power consumption is about 30 kw.

The SWAC is designed to work in a synchronous manner. That is, regeneration of the memory proceeds at a fixed rate determined by a crystal-controlled oscillator. The operations in the arithmetic unit derive their timing from the same source so that this unit works in step with the memory and every command takes a fixed length of time. The timing pulses for the various commands are derived from so-called period pulses coming at 8-μsec intervals corresponding to 8-μsec periods of the memory system. Timing arrangements inside these intervals are derived by the use of electrical delay lines.

In the Williams tube memory system, a time of 8 μsec is allowed for the operations at each cell in the memory. During these 8 μsec, about $2\frac{1}{2}$ μsec are allowed for the beam deflection circuits to stabilize. The beam is then turned on for about 1 μsec. If the position checked is found to store a zero (a dot in the dot-dash system), the beam is turned off for the rest of the period. If the position is found to store a one (dash), the beam is held on for another $3\frac{1}{2}$ μsec, while a sawtooth signal is applied to both deflection voltages (this restores the one, or dash, charge distribution on the face of the cr tube). The beam is turned off shortly before the end of the 8-μsec period so that it is safely off before the deflection voltages start to change.

Of interest, because of its novelty, is the method of eliminating the wait time when reading numbers from the drum or transferring information to the drum. The drum has 128 tracks with 32 words per track. Thus, each word arrives from the drum as a serial pulse train.

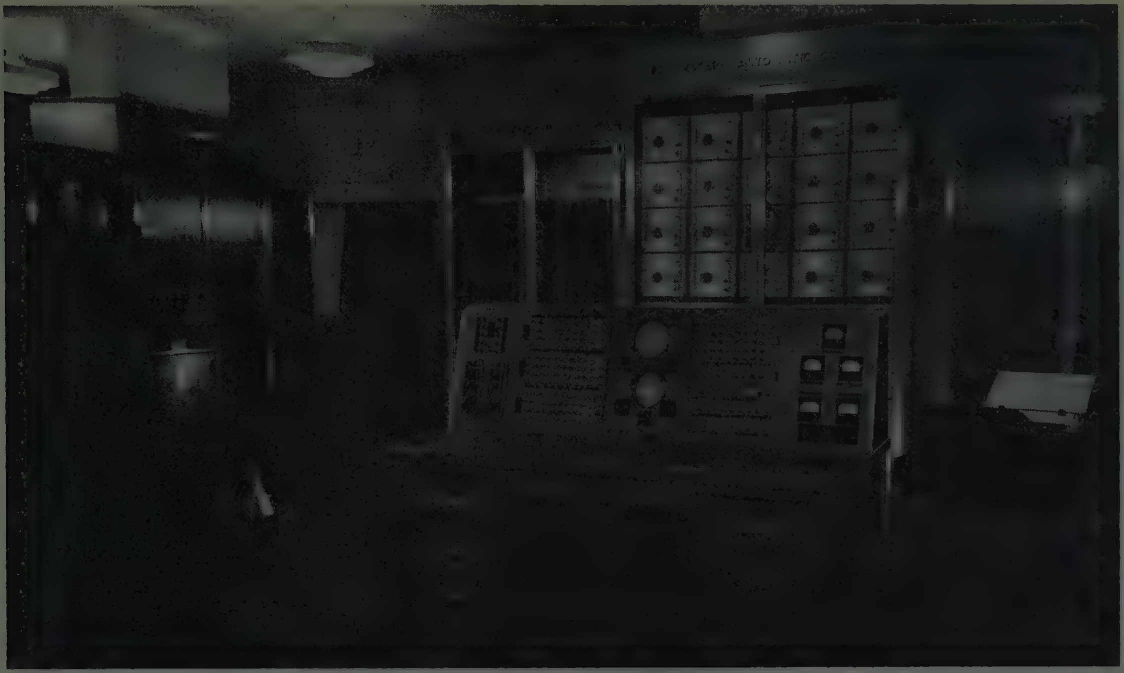


Fig. 1—The SWAC system. The SWAC computer and console, center right; IBM input equipment and magnetic drum memory unit, extreme left.

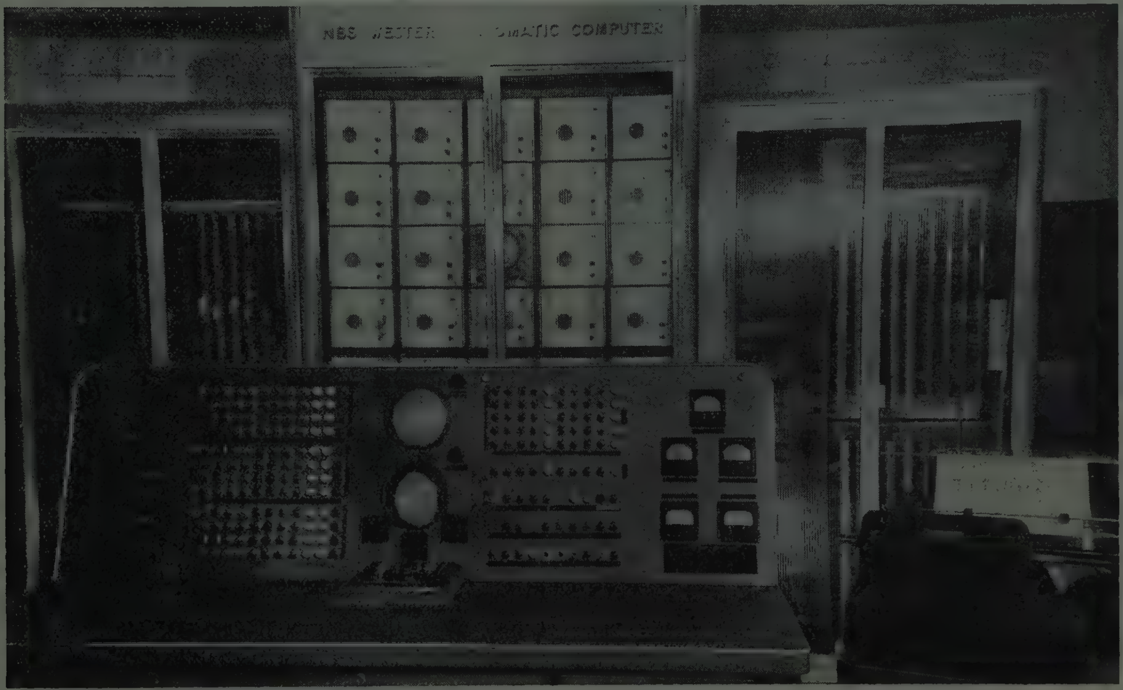


Fig. 2—The main SWAC computer, control console, and input typewriter.

Three pulse positions are left blank on the drum between words. The number arriving from the drum is shifted into one of the arithmetic registers, and it can be recorded in the electrostatic memory during the three-pulse time gap. Likewise, a new number can be read from the electrostatic memory and be ready to be recorded on the drum in this time interval. Thus, numbers can be handled in sequence in transferring to or from the drum.

A word-pulse channel drives a counter in the magnetic-drum circuits; this continuously keeps track of which particular addresses in the magnetic memory are available for reading or writing. Whenever a number is to be transferred to or from the drum, the address in this counter is sent to the Williams-tube selection circuits where it determines the five least significant digits of the memory address. The three most significant digits are specified by the command. This explains how the access time to the drum is reduced to approximately 500 μsec per word, since thirty-two words are transferred in, at most, one revolution plus one word time, or about 17 msec.

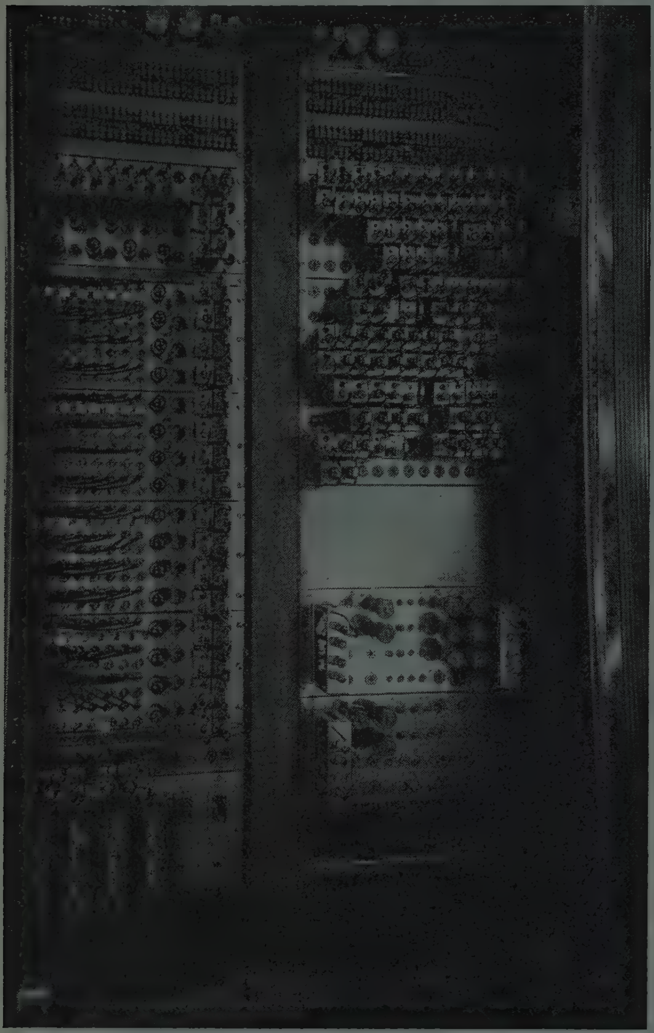


Fig. 3—Magnetic drum switching matrix and control circuits.

OPERATING EXPERIENCE

It may be of engineering interest that few tubes have been lost on account of heater failure. The heaters are turned on with transtats by hand and operated at rated voltage. The largest percentage of tube failures result from low emission and intermittent shorts. The average tube life in the SWAC ranges between 8,000 and 10,000 hours.

As is well known, there are two features of the Williams-tube type of memory which give trouble in computing machine applications. One of these is the presence of flaws on the face of the tube, which will not store information satisfactorily. The other is spill-over, or redistribution of charge, which limits the number of times the neighbors of a particular spot may be read before the spot in question must be regenerated. At the present time the only solution to the flaw problem seems to be particular care in manufacturing. Commercially available cr tubes are used in the SWAC and all tubes have some flaws in them. Therefore, the installation of circuits which eliminated most of the drift in the patterns on the face of tubes, provided the first substantial improvement in useful operating time on the computer.

Other improvements have been achieved by rebuilding certain parts of the circuitry which have shown a high out-of-order maintenance time. A substantial improvement in operating time occurred when an air-conditioning unit was installed, which maintained the incoming air in the ventilation system at a constant temperature. This minimized the temperature cycling of crystal diodes and substantially decreased their failure.

In the course of operation, certain logical facilities have been added to make the operation more efficient. A loudspeaker and buffer tube were added, with a plug-in arrangement allowing the operator to "listen" to any of the commands in a problem. For example, an alternate succession of add and subtract commands produces an 8-kc note. A certain problem involving generation of pseudorandom digits has produced sequences of tones christened "random symphony."

Additional Williams tube chassis have been inserted into the computer and arranged to record those addresses to which answers involving overflow have been sent, and to record all addresses in which answers have been inserted.

Recently, with the addition of one tube and a few crystals, a converting output command was obtained. This command, effective only with the output typewriter and tape punch, converts fractional binary numbers to octal, decimal, or any other base up to 16. This is accomplished by multiplying by the base, printing and deleting the integral part of the result, and repeating this process for the number of digits desired, up to a maximum of 11. Nonfractional numbers are handled by pre-multiplying by the appropriate constant.

PROBLEMS DONE ON THE SWAC

During the eight month period ending June 1, 1953, the SWAC spent on the average 53.2 hours per week in computing. More than 50 problems were handled in the past year, problems whose running time ranged from minutes to hundreds of hours. During this interval, the punched card input-output system was operative, but the magnetic drum was not as yet installed.

Problems solved on the SWAC originate from two sources. The staff of the Institute for Numerical Analysis originates problems in pure mathematics, in application to pure science, and in numerical analysis. Other government agencies and their contractors originate problems in applied mathematics and in engineering.

One of the most interesting problems in pure mathematics on which the SWAC has worked has been the study of Mersenne numbers, that is, numbers of the form 2^p-1, where p is a prime. These numbers, when prime, are related to the "perfect numbers" of the Greeks, numbers which are the sum of all their integral divisors excluding themselves. The present list of values of p which yield prime numbers is:

$$p = 2, 3, 5, 7, 13, 17, 19, 31, 61, 89, 107, 521, 607, 1279, 2203, \text{ and } 2281.$$

The last five values were added to the list by the SWAC as a result of the systematic testing of all prime numbers up to 2297. This project took 453 hours of time spread over 18 months of operation.

One application of mathematics to other fields of pure science is the study of Fourier Synthesis of X-ray diffraction patterns of crystals. Such studies, at present being carried on by members of the chemistry department of the University of California at Los Angeles, lead to the determination of the arrangement of molecules inside the crystals.

A classical problem in numerical analysis is the solution of systems of linear equations. Most of the methods in common use are variations of the elimination method that dates back to Gauss. A different approach to the problem is the conjugate gradient method developed by Hestenes, Lanczos, and Stiefel of the Institute staff. The numerical tests needed to perfect this method were made on the SWAC.

The applied problems supply examples of many of the primary fields of numerical analysis. In the field of linear equations, the SWAC has solved many systems of equations of order 10 to 15. Codes are prepared for the solution of systems of any order up to 45, but no system of that high order has as yet been solved. The characteristic values and their associated vectors have been found to 9 significant decimal digits for a 45th order system, as well as for systems of order 10 to 20. The large system took about 300 hours of SWAC time to reach a complete solution.

In the field of differential equations, a large amount of time was devoted to the study of Associated Legendre Functions, $P_n^m(x)$. The specific problem was the determination of the nonintegral values of the order (n) which, for fixed values of the degree (m) and argument (x), would make the value of the function zero. For each combination of m and x, an infinite set of discrete values of n will satisfy the requirements. The SWAC found the first thirty values of n corresponding to one value of x and three values of m.

Many applied problems deal with the reduction of large blocks of data. Such a problem handled by the SWAC arises from a study of the large-scale circulation patterns in the earth's atmosphere. Some 750,000 pieces of data, each of five decimal digits in length, were processed to yield about the same number of answers. SWAC spent 325 hours on this problem.

Problems in the evaluation of definite integrals have arisen from studies in probability and statistics. One such problem, the computation of a table of kill-probabilities, required the evaluation of 12,500 double integrals with each variable ranging from plus to minus infinity. This table was computed in 177 hours. A second table, used in biological experiments for probit analysis when the exact level of the dose is unknown, required the evaluation of 7,500 single integrals, this time with an infinite lower limit and a finite upper limit.

Finally, the SWAC has been used on several combinatorial problems. In some it has exhaustively searched through all possible combinations of several discrete variables. Such a problem is that of finding "difference sets," that is, a set of n numbers such that all $n(n-1)$ non-zero differences give distinct remainders on division by n^2-n+1.

The various examples cited indicate the types of problems that the SWAC has successfully solved. No attempt has been made to achieve complete coverage in this survey.

* * *

SEAC*

SIDNEY GREENWALD†, ASSOCIATE, IRE, R. C. HAUETER†, ASSOCIATE, IRE, AND
S. N. ALEXANDER†, MEMBER, IRE

Summary—**This article gives a comprehensive view of an electronic digital computer located at the National Bureau of Standards in Washington, D. C. The machine, called SEAC, has been in almost continuous operation since it was dedicated in the spring of 1950. It features a novel type of "transformer-coupled dynamic circuitry" and makes extensive use of germanium diodes. SEAC is a synchronous machine, operating at a one megacycle repetition rate. It is essentially serial in operation, employs both acoustic and electrostatic memories, and operates in either the three- or four-address mode at the programmer's discretion. This description covers the specifications of the machine, its logical, electrical, and physical structure, and finally, its performance over the last three years.**

INTRODUCTION

THE FIRST MAJOR CONTRIBUTION of the National Bureau of Standards to the development of electronic computing machinery occurred with the completion of the SEAC (Standard Eastern Automatic Computer) in May, 1950. This digital machine was the culmination of almost two years of intensive design and construction work. The initial objective set during the summer of 1948 was to provide at the earliest possible date a machine of limited computing power which would meet the immediate computational needs of the National Bureau of Standards. This installation would serve as a "stopgap" for the interim period during which full-scale equipment from a commercial source was being completed for delivery to the Government.

Toward the end of 1949 this point of view was gradually abandoned as it became evident that there would be no other equipment available for two years or possibly longer. As a result, the ultimate objective was altered so that a full-scale machine could be attained by expansion of the initial nucleus without delaying its completion. Still another aspect of building an expandable machine was the ability to use it as a proving ground for experimental equipment.

At the present time, after more than three years of regularly scheduled operation, SEAC is still actively employed in the solution of problems for both NBS and many government agencies. What is perhaps more important is that for the initial two years of its operation it was the most powerful computer installation readily available to the Government and thus was scheduled round-the-clock for a full seven-day week.

Since the machine was first put into operation, a significant fraction of the total time available has been devoted to the engineering work associated with the expansion of SEAC. The magnitude of this effort can be estimated from the fact that the number of vacuum tubes in the system was increased from approximately 750 to 1,300 and the number of germanium diodes from approximately 10,500 to 16,000. This expansion and testing program was carried out in the midst of a regular work load of important computation tightly scheduled because of priorities. This was no minor task, and consequently required careful planning.

A number of circuit and equipment innovations were included in the SEAC program in order to evaluate the reliability and serviceability of techniques that were highly promising but unproved. One example in this area is the extensive use of diode switching. Another is the achieving of ac coupling by using pulse transformers for highly variable duty-factor service. Success with these techniques made practical the use of vacuum tubes as a means of power amplification rather than as gating devices.

At the present, two machines based on a packaged version of the SEAC "transformer-coupled dynamic circuitry" have been completed. One is located at the Air Force Missile Test Center in Florida and the other at the Willow Run Research Center of the University of Michigan. A still further extension of these techniques was employed at the National Bureau of Standards in the construction of the DYSEAC.

OPERATING CHARACTERISTICS

The SEAC is an automatic high-speed digital computer that operates at a 1-mc pulse repetition rate. The machine is predominantly serial in nature and uses the binary number representation. Both instruction words and number words consist of 45 binary digits, which are equivalent to approximately 13 decimal digits. When the machine was first put into operation in May, 1950, eleven different types of operations were performed by it: (1) addition; (2) subtraction; multiplication, major part, unrounded; (4) multiplication, major part, rounded; (5) multiplication, minor part; (6) division; (7) comparison, algebraic value; (8) comparison, absolute value; (9) logical transfer; (10) read in; and (11) print out. The instruction words expressed these operations in the four-address mode. The original high-speed memory consisted of 512 words of acoustic delay-line storage, and all of the input-output devices were modified Teletype equipment. The input was from either a tape reader or keyboard, and the output was to either a printer or tape punch.

During the three years the machine has been operating, it has been expanded into a far more powerful and convenient tool than its original conception. For example, five additional operations have been incorporated: (1) reverse tape or wire, (2) logical multiplication, (3)

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, July 9, 1953. The work described in this paper was sponsored by the Office of the Air Comptroller, Department of the Air Force.

† National Bureau of Standards, Washington, D. C.

base, (4) file counter information, and (5) clear memory cell, bringing to a total of 16 the types of operations available. An experimental Williams type electrostatic memory has also been added. This stores 512 words in 45 cathode-ray tubes, with parallel access to a complete word in 12 μsec. An alternative instruction system using the three-address mode of operation has also been installed. By simply setting several switches inside the machine, the computer is set for operation in either the three-address or four-address system.

Magnetic wire and magnetic tape units were added to increase the speed of the computer on problems which require considerable input-output or auxiliary memory capacity. In particular, the magnetic-wire handling equipments greatly speed up initial input and final output. Magnetic tape units, both single- and multiple-channel, provide external memory. Fig. 1, which is a view of the computer from the console side, shows several of these units. Either automatic or manual selection of input-output units is available. Still another feature which has been added by modification of the circuitry is the ability to automatically monitor the operations being performed. When called into use by setting a switch on the console, this feature causes the machine to print out the program-sequence counter information, the instruction being performed, and the result of the operation. This facility is a great convenience, and will be discussed in more detail later.

Fig 1—View of computer from control console side.

The component parts of an instruction word in both the four-address and three-address systems are shown in Fig. 2. In the four-address system the addresses are denoted by the symbols α, β, γ, and δ. Normally α is the address of the first operand, β the address of the second operand, γ the address of the result of the operation, and δ the address of the next instruction. The instruction also contains a code specifying the type of operation to be performed and a conditional halt-control digit in the sign position. An address comprises ten binary digits, so it can designate one out of 2^{10} or 1,024 memory cells. This is sufficient for the two SEAC memories. Four binary digits specify the operation to be performed. The sixteen different operation codes thus available are now all used. The single binary digit in the sign position indicates whether or not the computer is to halt after performing the operation. In the course of executing one instruction, the control of the computer cycles through four phases, one for each reference to the memory. In a typical address β is referred to in phase 2, α in phase 3, γ in phase 4, and δ in phase 1.

A typical three-address instruction word contains the addresses α and β of the operands and the address γ of the result. The remainder of the word contains floating-address information, the code specifying the type of operation to be performed, and the conditional halt digit. Twelve binary digits are used to specify an address, providing the basis for selection among 4,096 memory cells, and four binary digits are used to provide information for the floating address feature. The operation code for the sixteen instructions is the same as in the four-address system.

The main difference between the three- and four-address systems is in the designation of the next instruction to be performed. In the four-address system the instruction contains an explicit statement (δ) designating where the next instruction is located in the memory. In the three-address system, however, there is no such explicit statement. Instead, instructions in this system are automatically sequenced in accordance with a convention, successive instructions being normally located in consecutively-numbered memory positions. An exception to this convention is available through the comparison (conditional transfer) operation, whenever the first operand (α) is less than the second operand (β). In this case the result of the comparison leads to what is called a "jump" operation in which the next instruction for both the three-address and four-address systems is chosen from address γ.

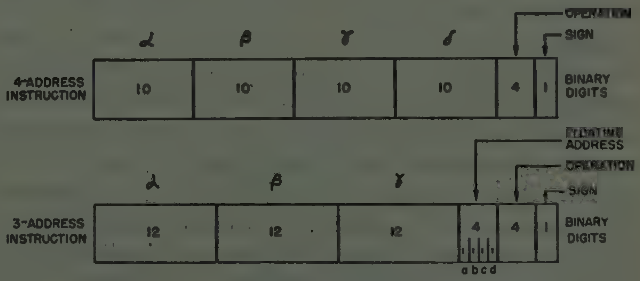


Fig. 2—Component parts of a SEAC instruction.

The floating address feature allows the programmer to designate any address as either absolute or relative. An absolute address is interpreted in the usual sense, merely as a number identifying a specific memory location. A relative address, however, identifies a position in the memory by specifying its displacement relative to that position from which the instruction word itself was taken. To illustrate: suppose an instruction located in memory position m specifies that the address of the the first operand is number 17 relative. Then the control will take the word in memory location $(m+17)$ and use it as the first operand. If location $(m-17)$ is desired, the complement of 17 is used as the address.

It is possible to use any combination of absolute or relative addresses in an instruction word. Of the four binary digits that supply floating address information, the first three digits, a, b, and c, indicate whether α, β and γ, respectively, are absolute or relative. The fourth binary digit d tells which of two control counters is to be used during operation in the three-address mode. Counter 0 is normally the operating counter. However, starting with any desired address, counter 1 can be put into operation by a "jump" comparison in which γ is the desired address and binary digit d specifies counter 1. Counter 1 will be the operating counter only so long as d in each following instruction indicates counter 1. As soon as an instruction is reached in which d indicates counter 0, the control automatically returns to counter 0 after performing the instruction.

A typical use of this feature is to code sub-routines for counter 1 with floating addresses. The use of floating addresses allows the sub-routine to be placed anywhere in the memory automatically. By coding a sub-routine for counter 1, a "jump" comparison sends the control to counter 1 at the desired address, and after finishing the sub-routine it returns the control automatically to counter 0 at the point in the main program where it left off.

The basic operations of SEAC and their functions are summarized in Table I.

MACHINE ORGANS

An over-all block diagram of SEAC is shown in Fig. 3, in which information paths are shown as solid lines and control paths as dashed lines. Interchanges of information between the shift register, the arithmetic unit, the control, and the mercury memory are made through the unit called the "bus." The bus not only provides correct routing of information but correct timing as well. During an input operation instructions and numbers are read into the shift register from one of the input-output units via the selection circuits. From the shift register there are two possible paths. The digits are transferred either in parallel into the electrostatic memory or serially into the mercury memory via the bus. For an output operation the procedure is the same but the path is reversed. For internal operations instructions are routed from the memory to the control unit, and numbers routed between the memory and the arithmetic unit. Transfers are made to and from the mercury memory directly through the bus. Whenever the electrostatic memory is used, an additional transfer through the shift register is required.

TABLE I

NAME OF OPERATION	DESCRIPTION OF INSTRUCTION
Addition	Form the sum of word in α and word in β, and write result in address γ in the memory.
Subtraction	Form the difference between the word in α and the word in β, and write the difference in address γ in the memory.
Multiplication, major, unrounded	Form the product of the word in α and the word in β, and write the major part (unrounded) in address γ in the memory.
Multiplication, major, rounded	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory.
Division	Form the quotient of the word in β divided by the word in α, and write it in address γ in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits of the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal next-instruction address position. (In the four-address system, this is address δ in the memory; in the three-address system, this is the next consecutively numbered address position.) If, however, the word is α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	Perform algebraic comparison except treat both words as positive.
Read in	If the address number β is odd, read in one word from the selected external unit designated by address number α, and write the data in address γ in the memory; if the address number β is even, read in eight words, and write in the eight addresses beginning with address γ.
Print out	Print out the word in address γ in the memory if the address number β is odd (or the block of eight words beginning with address γ if β is even) onto the selected external unit designated by address number α.
Reverse	Reverse through one word if the address number β is odd (or through eight words if the address number β is even) on selected external unit designated by address number α.
Logical multiplication	Write the digit-by-digit product of the words in addresses α and β into address γ in the memory.
Base (primarily for four-address system)	If address number α is greater than or equal to address number β, put the number β into the special base-number counter-register and take the next instruction from address γ in the memory. In subsequent instructions, all references to odd-numbered addresses will now be interpreted relative to this constant number β. If address number α is less than address number β, the counter-register is cleared and the next instruction is taken from address γ in the memory.
File	Write the contents of special counter-registers into memory address γ.
Clear	Clear memory address γ.

The arithmetic unit in SEAC is involved in almost every operation that the computer performs, with the exception of several such as file and base. Fig. 4 is a block diagram of the arithmetic unit. In the process by which two numbers are added, the first number enters the arithmetic unit in phase 2 of the cycle through which the computer sequentially progresses. If the number is positive, it goes through the input complementer and adder into the accumulator register. If the number is negative, the sign sensing unit activates the input complementer, and the complement of the number is sent to the accumulator register. During phase 3 the second number is sent to the arithmetic unit. Again it is complemented or not, depending on whether it is negative or positive. The second number is then added to the first number, which has been circulating in the accumulator register and is available at the second input to the adder. In phase 4, the result of the addition is sent via the output complementer through the bus connection to the memory. If the result is negative, the sign determining unit inserts a binary 1 in the sign position of the number and also activates the output complementer.

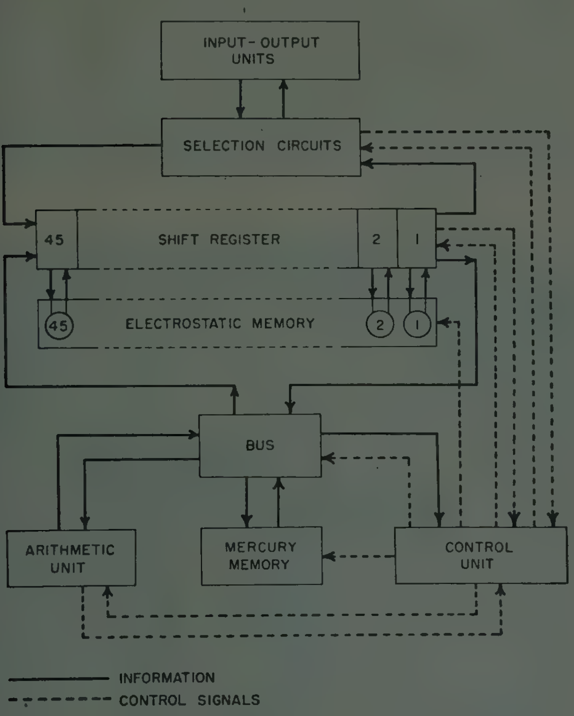

INPUT-OUTPUT UNITS
SELECTION CIRCUITS
45
SHIFT REGISTER
2
1
45
ELECTROSTATIC MEMORY
2
1
BUS
ARITHMETIC UNIT
MERCURY MEMORY
CONTROL UNIT
INFORMATION
CONTROL SIGNALS

Fig. 3—Block diagram of SEAC.

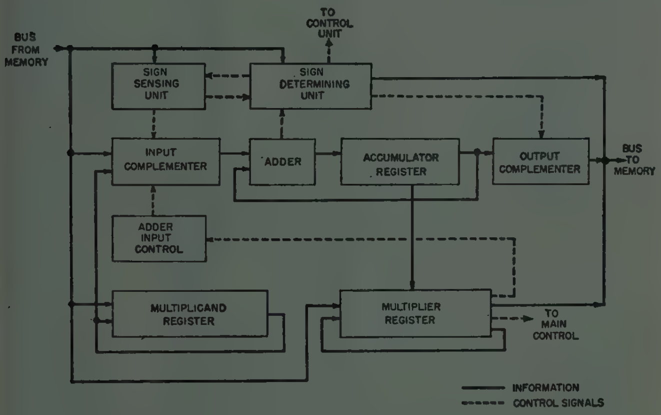

TO CONTROL UNIT
BUS FROM MEMORY
SIGN SENSING UNIT
SIGN DETERMINING UNIT
INPUT COMPLEMENTER
ADDER
ACCUMULATOR REGISTER
OUTPUT COMPLEMENTER
BUS TO MEMORY
ADDER INPUT CONTROL
MULTIPLICAND REGISTER
MULTIPLIER REGISTER
TO MAIN CONTROL
INFORMATION
CONTROL SIGNALS

Fig. 4—Block diagram of arithmetic unit.

The process of subtraction is almost identical, the difference being that the effect of the sign of the number from β on the sign sensing unit is reversed. The process for a comparison is similar to that for subtraction. However, no result is transferred to the memory; instead a signal is sent to the control unit when α is less than β.

Multiplication is performed in SEAC by repetitive additions which involve the use of two other registers, the multiplier and the multiplicand registers. In phase 2, β enters the multiplier register and in phase 3, α enters the multiplicand register. Multiplication is accomplished by successive additions of the multiplicand to the partial product in the accumulator register under the control of the digits of the multiplier. The shifting is accomplished in the accumulator register by shortening it one pulse time. Division is also a repetitive process using all three registers, with the quotient formed in the multiplier register. The nonrestoring method of division is used and consists of successive subtractions or additions of the divisor, according to the sign of the remainder. Physically, the entire arithmetic unit occupies only one and one-fourth relay racks. It is interesting that this early design for a binary adder, which is used in all computations, employs only three single-cathode vacuum tubes.

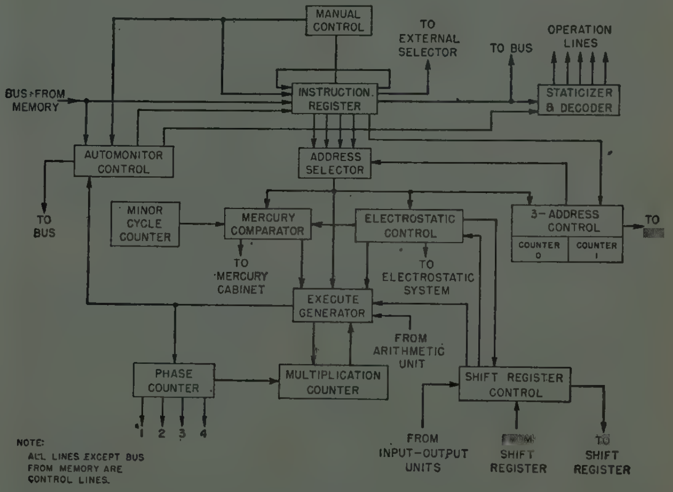

MANUAL CONTROL
TO EXTERNAL SELECTOR
TO BUS
OPERATION LINES
BUS FROM MEMORY
INSTRUCTION REGISTER
STATICIZER & DECODER
AUTOMONITOR CONTROL
ADDRESS SELECTOR
TO BUS
MINOR CYCLE COUNTER
MERCURY COMPARATOR
ELECTROSTATIC CONTROL
3-ADDRESS CONTROL
COUNTER 0
COUNTER 1
TO
TO MERCURY CABINET
TO ELECTROSTATIC SYSTEM
EXECUTE GENERATOR
FROM ARITHMETIC UNIT
PHASE COUNTER
MULTIPLICATION COUNTER
SHIFT REGISTER CONTROL
1 2 3 4
NOTE:
ALL LINES EXCEPT BUS FROM MEMORY ARE CONTROL LINES.
FROM INPUT-OUTPUT UNITS
FROM SHIFT REGISTER
TO SHIFT REGISTER

Fig. 5—Block diagram of control unit.

The control unit is the most complex part of the computer, as may be seen in the simplified block diagram of the control in Fig. 5. This has resulted partially from the experimental nature of the machine and from the continuous expansion it has undergone. One of the major functions of the control unit is to decode the instruction to determine (1) the type of operation to be performed, (2) the location of the numbers involved in the operation, and (3) the location of the instruction to be performed next. After the instruction is received from the memory, it circulates in the instruction register. The digits representing the operation are decoded in the staticizer and decoder, and the appropriate operation lines are activated.

The addresses are selected one at a time in what is called the address selector. If the location called for is in the mercury memory, the address information is sent to the mercury comparator. When the output of the minor cycle counter agrees with the temporal selection portion of the address, the mercury comparator sends a signal to the execute generator that the desired word is in position to be read out. The phase counter is then advanced and the transfer is made. On the other hand, if the location called for is within the 512 words of the electrostatic memory, the address is routed into the electrostatic control. This control then determines when the execute generator will advance the phase counter, and when transfer between the electrostatic memory and the shift register will be made. In three-address operation the information from the selected counter is sent to the address selector where it is used to select relative addresses and the location of the next instruction.

The shift register control serves mainly to direct the transfer of information in and out of the shift register at the rate acceptable to the input output device in use. The automonitor control automatically cycles the computer through the necessary print-outs for each instruction being monitored. The multiplication counter counts off the 44 minor cycles (word times) necessary for a multiplication or division, and prevents the phase counter from advancing until this portion of the operation is completed. Finally, the manual control permits the computer to be started or stopped, or its operation to be modified, by means of switches located on the console.

The mercury memory for SEAC is housed in a separate cabinet which contains the 64 mercury-filled acoustic lines, their associated amplifiers and gating circuits, the selection matrix, and other miscellaneous circuitry. Fig. 6 shows one side of the cabinet with 32 of the recirculation amplifiers and half of the selection circuitry. Since the nominal delay through the lines is 384 μsec, eight words of 48 digits each are stored in each mercury line. Thus the total capacity of the memory is 512 words.

Because the delay of a mercury line varies somewhat with temperature, and yet the whole memory must be kept in step with the crystal-controlled computer clock, it is necessary to maintain all lines at the same constant temperature. A system of aluminum plates and extrusions bonds the 64 mercury-filled glass tubes into a nearly isothermal unit, which is insulated from the outside and is electrically heated and thermostated to 50±0.25°C.

Pulses are stored in each line as packets of an 8-mc carrier. For every binary one there is an associated RF pulse packet, and for every zero there is a gap. The acoustic output of the line activates a quartz crystal whose electrical output is then transformer-coupled to the input of the recirculation amplifier. The first three tubes serve as an RF amplifier and detector with an over-all gain of 50 to 55 db and a center frequency of 8 mc. The fourth tube in the chain has the function of switching information into or out of the line as well as that of synchronizing and reshaping. The fifth tube develops the 8-mc packet of 200 volts peak-to-peak amplitude which is transformer-coupled to the input crystal of the mercury line.

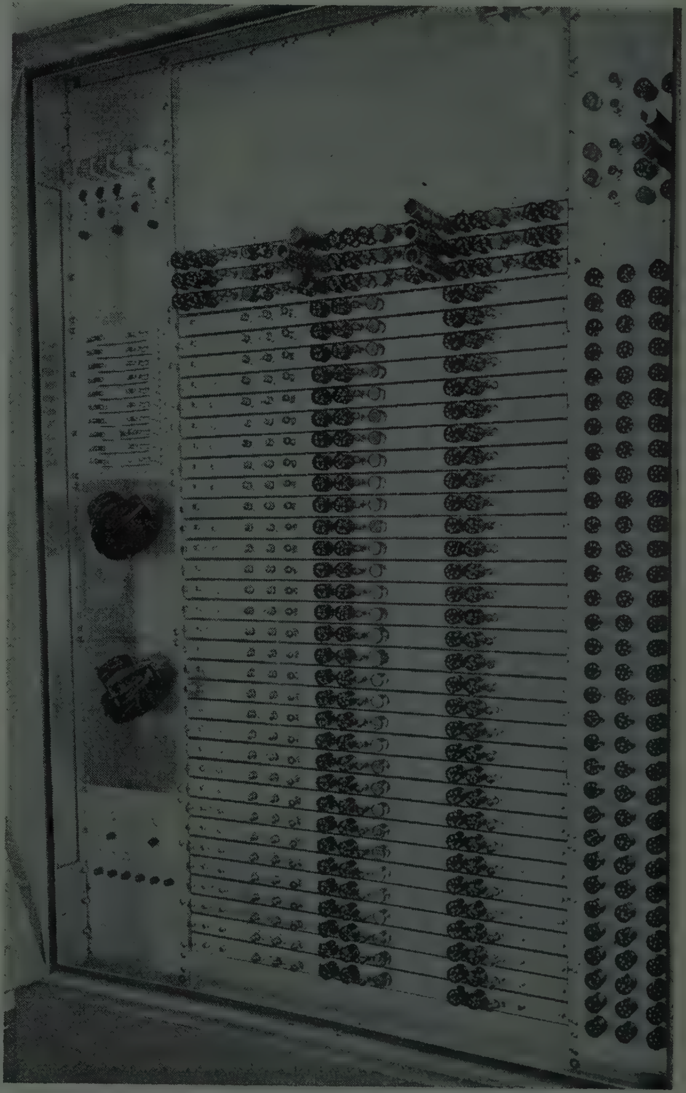


Fig. 6—Side view of mercury memory cabinet (dimensions approximately 3×5×6 ft).

Fig. 7 shows the general organization of the mercury cabinet. Digital information denoting the mercury line to be selected comes from the mercury comparator located in the control section of the machine. An electrical delay line brings these time sequential pulses into positions from which they can be simultaneously gated into six flip-flops with associated drivers. This portion of the circuitry is called access gating or, more popularly, "G" generators. The varied combination of six positive and six negative pulse lines from the "G" generators selects one of the 64 mercury lines which connect with the matrix. When writing into the memory which is done in phase 4, information appears on the bus to memory, from which it is routed to the selected memory line, the old information being simultaneously deleted. In phases 1, 2, and 3 information from the selected address is transmitted via the output mixer of the matrix to the bus. Information is erased by interrupting the recirculation path when new information is written in.

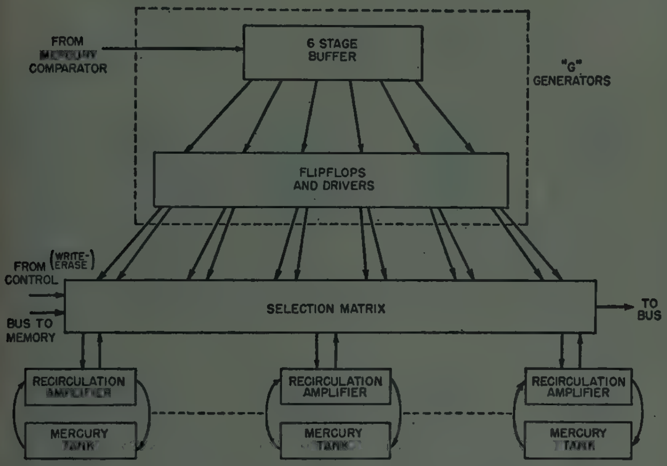

FROM
MERCURY
COMPARATOR
6 STAGE
BUFFER
"G"
GENERATORS
FLIPFLOPS
AND DRIVERS
FROM CONTROL (WRITE-ERASE)
BUS TO
MEMORY
SELECTION MATRIX
TO
BUS
RECIRCULATION
AMPLIFIER
MERCURY
TANK
RECIRCULATION
AMPLIFIER
MERCURY
TANK
RECIRCULATION
AMPLIFIER
MERCURY
TANK

Fig. 7—Block diagram of mercury memory.

As previously mentioned, in addition to the acoustic memory SEAC also includes a full-scale experimental electrostatic memory. This provides an additional 512 words of storage, effectively increasing the capacity of the machine to 1,024 words. Since this memory is arranged to operate in the parallel mode, the access time is considerably decreased, which thereby increases the speed of the machine over that possible with the mercury memory. The type of electrostatic storage is that originated by Williams and Kilburn, in which the phosphor surface of a conventional cathode-ray tube is charged to store digital information.

This memory occupies approximately six standard relay racks. Four racks hold the cathode-ray tubes (CRT), plus their associated regeneration amplifiers and gating circuitry. The remaining two racks contain the deflection generators, the counter, and other control circuitry. There are actually 48 CRT positions, but only 45 are employed at any one time. The other three positions are available as spares. Two types of cathode-ray tubes are used for storage, the 5UP1 and the 3KP1. The well-known dot-slide technique is used, in which a dot signifies a binary zero and a dash a binary one.

Fig. 8 is a block diagram of the electrostatic memory for SEAC, showing the flow of information and the method of control. Numbers or instructions are transferred to the memory along parallel lines from the shift register, and this information is stored for as long as it is needed by a continuous process of regeneration which takes place with the aid of the regeneration amplifiers. At any given time the location of the electron beam in the CRT is determined by the digital information in the staticizer, which can be loaded from either the address register or the regeneration counter. The staticizer sends out pulses of about seven μsec duration. These pulses are sent to the deflection generators where they are decoded and converted to CRT deflection signals having accurately derived voltage levels. All 48 CRT's are deflected in parallel, and the actions of turning the the beam on and strobing the output signal of the amplifier are also performed simultaneously for all CRT positions.

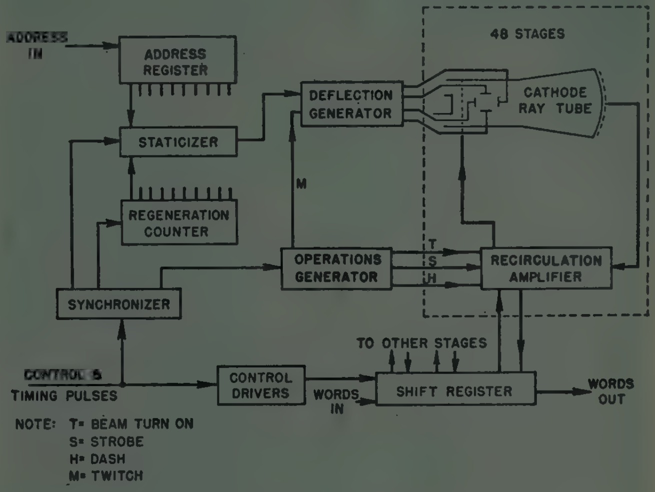

ADDRESS
IN
ADDRESS
REGISTER
48 STAGES
DEFLECTION
GENERATOR
CATHODE
RAY TUBE
STATICIZER
M
REGENERATION
COUNTER
T
S
H
OPERATIONS
GENERATOR
RECIRCULATION
AMPLIFIER
SYNCHRONIZER
TO OTHER STAGES
CONTROL &
TIMING PULSES
CONTROL
DRIVERS
WORDS
IN
SHIFT REGISTER
WORDS
OUT
NOTE: T= BEAM TURN ON
S= STROBE
H= DASH
M= TWITCH

Fig. 8—Block diagram of electrostatic memory.

The operations generator provides the proper "turn-on" signals to the CRT grids for both dot and dash conditions. It also provides a strobe pulse to the amplifier and a "twitch" signal to the deflection generators. The synchronizer dispatches signals to the other units to insure that the correct sequence of pulses takes place and, furthermore, that these actions are synchronous with the rest of the machine.

When the electrostatic memory is being used, a read or write action can take place as frequently as every 48 μsec. Of this time, only 12 μsec is actually required for the action, so the remaining time is always used to accomplish three regenerations.

The shift register and its control comprise two full racks of equipment which are shown in Fig. 9. Its size and complexity are due to its many functions. First, it acts as an intermediary or buffer storage between the input-output equipment and the serial acoustic memory. In connection with input-output operations, it also has the functions of digit counting, word counting, and word inversion. Further, the shift register acts as a register for the electrostatic memory, which operates in the parallel mode, and serves to provide the transfer to and from the serial representation in the rest of SEAC. In connection with the electrostatic memory, it also helps perform the logical transfer operation.

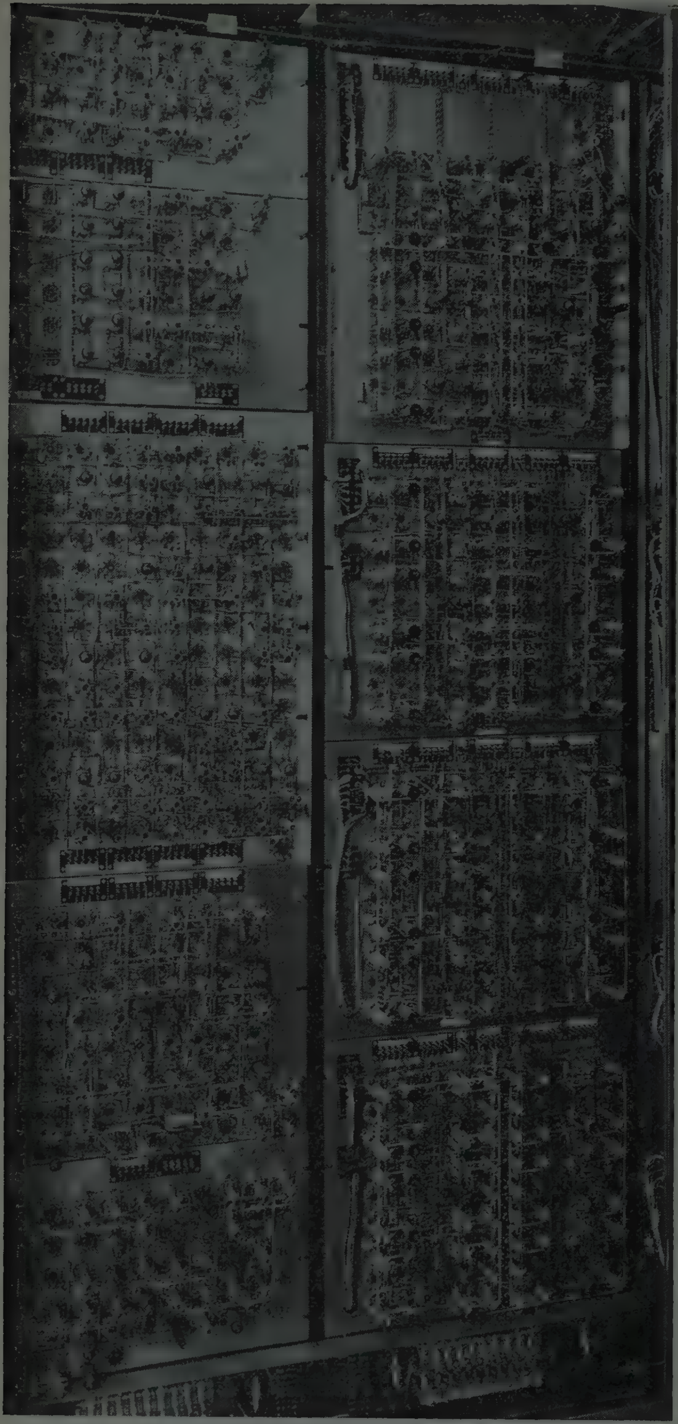


Fig. 9—View of shift register and shift register control.

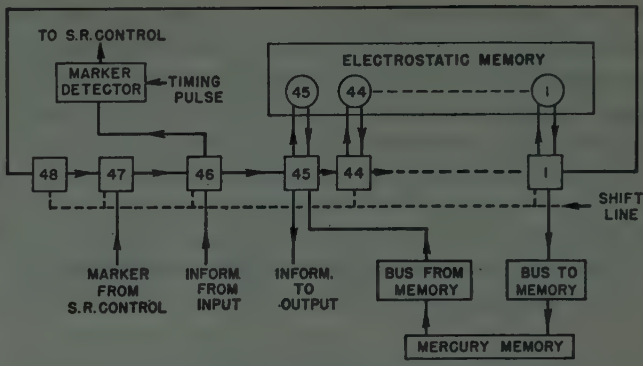


Fig. 10—Block diagram of the shift register.

Fig. 10 is a simplified diagram of the shift register showing how it connects to both memories. It will be noted that the register consists of 48 flip-flops arranged in a closed loop. Shifting may be done only to the right, as indicated by the arrows. During an input operation the highest order of the number comes in first and is sent to stage 46. This digit then undergoes a series of right shifts, until it ends up in stage 47. Then the second highest order digit is inserted in stage 46, and again a series of right shifts takes place. This process continues until the entire number has entered the shift register. When the number is in position, a marker pulse signals the end of operation. At this time the number is shifted serially from stage 1 of the shift register into the memory at a 1-mc rate.

During an output operation the reverse process takes place. The number is shifted rapidly into the register through stage 45. Then, one digit at a time is sent to the appropriate tape, wire, or teletype unit via stage 45. The end of operation is again signaled by the marker pulse.

Some salient facts pertaining to input-output equipment may be of general interest. The teletype equipment operates at six characters per second, with each character representing four binary digits. This gives an equivalent speed of two seconds per word. Because of this low speed, teletype is used primarily for manual operations, for which it is a convenient means for printing out or inserting information in any memory location. The wire units, which employ cartridge loading, are used mainly for initial input and final output from the computer. The time required to fill the mercury memory from the wire input is about 12 seconds, including the time for manual manipulations. The tape units developed for external storage use no reels and are single channel only. These units will hold up to 24,000 words on a 1,200-foot tape. Recently a multi-channel tape unit was added to SEAC. Both types of tape unit have extremely rapid acceleration, starting and stopping in less than 5 msec. This characteristic makes them especially valuable for external storage.

The input-output selector (upper half of Fig. 11) consists of the manual switches and the circuitry necessary to select one or more units for an input or an output operation. The system permits selection from among ten different units. A unit may be selected automatically by inserting the proper information in the input or output instruction. The five binary digits that contain the necessary coding enter the selection register, as indicated in Fig. 12. The outputs of the register energize at least one selector relay (shown at the top of the diagram) by means of the selection gates and automatic selection switches. These multicontact relays switch the necessary signals to control reading and writing on the unit. An input or an output instruction, of course, contains a code to designate a particular input-output unit; however, by means of manual switches on the input-

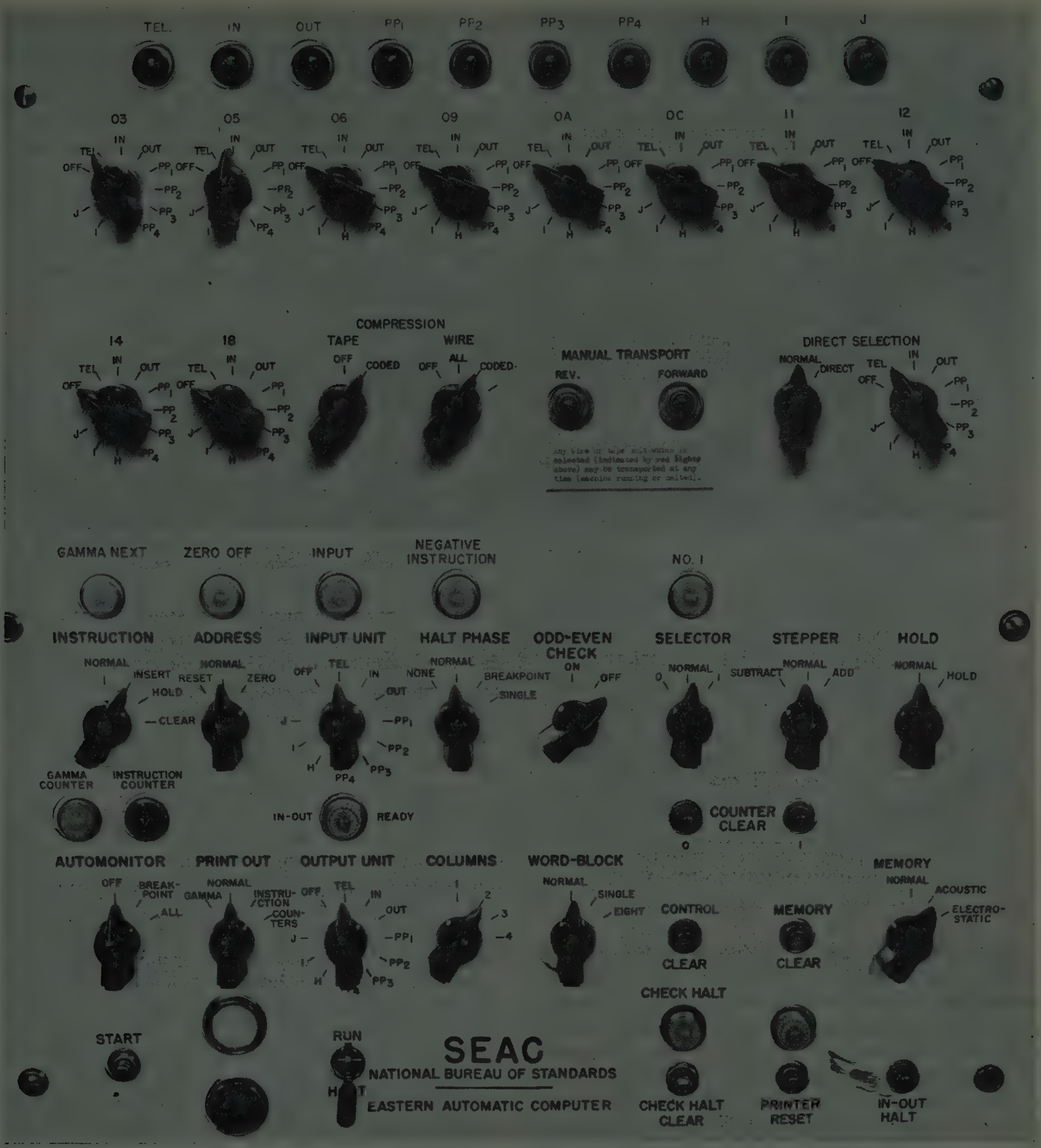

TEL.
IN
OUT
PP1
PP2
PP3
PP4
H
I
J
03
05
06
09
0A
0C
11
12
14
18
COMPRESSION
TAPE
WIRE
OFF
CODED
ALL
MANUAL TRANSPORT
REV.
FORWARD
DIRECT SELECTION
NORMAL
DIRECT
GAMMA NEXT
ZERO OFF
INPUT
NEGATIVE INSTRUCTION
NO. 1
INSTRUCTION
ADDRESS
INPUT UNIT
HALT PHASE
ODD-EVEN CHECK
SELECTOR
STEPPER
HOLD
INSERT
CLEAR
RESET
ZERO
NONE
BREAKPOINT
SINGLE
ON
SUBTRACT
ADD
GAMMA COUNTER
INSTRUCTION COUNTER
IN-OUT
READY
COUNTER CLEAR
AUTOMONITOR
PRINT OUT
OUTPUT UNIT
COLUMNS
WORD-BLOCK
MEMORY
BREAK-POINT
GAMMA
INSTRU-CTION COUN-TERS
EIGHT
CONTROL
ACOUSTIC
ELECTRO-STATIC
CHECK HALT
START
RUN
HALT
SEAC
NATIONAL BUREAU OF STANDARDS
EASTERN AUTOMATIC COMPUTER
CHECK HALT CLEAR
PRINTER RESET
IN-OUT HALT

Fig. 11—View of input-output selector panel (top) and manual control panel (bottom).

output selector one can establish any correspondence desired between the codes and the actual devices. This feature is especially useful when a new code is being checked or when one of the units happens to be inoperable.

The function of the comparator is to determine when the input-output unit called for is different from the one previously chosen. Only in this situation is the computer halted momentarily while the necessary relays are energized. Automatic selection can be overridden by any of the manual selection switches. There are three of these switches, one for manual input operations, one for manual output operations, and one for direct selection during computation.

There are a number of auxiliary units physically separate from SEAC which allow the slow work of preparing input programs and data and that of printing the output results to be accomplished without losing valuable computing time. Teletype keypunches and reperforators are used to prepare the initial punched paper tape. An inscriber transfers the information from the punched tape onto magnetic wire for rapid computer input and automatically inserts the proper spacing between blocks of information. An outscriber takes the output data recorded onto wire by the computer and produces a punched paper tape. This unit takes its information from a continuously moving wire, performs the necessary operations of counting and recognizing each binary digit, punches the paper tape, and checks for errors in the transcription to the wire as well as errors in its own operation. Additional equipment produces printed copy or punched cards, or both, from the tape punched by the outscriber.

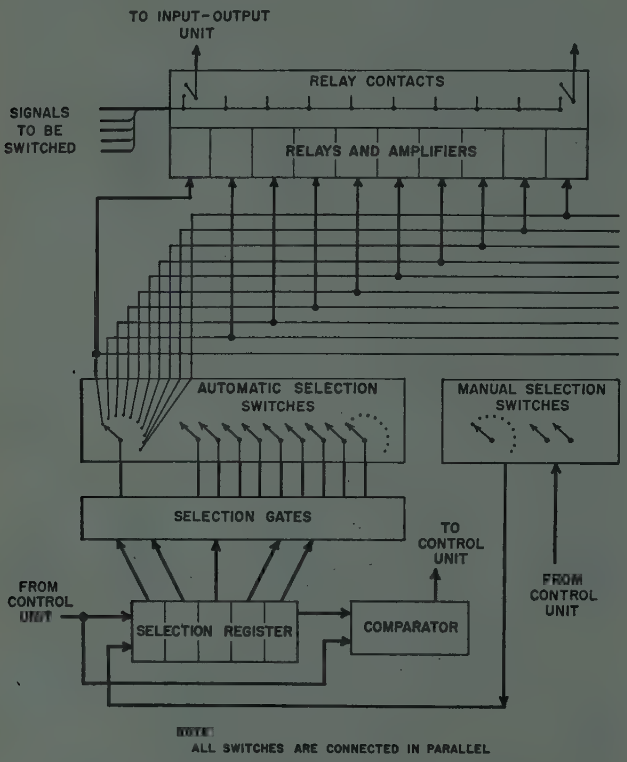


Fig. 12—Block diagram of selection circuits.

Besides the fundamental requirements of starting and stopping the machine, the SEAC control console has many facilities which enable the operator to follow the course of the problem, print out any desired information, and make any changes that might be required. Only a few steps are required to put a new problem into the computer. These are clearing the control and memory, selecting the desired input unit, and pressing the start button. To perform a manual print-out, the machine must first be halted by throwing the run-halt switch. The computer then halts after performing the present instruction. The print-out switch is then positioned to allow the operator to print out either the instruction just performed, the result of the instruction, or the counter contents. The manual output-selector switch allows the operator to select any unit, but the one usually chosen is teletype.

To insert a word into any specified memory location, first the machine must be halted and the instruction switch thrown to INSERT. When the start button is pushed, an input instruction in which γ is the specified location is read into the first cell of the memory from the unit selected by the input selector switch. Again the unit selected is usually teletype. The instruction switch is now set back to normal, the start button pushed once more, and the operation completed. The memory selector switch permits computation to be carried out in either the electrostatic or mercury memory without a change in coding. In the normal position of the switch both memories are in use. The preceding discussion is by no means an exhaustive treatment of the switches and manual-control operations available, but mentions briefly those most frequently used.

Circuitry and Symbols

The circuitry of SEAC follows a rather uniform pattern throughout most of the central computer, with the exception, of course, of recirculation amplifiers, magnetic tape amplifiers, and the like. This pattern consists of diodes and resistors for gating, a beam power tube for amplification, and a transformer for coupling to subsequent stages. By intensive engineering of a single type of circuit, a high degree of reliability was achieved and subsequent design, testing, and maintenance were simplified.

Fig. 13 shows a typical gating stage, of which there are numerous variations. Certain facts about the gating should be pointed out. The diode structure is three gates deep, or-and-or. Up to five inputs are allowed to each gate before the resistor values must be changed; however, this condition occurs in few locations. The resistors are computed to allow a minimum rise of 100 volts μsec during any part of the pulse excursion. The diodes drawn in a horizontal direction carry pulse information; those drawn in a vertical direction are the clampers. It will be noticed that the gate output, which connects to the grid of the amplifier, is connected to a -5-volt clamping diode. Since the middle of the gate employs a -8-volt clamping diode, a 3-volt disconnect is obtained across the final or-gate. This is important in preventing noise from producing spurious signals. An additional disconnect of 2 volts is achieved by connecting the positive output of the transformer to -10 volts. Negative inputs to and-gates that are used for inhibition omit the initial or-gate, and the position of the -8-volt clamping diodes is shifted to prevent them from drawing excessive current.

The single vacuum tube in the stage, tube type 6AN5, has no gating function. Its purpose is power amplification only. The 6AN5 is a miniature beam power tube with some excellent characteristics for this kind of computer service. Its pertinent characteristics are enumerated as follows:

input capacitance	9.0 $\mu\mu$f
output capacitance	4.8 $\mu\mu$f
transconductance	8,000 μmhos
filament rating	0.45 amp at 6.3 v.

The cathode material is passive nickel which apparently prevents the formation of interface impedance.

In the unpulsed condition the tube stands by with a current of at least 1 ma. The clamping diode to +2 volts and a small resistor in the cathode circuit help keep the dissipations of the control and screen grids within ratings.

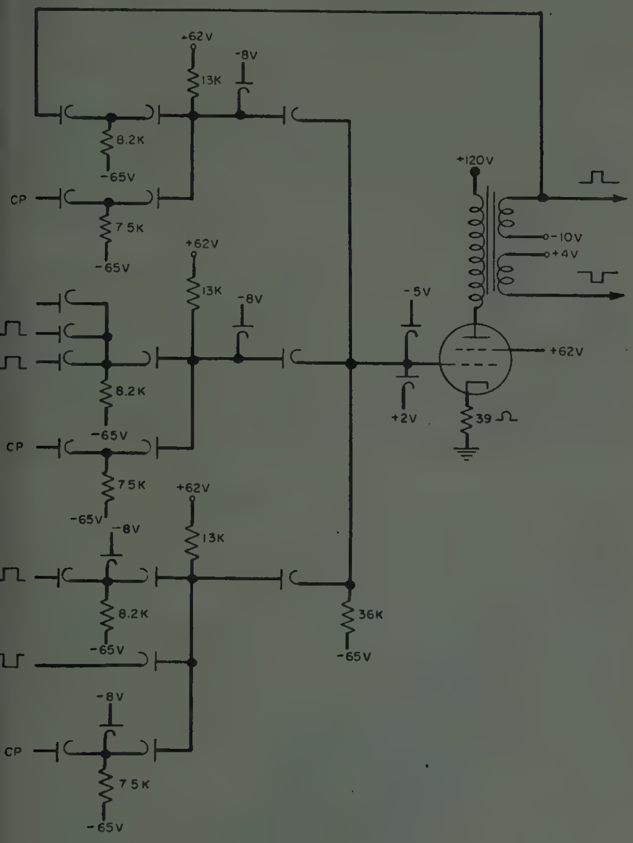


Fig. 13—A typical SEAC stage.

The transformer used for coupling has several advantages. It provides impedance matching between tube and load, it enables a single stage to transmit either positive or negative pulses, and it avoids the difficulties involved in dc coupling. A step-down ratio of either 5 to 1 or 7 to 1 is used in most SEAC circuits. In any case, the equivalent load presented to the tube is such as to cause the tube to bottom, i.e., to operate below the knee of the $e_p - i_p$ curve. This kind of operation results in almost uniform voltage output even though tubes with 2-to-1 variation in current capabilities are plugged into the same circuit. The cores of the pulse transformers in SEAC are grain-oriented silicon iron in one-thousandth inch thick laminations.

Since SEAC is a synchronous machine, it requires precise timing pulses to all its circuits to keep the various parts of the machine in step. This is accomplished by the use of a 1-mc master clock which resembles a small RF transmitter. The clock signals are not distributed as rectangular pulses or half sine waves, as might be expected, but are full sine waves. There are definite advantages in using sine wave distribution from the viewpoint of generation at high power levels, distribution without excessive pulse deterioration, and ease of phase shifting to produce the same precise timing in all parts of the computer. As the clock signal passes through the gating structure, only the trapezoidal center portion reaches the grid of the tube. These clock pulses are slightly under one-half μsec at the top of the gating level. Although the computer could have been designed with a clock having only a single phase, the clock signals are actually distributed in three phases 120 degrees apart which are named CP_1 CP_2 and CP_3. Because of the slight time delay in each SEAC stage and the overlap of successive clock phases, it is possible to send the output of a stage clocked with CP_1, for example, into the input of a stage clocked with CP_2 without the use of delay lines. Furthermore, three stages of gating may be done with only a 1-μsec delay. This is especially helpful in those parts of the machine where the time available to accomplish the necessary number of logical operations is limited. Fig. 13 shows how the clock pulse is inserted into each and-gate.

A problem closely related to that of timing is that of pulse reshaping so that the input signal on the amplifier grid is essentially a clock pulse. This may be accomplished by making sure that the incoming signals to any stage overlap both the leading and trailing edges of the particular clock phase used. Since the incoming pulses will certainly be no broader than the clock pulses that produced them, delay lines may be used to achieve the necessary overlap. The method known as regeneration, which was devised shortly before the computer construction program began, accomplishes the same result without delay lines. All that is necessary in this method is that the pulses into a stage overlap the leading edge of the clock pulse. The positive output of the transformer is fed back as one of the inputs of the stage, and thus the pulse is held up until the trailing edge of the clock terminates it. The regeneration line is shown near the top of Fig. 13.

Electrical delay lines play several important roles in the computer. They are utilized in connecting stages where the clock phases are not consecutive; where a circulating register of any given length is required, e.g., the one-word instruction register; and where a pulse requires broadening, such as when a negative signal is used in an and-gate for inhibition.

The type of delay line used most generally in SEAC is of the continuous-wound design with an external ground shield. Lines of two different impedances are used: 1,350 ohms into a single gate, and 800 ohms into two gates. The type of line used offers several advantages in this kind of computer service, viz., small space requirements, ability to be cut to exact value, satisfactory rise time for half-μsec pulses, low temperature coefficient, and low attenuation. Delay-line lengths in the computer vary from as little as 0.11 to 5.10 μsec.

One of the most frequently used circuits in any digital computer is the familiar Eccles-Jordan flip-flop. Its counterpart in the SEAC type of circuitry is called the dynamic flip-flop. This is not a flip-flop in the usual sense. Whereas the output of a conventional circuit has one of two dc levels, the dynamic flip-flop output is considered to be in the "one" state when its output is a series of half-μsec pulses and in the "zero" state when in the unpulsed condition.

The regular gating stage can be connected so as to become a dynamic flip-flop by returning the positive output of the transformer to the input through a delay line. By making the delay around the loop 1 μsec, there will be produced a continuous train of pulses until turned off. Only two and-gates plus a regeneration gate are required. The first gate can turn on the flip-flop with a single pulse, and the second gate serves as the recirculation path. The latter gate must also contain an inhibitor input to turn off the stage when desired.

While the functions of a given chassis can be traced by using a detailed circuit diagram, this is often extremely arduous because of the maze of signal leads, resistors, tubes, and the like. A set of easy-to-follow symbols was developed during the preliminary period of computer design. These are shown in Fig. 14. Since a tube is always associated with a transformer, a single symbol is used to denote both. A small circle indicates a negative output. Gates are symbolized by a closed semicircle with the arc indicating the output side, thus eliminating the necessity for an arrow. And-gates are distinguished from or-gates by allowing the input lines to come up to the semicircle in the first case and through the semicircle in the second case. Negative pulse inputs are again indicated by a small circle. Delay lines are symbolized by rectangles with the actual delay period indicated in the box. Fig. 15 shows how these symbols are used in the logical diagram of the dynamic flip-flop just described.

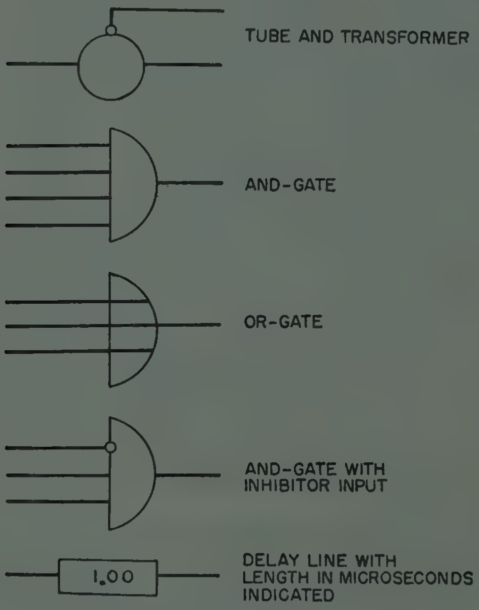

TUBE AND TRANSFORMER
AND-GATE
OR-GATE
AND-GATE WITH INHIBITOR INPUT
1.00
DELAY LINE WITH LENGTH IN MICROSECONDS INDICATED

Fig. 14—Logical symbols used in SEAC.

Several advantages, some obvious, have resulted from the use of a uniform circuit design. The fact that it allowed concentrated effort on a single type of stage has already been mentioned. Another advantage is that only one tube type is used, and tube selection is based on a single wide specification. The acceptable limits on plate current are 25 to 50 ma, with zero grid bias and +62 volts on the screen and plate. These limits apply when checked with 5.7 volts on the filament as well as with 6.3 volts. A tube is also rejected if there is an abnormal plate current variation when checked at the two filament voltage levels.

All diodes in SEAC are subject to the same specification, which for initial installation permits only 250 μa back current at 40 volts and 2 volts forward drop at 20 ma. Before a diode is removed the back current may increase to 500 μa.

It is possible to use unshielded wiring for distances up to 40 or 50 feet without encountering trouble from noise because of the low effective impedance of the circuits. When the stage is pulsed, the tube-transformer combination presents a low impedance. During the non-pulsed condition it is the forward resistance of the −8-volt clamping diode that furnishes the low impedance.

Physical Construction

Some of the over-all aspects of the physical construction of SEAC may be of general interest. The frame of the computer consists of two rows of nine standard relay racks (18 in all) with a walkway between. This arrangement does not include the mercury memory and the input-output equipment. When the computer was first put into operation, many of the racks were unfilled. This fitted in with the experimental nature of the machine and allowed for the expansion that was contemplated. At the present time the racks are completely filled by the additions that have since been made. On the interior all plug-in components are easily accessible, as are the interconnections between chassis. On the exterior all chassis wiring, resistors, and tubes are also readily available. Thus any point on any chassis can be easily inspected either visually or electrically by means of oscilloscope or voltmeter. The accessibility is such that much of the early modification of circuits was done with the chassis in place.

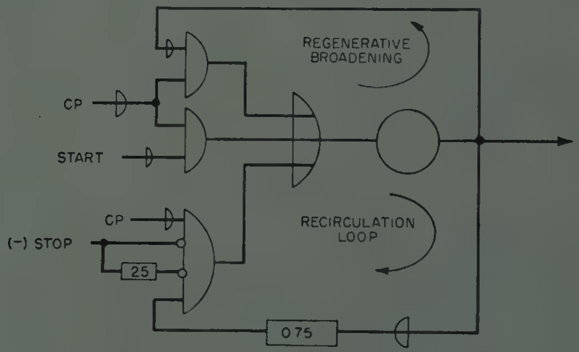


Fig. 15—Logical diagram of dynamic flip-flop.

Each relay rack has, on the average, four chassis of varying size. Filament and dc power are made available at the bottom of each rack, where each line is fused individually. Power is transmitted from one chassis to another merely by plugging each chassis into the one below it.

The three-phase clock system is distributed in much the same manner as the dc power. Phasing controls and shaping circuits are provided on each rack for the individual clock phases. The shaping circuits are parallel LC combinations located at both top and bottom of the rack to help maintain proper sine-wave form.

All signal outputs sent from one chassis to another are first terminated on a connector strip made especially for this purpose. This terminal strip is a rectangular piece of thin bakelite on which are mounted pins similar to those used on an octal base, except that they are made available on both sides. For interchassis wiring, flexible insulated wire is used. Small female connectors that fit the pins on the terminal strip are mounted on either end.

Although the mechanical arrangement of components is not the same for all SEAC chassis and reflects the change in ideas that occurred during construction, the majority follow certain practices. Fig. 16 shows both sides of a typical chassis. It will be noticed that tubes, resistors, and wiring are all located on one side, and the other components are on the other side. Everything except resistors and wiring is plug-in, and so is easily replaced.

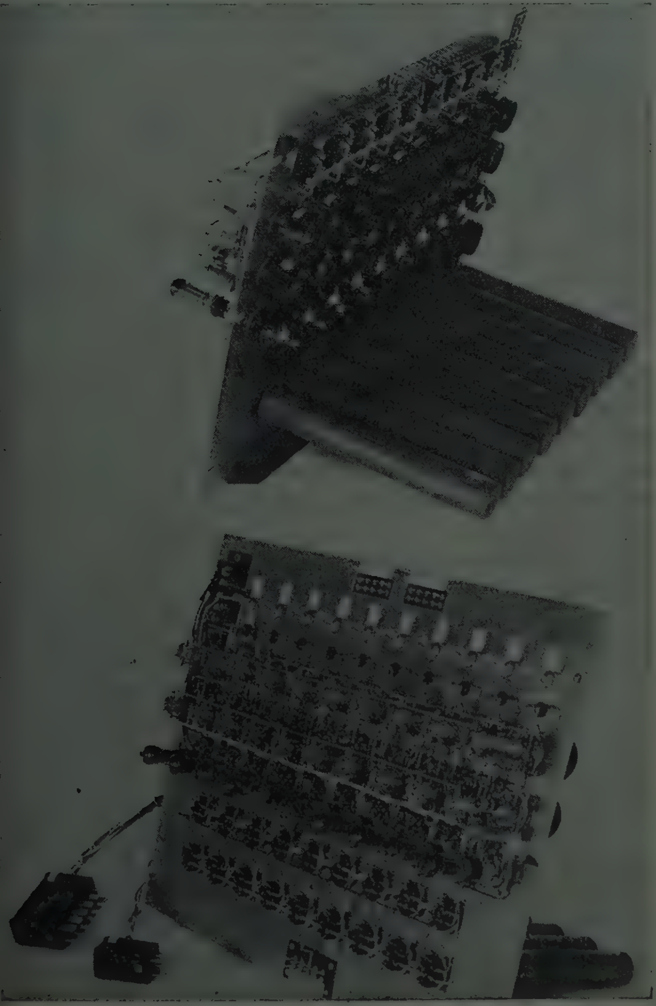


Fig. 16—View of both sides of typical chassis.

The chassis is essentially two-dimensional although the use of turrets and plug-in components gives a certain amount of depth to the construction. This is achieved without any appreciable loss of accessibility which is one of the main advantages of the two-dimensional layout. Placing tubes and resistors on one side of the chassis and all other components on the other side separates the principal heat-generating elements from the heat-sensitive components, the most sensitive of which are the germanium diodes.

The plug-in components consist mainly of pulse transformers, electrical delay lines, and germanium diodes. Their construction is similar in that all use octal tube bases with solder-dipped connections. In Fig. 16 the first, second, and fourth rows are the diode clusters mounted in octal tube bases. The components in the third row are pulse transformers mounted in similar tube bases. The bottom row contains plug-in delay lines. These are made from a long length of delay line cut into sections of approximately the right length, which are then tailored to the desired value. When the electrical length of the delay line is not more than about 2 μsec, the line can be mounted in an octal tube base and covered with a protective bakelite tube. Longer lengths of line are coiled in aluminum containers for mounting on the chassis. A more detailed view of typical plug-in units is shown in Fig. 17. The diode clusters, which comprise the majority of the plug-in units, consist of from four to seven germanium diodes connected in a variety of ways. By restricting the number of diodes in a cluster to seven, each diode can be checked individually in the unit. Since there are over 20 different types, there is sufficient choice to permit the straightforward layout of gating circuitry. When a cluster is rejected from the machine because of diode deterioration, the cluster is salvaged and only the bad diode (or diodes) is replaced.

Depending on their use, transformers are made with several different primary inductances and primary-to-

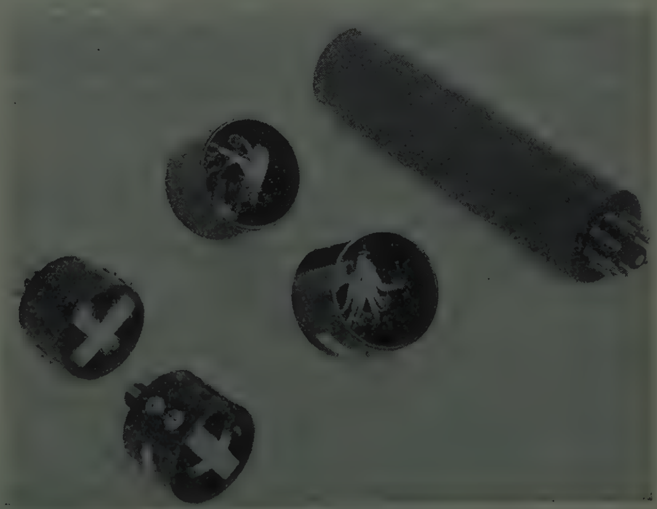


Fig. 17—Typical plug-in units.

secondary turns ratios. Originally transformers were potted with a high-temperature wax compound, but later they were bracket-mounted to permit air cooling.

OPERATING PERFORMANCE

During most of its three years of operation thus far, SEAC has been in use 24 hours per day, 7 days a week. Regularly scheduled computation comprises the bulk of the 168-hour week, with smaller amounts given to routine maintenance and experimental engineering. During routine maintenance periods a continuing check of tubes and diodes is made such that all tubes are checked every three months and all diodes every six months. In addition, a system of marginal checking is used in which several of the more sensitive gating voltages are shifted up and down. Simultaneously, standard test routines are run and the point at which failure occurs is noted. Any poor tolerances that show up are investigated further. Several other items which are checked during the weekly maintenance period are:

1. phasing of 1-mc clock on each rack,
2. mechanical adjustment of teletype equipment,
3. gain of mercury memory recirculation amplifiers and
4. condition of magnetic tapes.

A fair-sized library of routines has been accumulated for checking the mercury memory and various specific machine operations. However, except when unusual difficulties arise, use of two standard test routines is sufficient. One of these checks the memory for its ability to store several different pulse patterns; the other checks the ability of the arithmetic unit to perform the various operations. When an error occurs in either routine, the operator can usually diagnose the trouble by analyzing the information printed out.

In a machine as complex as any of the modern digital computers the operator should be given, in procedure or machine facilities, any aid possible in checking codes and running problems. One of the procedures that has been used to great advantage with SEAC is summing of the memory. For example, after every read-in from magnetic wire, the machine is used to sum the information read-in, after which the sum is compared with the known correct one. This enables the operator to know immediately whether or not the information has been correctly transferred into the memory.

The use of the sign in the instruction code to halt the computer has already been described. By manipulating one of the switches on the control console, the halt action can be modified in such a way as to help the operator check new codes. On one switch position the machine halts on all negative instructions, on the second position the machine halts only on negative print instructions, and on the third position the machine ignores all coded halts. If the operator uses negative instructions at strategic points (breakpoints), he can more quickly check the accuracy of his coding. Once the code is proved he can then eliminate these breakpoints merely by throwing a switch, without any necessity for changing his code.

Another valuable operator aid is the automonitor feature. The action of printing out the instruction, the result of the operation, and the counter contents is particularly useful when checking out a new code. The operator can set the automonitor switch so that all instructions are monitored or so only negative instructions are monitored. If a code does not work the first time it is tried, the operator can automonitor the breakpoint instructions. By examining the information printed out, he can determine between what two points in the code the trouble occurred. He can then monitor all instructions between the two points and thus determine the exact point at which the program is in error.

The speed of various arithmetic operations in SEAC is given in Table II. This is broken down by acoustic and electrostatic memories.

TABLE II

Operation	Time for Complete Operation Including Access Time (in msec)			
	Acoustic Memory			Electrostatic memory
	Max.	Min.	Avg.	
Addition	1.54	0.19	0.86	0.24
Subtraction	1.54	0.19	0.86	0.24
Comparison	1.20	0.19	0.70	0.19
a. algebraic				
b. absolute				
Logical transfer	1.54	0.19	0.86	0.24
Logical multiplication	1.54	0.19	0.86	0.24
Multiplication	3.65	2.30	2.98	2.35
a. major part, unrounded				
b. major part, rounded				
c. minor part				
Division	3.65	2.30	2.98	2.35
Base	1.20	0.19	0.70	0.19
File	0.86	0.19	0.52	0.24
Clear	1.54	0.19	0.86	0.24

An article on SEAC would be incomplete without some mention of the computation performed since the machine went into operation. During the past three years hundreds of problems covering a wide range of applications have been run on SEAC. A list of broad categories of problems with a few examples in each category follows:

1. Mathematics and statistics:
    (a) Table of Jacobi Elliptic functions for real arguments.
    (b) Solution of partial differential equations by Monte Carlo method.
    (c) Generation of optimum sampling plans for the Bureau of the Census.
2. Physics problems:
    (a) Crystal structure.
    (b) Relative abundance of the elements.
    (c) Wave functions for helium atom and for lithium atom.
3. Engineering problems:
    (a) Optical system design.
    (b) Synchrotron design.

   (c) Starting transient in a class C oscillator.
   (d) Transient stresses in aircraft structures.
   (e) Plastic deformation of eccentric columns.
4. Business management and economic problems:
   (a) Problems related to Air Force program planning.
   (b) Problems related to social security accounting procedures.
5. Problems of a security classified nature for the Atomic Energy Commission and the Armed Forces.

ACKNOWLEDGMENT

Building a large-scale electronic computer such as SEAC from original conception to eventual realization is of course the work of many minds and hands. The successful completion of SEAC at a point in time when its service was of urgent importance to the government was recognized by the Department of Commerce in its Award for Exceptional Service in February, 1951. This citation was awarded to the SEAC staff as a group, and makes particular reference to the individual contributions of W. W. Davis, R. D. Elbourn, A. L. Leiner, S. Lubkin, C. H. Page, J. L. Pike, R. J. Slutz, J. R. Sorrels, and the authors. Special mention should also go to H. Senf and W. Martin for valuable contributions in the early phase of the NBS computer program.

Electronic Circuits of the NAREC Computer*

PAUL C. SHERERTZ†

Summary—**This paper describes several of the circuits developed at the Naval Research Laboratory for its electronic digital computer, the NAREC. These circuits, which include inverters, flip-flops, counters, steppers, pulse generators, adders and comparators, employ crystal diodes where practical for all non-linear functions and use vacuum tubes only where inversion or amplification is required. All circuits are designed to provide low impedance output signals whose maximum and minimum levels are held to prescribed dc potentials. The circuits are packaged in standard 4-tube plug-in chassis in arrangements which make these units functional building blocks of the computer.**

INTRODUCTION

THE NAREC[1] is an electronic digital computer currently being placed in operation by the Naval Research Laboratory. The machine is designed to perform several thousand mathematical operations per second on 11 decimal digit (44 binary digit) numbers, operate in the parallel mode and may be asynchronously controlled to operate at any speed up to its maximum. Cathode-ray tubes and a magnetic drum are employed for high and low speed storage respectively. Information is read into and out of the computer from or to magnetic tape, punched paper tape, or automatic electric typewriters.

A diagram of the computer layout is shown in Fig. 1. Physically, the main frame is divided into the *left* or control section, the *middle* or arithmetic section, the *right* or input-output section and the *bottom* or electrostatic storage section. The magnetic drum is located to the right of the main frame, and a control console is located in front of the *middle* section. Circuit packages are designed to plug in from the front of the frame and are interconnected by horizontal and vertical busses on the back of the frame.

As can be seen from the block diagram of Fig. 2, the major portion of the computer is devoted to the task of either storing or transferring numbers. Addition is the only basic mathematical function performed by the computer. Negative numbers are expressed in binary complementary form and subtraction is performed by the addition of negative numbers. Multiplication, division and all other operations are accomplished by a series of shifts and additions or subtractions. Comparators are used to check the transfers between registers and to halt computation when an error is made in the process of a transfer.

The physical realization of the NAREC has resulted in the design of a complete family of digital circuit elements whose inputs, outputs, and constructional features were tailored to the same standards. These devices include gating circuits, vacuum tube registers, pulse generators, stepping elements, counters, parallel adders, inverters, comparators and signal drivers. This report will describe the basic circuits developed for all functions except electrostatic and magnetic storage.

At the time that the electronic design of the NAREC computer was initiated, the following rules were adopted to guide the circuit development:

(a) Where practical, circuits should be designed for dc operation and aperiodic triggering.
(b) Output signal levels should be high enough to permit checking by indicator lights and simple dc measurements.
(c) Crystal diodes should be used in place of vacuum tubes whenever a substantial saving of space or power could be anticipated.
(d) Circuits should be designed to operate at the maximum rate obtainable without the use of complex circuits or heavy duty tubes.
(e) A minimum number of tubes should be used and, where practical, these should be restricted to the

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 1, 1953.

† Operational Research Branch, Radio Division III, Naval Research Laboratory, Washington 25, D. C.

[1] D. H. Gridley and B. L. Sarahan, "Design of the Naval Research Laboratory Computer," *Elec. Eng.*, vol. 70, p. 111; February, 1951.

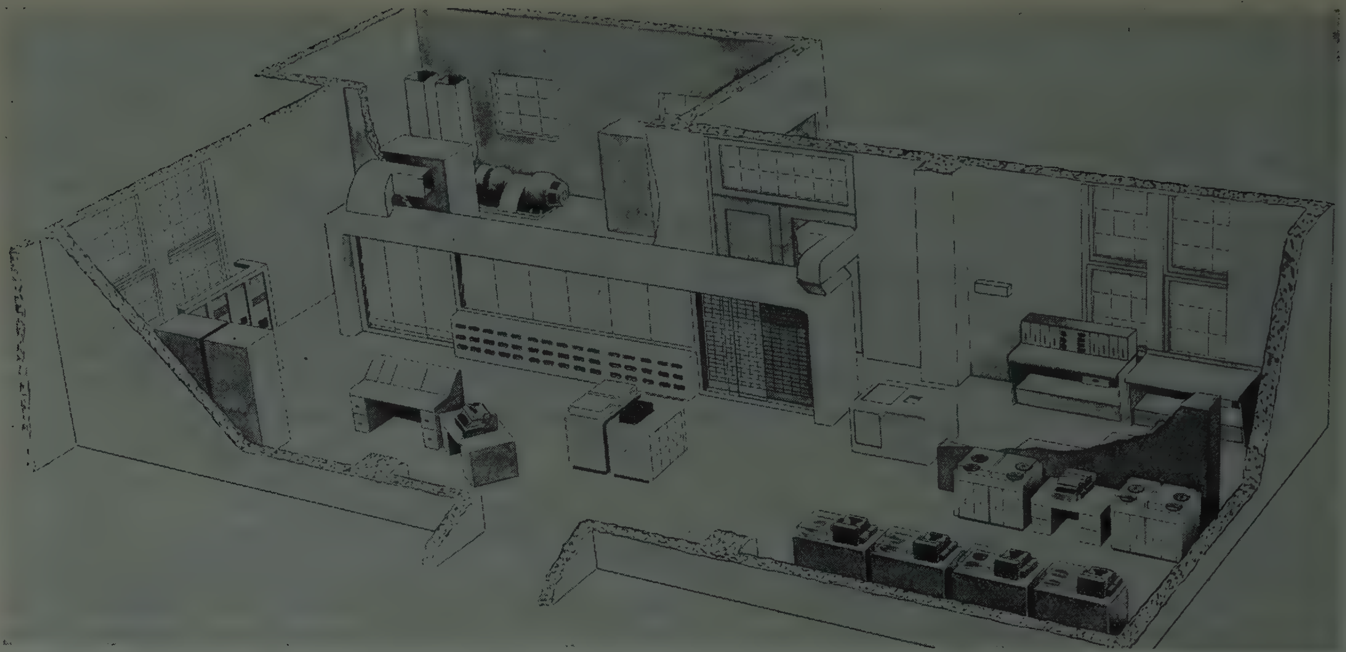


Fig. 1—The NAREC installation.

5670 (or 2C51) and the 5687 dual triodes, and the 6AN5 power pentode.

(f) Circuit design should allow component tolerances of at least five per cent.

(g) Circuits should be designed for plug-in operation.

(h) The outputs of plug-in units should be capable of driving signals with a few-tenths-of-a-microsecond rise time for distances up to 20 feet over open wires without appreciable attenuation.

(i) Plug-in units should contain such circuits as necessary to make the unit a functional building block of the computer.

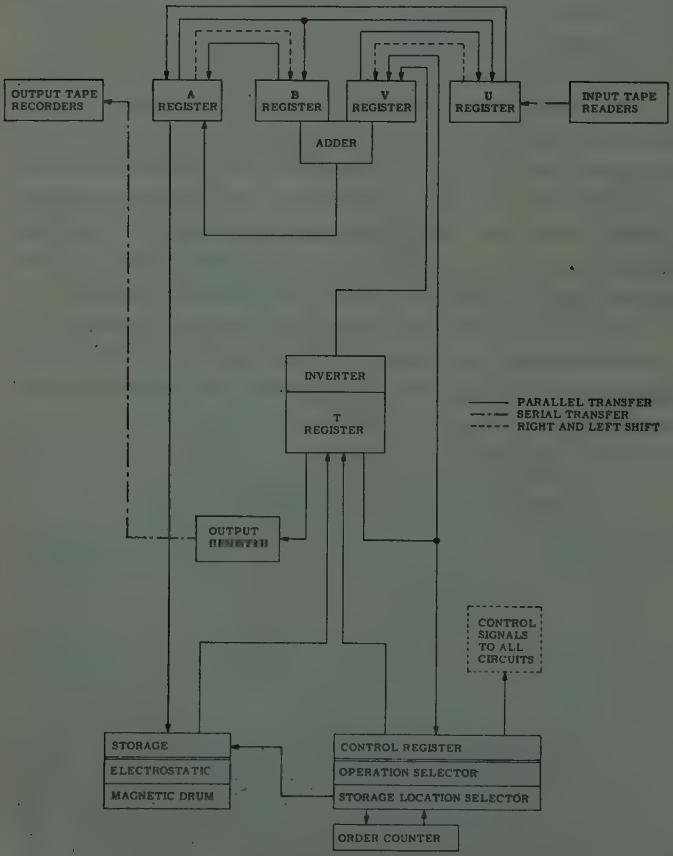

OUTPUT TAPE RECORDERS
A REGISTER
B REGISTER
V REGISTER
U REGISTER
INPUT TAPE READERS
ADDER
INVERTER
T REGISTER
PARALLEL TRANSFER
SERIAL TRANSFER
RIGHT AND LEFT SHIFT
OUTPUT REGISTER
CONTROL SIGNALS TO ALL CIRCUITS
STORAGE
ELECTROSTATIC
MAGNETIC DRUM
CONTROL REGISTER
OPERATION SELECTOR
STORAGE LOCATION SELECTOR
ORDER COUNTER

Fig. 2—Block diagram of the NAREC.

The decision to place all electronic circuits on plug-in frames resulted from the view that the servicing of the computer as a whole should consist in locating and replacing faulty units rather than individual faulty components. Thus, the reason for using plug-in units is to speed and simplify servicing rather than to standardize on circuit elements, desirable as this may be. A review of the circuit requirements and available connectors led to the final adoption of the standard chassis shown in Fig. 3, which has a 36-terminal plug, four tubes and space for five neon indicators and 108 components. This type of unit is used for all NAREC circuits except those associated with the electrostatic and magnetic memories. Consideration was given to further subdivision of each plug-in unit into a few standard types of smaller plug-in circuit elements. However, it was decided that this would not appreciably simplify the over-all construction or service problem and might slow down the operation of the circuits by adding capacitance to sensitive signal leads.

Diode Gates

The flow of information within the computer is controlled almost entirely by means of gates. Only two basic types of gates are required to perform all logical selection functions: (1) the "*AND*" gate corresponding to series-connected switches, all of which must be closed to connect the input to the output; and (2) the "*OR*" gate corresponding to parallel-connected switches, only one of which need be closed to connect the input to the output. Logically, the "*AND*" gate indicates that, if all

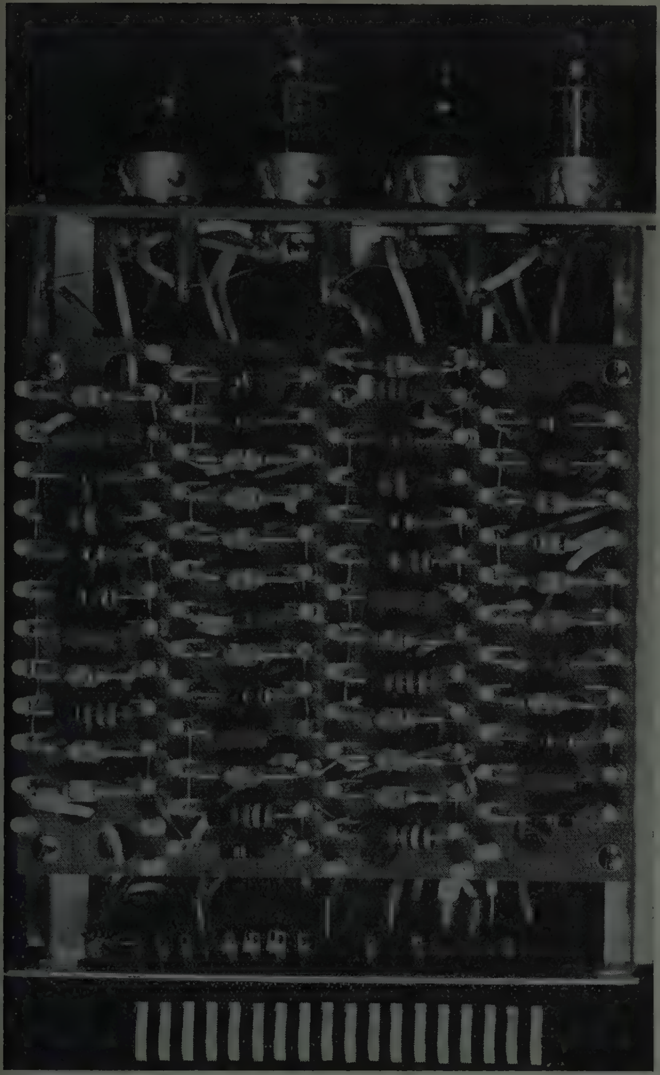
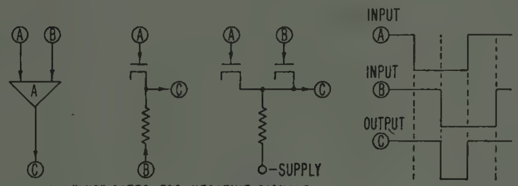


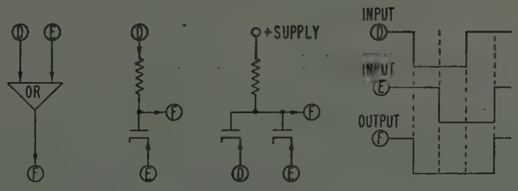
Fig. 3—The standard plug-in chassis.

its inputs (A, B, and . . .) have the value "one," its outputs will have the value "one," while the "*OR*" gate indicates that, if any of its inputs (A or B or . . .) has the value "one," its output will have the value "one." In the NAREC, diodes and resistors are used to make up the gates so that the output of a gate depends on its input potentials. A diode has low resistance when its plate is positive with respect to its cathode, and high resistance when its plate is negative with respect to its cathode. Consequently, in the circuits of Fig. 4(a), the output is held to the more positive of the two input signals A and B, while in the circuits of Fig. 4(b) the output is held to the more negative of the two input signals. The circuits of Fig. 4(a) are indicated symbolically as "*AND*" gates and those of Fig. 4(b) as "*OR*" gates because in the majority of the NAREC circuitry a negative potential represents the value one and a positive potential the value zero.

Crystal rather than vacuum diodes are used in the NAREC for gating and other non-linear functions (such as voltage limiting) that are suited to their characteristics. All crystals used in NAREC circuits were selected to have reverse currents of 0.25 ma or less at 50 volts, negligible drift characteristics and forward resistances of approximately 100 ohms. In the initial design phase of the NAREC it was decided to limit signal amplitudes to a maximum of 50 volts, corresponding to the rated reverse voltage of the crystals, and to a minimum of 30 volts, corresponding to the minimum voltage that would reliably operate a neon indicator. In general, arithmetic circuits such as the registers, adders, comparators and counters were designed for operation with 30-volt signals, while control circuits such as steppers, pulse generators, inverters and drivers were designed with 50-volt signals.



(a) "AND" GATES FOR NEGATIVE SIGNALS



(b) "OR" GATES FOR NEGATIVE SIGNALS

Fig. 4—Diode gates.

Vacuum Tube Circuits

The liberal use of crystal diodes makes it possible to restrict the use of vacuum tubes to functions requiring inversion, voltage amplification, power amplification, or storage. As illustrated in Fig. 5, these functions are ordinarily obtained from triodes connected as inverting amplifiers or cathode followers. The typical NAREC circuit employs dc coupling of high-impedance gate or amplifier outputs to the grid of a cathode follower. Since the cathode follower has a high impedance input and a low impedance output, the amplifier triode may be operated at low currents and voltages in a manner that allows efficient dc coupling without sacrificing high frequency response.

The circuit actually used in the inverter units of the NAREC is shown in Fig. 6. In this circuit the plate load resistor of the amplifier tube is coupled to the positive supply voltage but is limited in its maximum positive excursion to +30 volts by means of diodes. This arrangement permits more rapid response, heavier loading of the cathode follower and higher signal levels for a given current through the amplifier tube, than can be obtained by returning the amplifier plate load resistor directly to +30 volts. The output signal is also limited to a maximum negative excursion of −20 volts by a diode directly on the output bus. For use in the com-

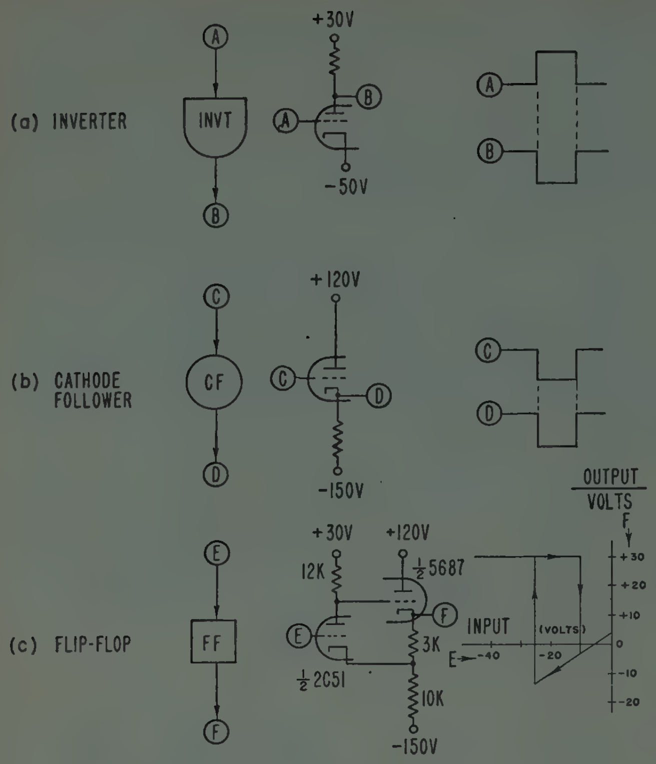

(a) INVERTER
A
INVT
B
+30V
-50V
(b) CATHODE FOLLOWER
C
CF
D
+120V
-150V
(c) FLIP-FLOP
E
FF
F
+30V
+120V
12K
½5687
½2C51
3K
10K
-150V
OUTPUT VOLTS
INPUT
(VOLTS)
-40
-20
+30
+20
+10
0
-10
-20

Fig. 5—Basic vacuum tube circuits.

puter, four inverter circuits are packaged in a plug-in unit along with a set of input gates which, by appropriate cross connections on the back of the plug, may be used with any one of the inverters or some other unit.

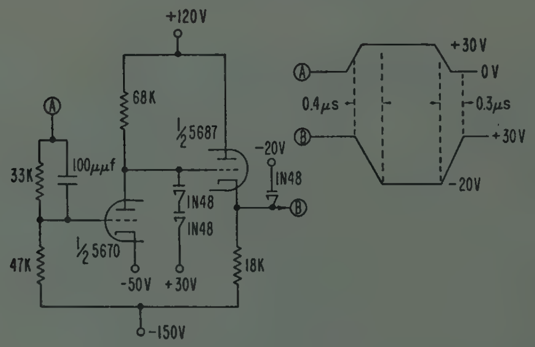

+120V
68K
33K
100μμf
½5687
½5670
47K
1N48
1N48
-20V
1N48
18K
-50V
+30V
-150V
A
B
+30V
0V
0.4μs
0.3μs
+30V
-20V

Fig. 6—Inverter circuit.

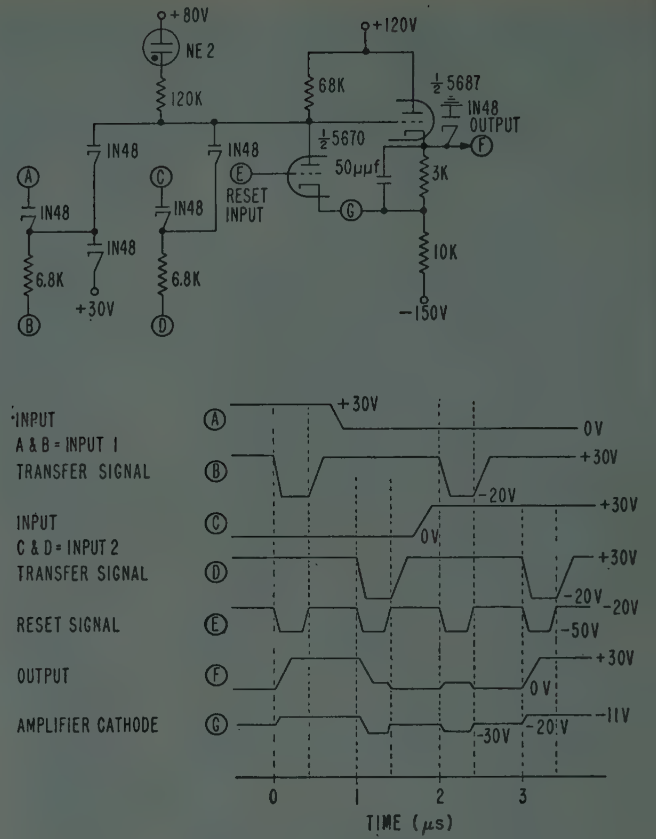

+80V
NE2
120K
+120V
68K
½5687
1N48
OUTPUT
F
1N48
1N48
½5670
50μμf
3K
E
RESET INPUT
G
A
1N48
C
1N48
1N48
6.8K
6.8K
+30V
B
D
10K
-150V
INPUT A & B = INPUT 1 TRANSFER SIGNAL
INPUT C & D = INPUT 2 TRANSFER SIGNAL
RESET SIGNAL
OUTPUT
AMPLIFIER CATHODE
+30V
0V
+30V
-20V
+30V
0V
+30V
-20V
-20V
-50V
+30V
0V
-11V
-30V
-20V
0
1
2
3
TIME (μs)

Fig. 7—Schematic diagram of a flip-flop with two input gates.

The most commonly used electronic elements in the NAREC are the single binary digit storage circuits or flip-flops that make up the arithmetic registers. One of these circuits with two input gates, which allow it to be set to the level of either of two input signals, is shown in Fig. 7. The flip-flop itself differs from the basic circuit in that the amplifier plate resistor is returned to the positive supply voltage and that diodes are used to limit the output level to a maximum of +30 volts or a minimum of zero volts. The waveforms included with the schematic diagram illustrate the transfer of information alternately from the two inputs to the flip-flop output. When a transfer is made, a negative reset signal cuts off the amplifier triode and a transfer signal simultaneously connects the plate of the amplifier with a particular input through the gates. If the input signal is at +30 volts, the amplifier plate is drawn to +30 volts as soon as the reset signal is applied and remains there when the transfer and reset signals return to their quiescent levels. On the other hand, if the input signal is at zero volts, the transfer signal applied to the input gate holds the amplifier plate to zero volts until after the reset signal has subsided, and the flip-flop output is left at the zero-volt level. For use in the NAREC registers, four flip-flops are packaged in a single plug-in unit together with a total of twenty input gates which permit the transfer of information from five sources into each of the four flip-flops.

The flip-flop can be used as the vacuum tube element of circuits such as counters, steppers, or pulse generators through the addition of appropriate triggering and gating circuitry. Fig. 8 shows a block diagram of a four-stage binary counter and the waveforms of the first two stages. Each counter stage consists of a flip-flop which can be set either positively or negatively by positive rising signals applied to the "set +" or "set −" inputs respectively. The circuitry is so arranged that the "set +" signal overrides the "set −" signal when both are simultaneously present. An "*AND*" gate is used to prevent the "set +" input of the flip-flop from receiving a signal until both the input signal and the flip-flop output are negative. Thus with the flip-flop initially positive, the first positive input pulse will set the output negatively by means of the "set −" signal and the second positive input pulse which reaches both

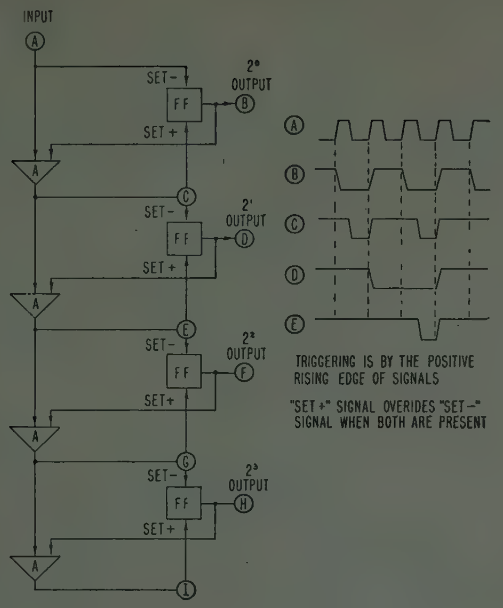

INPUT
A
SET −
SET +
FF
2⁰ OUTPUT
B
C
2¹ OUTPUT
D
E
2² OUTPUT
F
G
2³ OUTPUT
H
I
TRIGGERING IS BY THE POSITIVE RISING EDGE OF SIGNALS
"SET +" SIGNAL OVERIDES "SET −" SIGNAL WHEN BOTH ARE PRESENT

Fig. 8—Binary counter block diagram.

the "set −" and "set +" inputs, will set it positively. To minimize delays in the triggering of successive counter stages, the "set +" signal for one counter stage is also used as the input signal for the following stage. Through this arrangement, each counter in a chain is triggered simultaneously by the rise of the input signal and no cumulative delay occurs.

A binary counter stage operating according to the principles outlined in the block diagram of Fig. 8 is shown schematically in Fig. 9. The flip-flop of the counter is alternately set negatively and positively by positive pulses derived from the positive-rising-edge of the input signal and applied respectively to the grid and cathode of the amplifier triode. The impedances of the "set −" and "set +" trigger circuits are such that the flip-flop will be set positively by the "set +" signal despite the simultaneous presence of a "set −" signal. The maximum counting rate of this type of counter is largely determined by the time constant of the "set +" circuit, and is about one megacycle for the circuit shown. For use in the NAREC, four counter stages are packaged in a single plug-in unit and are connected as indicated in the block diagram so there is no cumulative delay between stages, the delay for any of the four stages being 0.25 microsecond.

A circuit which may be used either as a stepper or as a pulse generator is illustrated in Fig. 10. In principle at least, the circuit is very simple, the flip-flop being set negatively by positive signals applied to the grid of the amplifier triode and set positively, either by the introduction of a negative signal to the amplifier grid, the discharge of a condenser, or a positive signal to the cathode of the cathode follower. When used as a pulse generator, diodes X1, X2, and X5 are biased in a manner that effectively eliminates them from the circuit. In the quiescent state, the amplifier triode is cut off by the biasing arrangement which holds the grid about four volts negative with respect to the cathode. Introduction of a positive signal to the small input condenser, C1, causes current to flow in the amplifier triode and sets the flip-flop to its negative state. A second con-

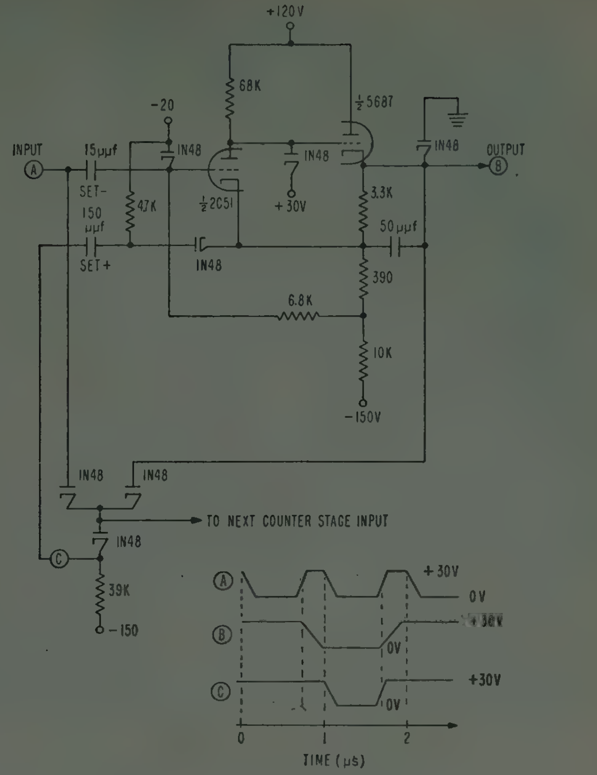

+120V
68K
−20
½ 5687
INPUT
A
15 μμf
1N48
SET −
150 μμf
SET +
47K
½ 2C51
+30V
3.3K
50 μμf
390
6.8K
10K
−150V
OUTPUT
B
TO NEXT COUNTER STAGE INPUT
C
39K
−150
+30V
0V
TIME (μs)
0
1
2

Fig. 9—Binary counter circuit.

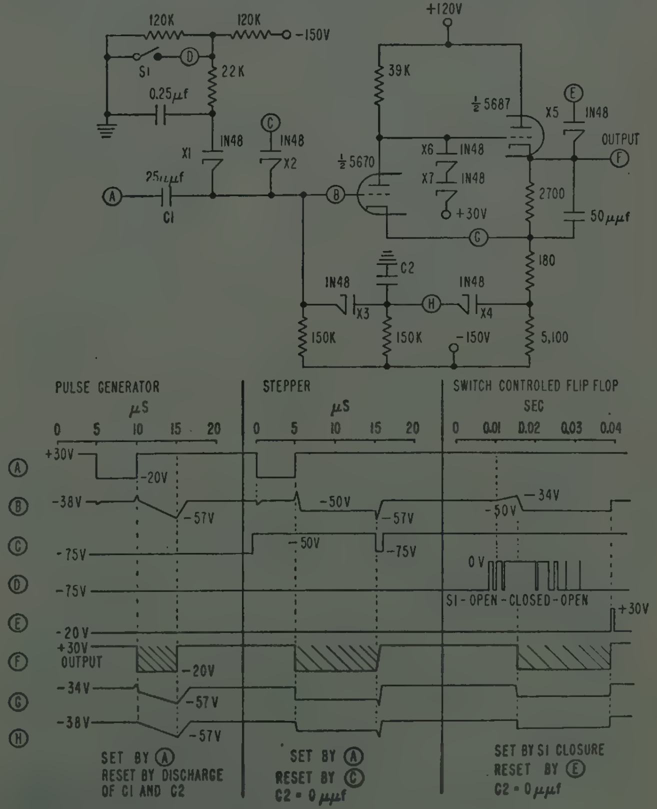

120K
120K
−150V
+120V
S1
D
22K
0.25 μf
39K
½ 5687
X5
E
1N48
OUTPUT
F
X1
X2
25 μμf
A
C1
½ 5670
B
X6
X7
+30V
2700
50 μμf
G
C2
180
X3
X4
H
150K
150K
−150V
5,100
PULSE GENERATOR
STEPPER
SWITCH CONTROLED FLIP FLOP
μS
SEC
+30V
−20V
−38V
−57V
−50V
−34V
−75V
0V
S1 - OPEN - CLOSED - OPEN
−20 V
+30V OUTPUT
SET BY A
RESET BY DISCHARGE OF C1 AND C2
SET BY A
RESET BY C
C2 = 0 μμf
SET BY S1 CLOSURE
RESET BY E
C2 = 0 μμf

Fig. 10—Pulse generator or stepper circuit.

denser, C2, whose value is chosen to give the desired pulse length, is coupled to the grid of the amplifier triode through a diode, X3. The positive triggering signal is unimpeded by the capacitance of C2 because of the high reverse impedance of X3; however, when the circuit flips to the negative state, the amplifier grid can drop negatively and cut off the triode once more only by discharging both C2 and C1. When the flip-flop has reset to positive state, both condensers C1 and C2 are rapidly recharged by diodes X3 and X4 and low impedance resistance divider in cathode follower output.

In the usual use of the circuit of Fig. 10 as a stepping circuit, C2 is removed, a normally −50 volt "shift" signal is applied to the plate of diode X2, and diodes X1 and X5 are biased to cut off. The flip-flop is triggered negatively by a positive rising signal applied through C1 to the grid of the amplifier triode. Once its output is in the negative state, the flip-flop will not reset because the grid of the amplifier triode is prevented from dropping below −50 volts by the limiting action of diode X2. When it is desired to set the flip-flop positively, the "shift" signal input to this diode is dropped negatively for a time sufficient to permit the discharge of C1 and consequently the resetting of the circuit. If the stepper is part of a ring counter composed of several similar circuits, the output of one circuit (F in Fig. 10) is connected to the input of the next (A in Fig. 10), and the reset or "shift" inputs (C in Fig. 10) of all circuits are connected in parallel. Under this condition a "shift" signal must be long enough to reset a stepper originally in the negative condition, but not long enough to reset a stepper which is triggered to the negative condition during the interval of the "shift" signal. For the circuit illustrated, the "shift" signal should be approximately 0.7 microsecond.

To control the computer it is necessary to transfer information from switches into flip-flops and other circuits. Although this would seem an elementary function, it is complicated by the fact that most switches have appreciable bounce which may last several hundredths of a second. Fig. 10 illustrates one method by which a noisy switch may be made to set a flip-flop. When switch S1 is closed, the input grid of the amplifier triode is raised positively until the circuit is flipped to the negative state. Once triggered, the circuit is held in the negative condition by the signal (−50 volts) applied to the plate of diode X2, despite opening of the switch. Resetting of the flip-flop may be accomplished by raising the level of the potential applied to the plate of diode X5 from −20 volts to +30 volts, or by dropping the potential on diode X2 from −50 to −75 volts.

Aside from the specialized memory and input-output circuitry, the only vacuum tube device in the NAREC which does not employ a dc coupled amplifier, and/or a cathode follower arrangement, is the amplifier driver shown in Fig. 11. The circuit forms the "transfer" and "reset" pulses required to transfer information into flip-flop registers and the "shift" pulses required to step information in stepper circuits. According to the load used, a single amplifier driver stage is capable of resetting 24 flip-flop register stages, driving 16 register input gates, or shifting the count in a 20-stage ring counter. In effecting the transfer of information between registers, a single pulse is applied to two amplifier drivers, one of which is connected as a "reset" driver, and the other as a "transfer" driver. The "transfer" driver output pulse is caused to lag the output pulse of the "reset" driver by removing the condenser, C1, from the input of this circuit.

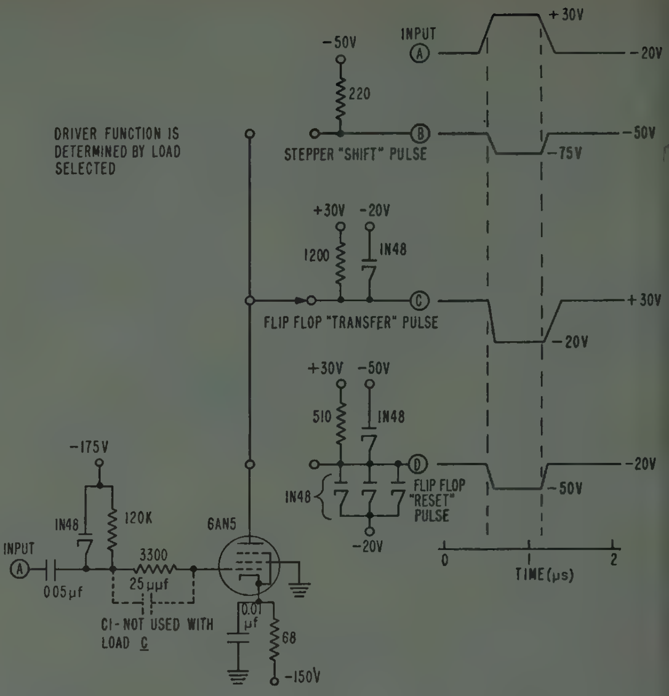


Fig. 11—Amplifier driver circuit.

Logical Circuits

All of the circuits which have been discussed are constructed on the standard plug-in unit illustrated in Fig. 3. In general, four similar circuits such as flip-flops, inverters, or counters are packaged in a single unit together with such input gating as is required by the NAREC logic and permitted by the available plug connections. A few of the units, however, contain a combination of gates and circuits to modify the input signals according to a particular logic. Three of these circuits, namely the comparator, adder and activator, will be discussed to illustrate the use of gates for controlling circuit operations and to indicate the type of circuit building block formed by a plug-in unit.

A block diagram of a comparator is shown in Fig. 12. Comparison of A against B is made according to the logic that if A *and* B are both negative *or* if A *and* B are both positive, the output of the circuit will be negative. If either A is positive and B negative, or A negative and B positive, the output of the circuit will be positive. Similar comparisons are made for all signal pairs which must be compared and the outputs of all comparators

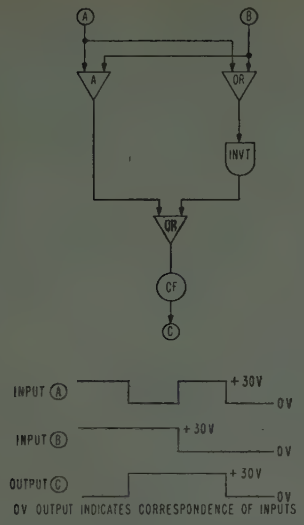

A
B
A
OR
INVT
OR
CF
C
INPUT A
INPUT B
OUTPUT C
+30V
0V
+30V
0V
+30V
0V
0V OUTPUT INDICATES CORRESPONDENCE OF INPUTS

Fig. 12—Comparator block diagram.

are connected in parallel. By this arrangement the output cathode followers act together as a large *"AND"* gate and give a negative output signal only if all signal pairs correspond.

A block diagram of the NAREC adder unit is shown in Fig. 13. This unit contains two logically similar dc coupled parallel adders, the second of which amplifies the output carry signal. The first stage adds the inputs A1, B1, and C1 and develops the digit output D1 and the carry output C2 according to the rules of binary addition. A positive potential, nominally +30 volts, represents the binary value "zero" and a negative potential, nominally 0 volts, represents the binary value "one." The gating is arranged so that the carry output C2 will be "one" if [A1 and C1] or [(A1 or C1) and B1] equal "one," and the digit output D1 will be "one" if [A1 or C1 or B1 and not C2] or [(A1 and C1) and B1] are "one." The inversion of carry output C2 is the "not C2" signal. In the second adder stage, the inputs A2 and B2 are added to the carry output (C2) of the first stage to give the digit output D2 and the carry output C3, according to the same logic. Carry output C3 is amplified by means of a double inverter stage to eliminate the attenuation and bias introduced by successive cathode followers and gates. As used in the NAREC, this adder propagates the carry signal with a delay of about 0.05 microsecond per stage.

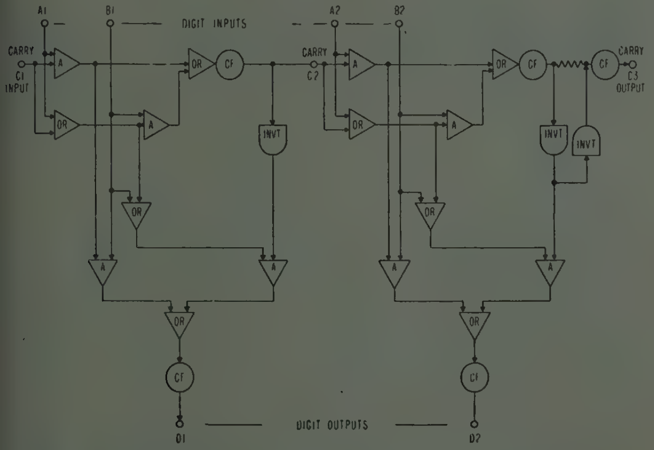

A1
B1
DIGIT INPUTS
A2
B2
CARRY
C1
INPUT
A
OR
CF
CARRY
C2
A
OR
CF
CF
CARRY
C3
OUTPUT
OR
A
INVT
OR
A
INVT
INVT
OR
OR
A
A
A
A
OR
OR
CF
CF
D1
DIGIT OUTPUTS
D2

Fig. 13—Block diagram of a two-stage, binary, parallel adder.

The various dynamic functions of the NAREC are controlled by compound circuits called activators. One activator is provided for each unique operation (such as the transfer of digits 0 to 12 in the B register to digits 24 to 36 in the A register) directed by the control section of the computer and an order such as multiplication is performed by the successive triggering of several activators. As may be seen in the block diagram of Fig. 14, an activator is basically a stepping circuit with a large number of input selection gates. A cathode follower and gated inverter stage were incorporated in the activator package because these circuits are required to supply signals at the appropriate time and levels to the drivers which actually carry out the functions specified by the activator. Since the stepper circuit of an activator is designed to be triggered by a pulse having a rise time of 0.5 microsecond or less, it is possible to prevent the selection inputs from triggering an activator by slowing their rise time to a minimum of 1.5 microseconds. When an order is to be performed, gated inverters and cathode followers controlled by the order digits of the control register interconnect a set of activators by applying negative selection potentials to one input gate on each. The first activator of the order is triggered to the negative state by a "start" signal. When its function has been performed, it is reset by a "shift" signal which is applied simultaneously to all activators. The resetting of the first activator triggers the second, and the process is continued until the order is completed.

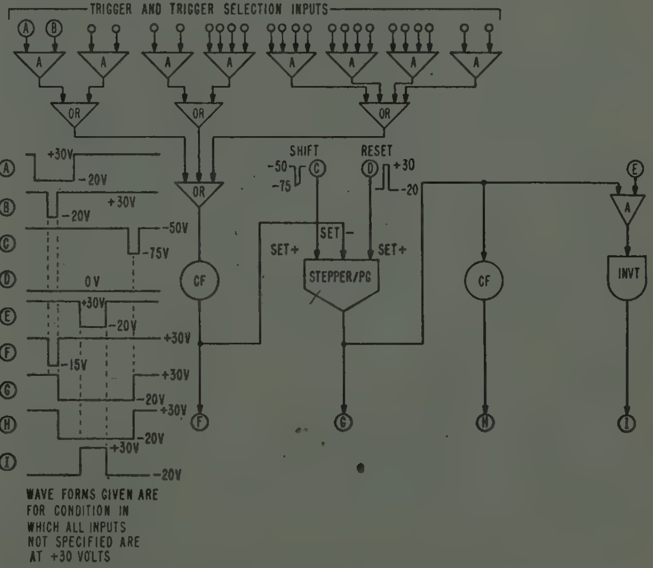

TRIGGER AND TRIGGER SELECTION INPUTS
A
B
A
A
A
A
A
A
A
A
OR
OR
OR
OR
CF
SHIFT
RESET
-50
-75
C
D
+30
-20
SET
SET+
SET+
STEPPER/PG
CF
E
A
INVT
F
G
H
I
A
+30V
-20V
B
+30V
-20V
C
-50V
-75V
D
0V
E
+30V
-20V
F
+30V
-15V
G
+30V
-20V
H
+30V
-20V
I
+30V
-20V
WAVE FORMS GIVEN ARE FOR CONDITION IN WHICH ALL INPUTS NOT SPECIFIED ARE AT +30 VOLTS

Fig. 14—Activator block diagram.

An activator specifying a particular information transfer between two registers also specifies the gating of the outputs of these registers into inputs of the comparators. The output signal of the comparator then indicates whether the transfer has been correctly made and is used to gate the "shift" pulse applied to the activators. Thus, if the two registers do not contain identical information after the transfer, no "shift" pulse will be transmitted to the activators and the computer will halt on the operation which is in error.

ACKNOWLEDGMENT

The author is indebted to J. J. Fleming and D. H. Gridley for the encouragement and helpful suggestions they have given during the development of these circuits. Much credit should be given A. B. Bligh, E. P. Brown, K. H. Folse and I. J. Levy for their assistance in all phases of the construction, testing and installation of the circuits.

Diagnostic Programs for the Illiac*

DAVID J. WHEELER†, AND JAMES E. ROBERTSON†, ASSOCIATE, IRE

***Summary*—The diagnostic programs used for maintenance of the ILLIAC, the University of Illinois' digital computer, are described. The uses of diagnostic programs for fault detection, fault isolation, and periodic computer servicing are discussed. The characteristics of the "leapfrog" program, both as a detection program and as an isolation program, are described in detail. Descriptions of one of the more complex isolation programs and of a typical servicing program are given. Pertinent characteristics of the ILLIAC and techniques of fault isolation are also included.**

INTRODUCTION

THE MAINTENANCE of an electronic digital computer presents unusual problems for the engineer.[1] A computer is a complex collection of elementary circuits. Although the repair of any individual circuit is simple, the location of the particular circuit at fault among the hundreds of faultless circuits poses a problem of major proportions.

Furthermore, the standard of reliability required is an order of magnitude greater than for other electronic apparatus. Fortunately for the engineer, the computer itself can be used as a versatile test instrument for the localization of faults.

In this paper we discuss first the pertinent characteristics and principles of operation of the Illiac. Next, we describe the typical faults which occur and the effects they have on computer operation. Finally, we discuss the use of three types of diagnostic and servicing programs which enable us to use the computer to diagnose its own troubles. These three kinds of programs answer the questions: Is the computer working correctly? Which part of the computer is at fault? How should this analogue control be adjusted?

Because persistent faults can usually be traced easily with a voltmeter, this paper is concerned mainly with intermittent faults. Refined methods are often required for intermittent faults, especially when the error rate is small.

TABLE I

CHARACTERISTICS OF THE ILLIAC

Computer type		parallel, asynchronous, general purpose
Register capacity		40 binary digits
Memory capacity		1,024 words each of 40 binary digits
Number of tubes		
Memory		900
Arithmetic unit		1,100
Control		600
Input-output		100
Total		2,700
Type of instruction		Single address, two instructions per word
Number of digits defining an instruction		8 binary digits
Number of digits defining a memory position		10 binary digits
Operation times		
Multiplication	max.	822 μsec
	min.	642 μsec
Division		772 μsec
Addition		72 μsec
Input		4 msec per character
Output (punch)		40 msec per character
Total operation time		3,000 hours[1] (approx.)
Tube failures (excluding cathode-ray tubes)		120[1] (approx.)

[1] On April 20, 1953.

CHARACTERISTICS OF THE ILLIAC

The Illiac, which was completed in September, 1952, is the second automatic electronic computer built at the University of Illinois. It is of the same general type as the Institute for Advanced Study computer at Princeton.[2] In particular, it is a parallel computer with an electrostatic Williams memory. The memory is the only synchronous part of the computer, the rest of the control being asynchronous and designed so that the completion of one operation initiates the next. The computer works internally in the binary system and has 40 binary digits

---

* Decimal classification: 321.375.2. Original manuscript received by the Institute April 27, 1953.

† University of Illinois, Engineering Research Laboratory, Urbana, Illinois.

[1] Other papers discussing the maintenance of digital computers were published in the 1953 Convention Record of the I.R.E.

[2] Descriptions of digital computers similar to the Illiac are given in: G. E. Estrin, "A description of the electronic computer at the Institute for Advanced Study," *Proc. Assoc. for Computing Machinery*, pp. 95–109, Toronto, Ontario, Canada; September, 1952; and R. E. Meagher, and J. P. Nash, "The ordvac," *Rev. Elec. Digital Computers*, pp. 37–43, 1952. (Proc. of Joint AIEE-IRE Computer Conference; December, 1951).

for a single word or number. The instructions are single-address instructions and packed two in a word. The input unit reads teletype tape by means of a photoelectric tape reader and the output unit punches teletype tape. Some of the Illiac characteristics are given in Table I.

The Illiac Memory

The memory is of the electrostatic Williams type, binary digits being stored as charge distributions on the phosphor of commercially available 3KP1 cathode ray tubes. A digit is read from the memory by sensing the appropriate charged area of the phosphor with the electron beam; the resulting potential change is electrostatically coupled to a wire screen on the outer face of the cathode ray tube and is amplified to the signal level of the logical circuits of the computer.

Such a memory is subject to a variety of faults. First, flaws in the phosphor may make storage marginal or impossible. Second, frequent consultations of one area of the storage surface may affect the digits stored in the immediate vicinity. Third, small noise signals may be generated in cathode-ray tubes or amplifier circuits, causing errors in stored data. We shall refer to these as flaws, read-around faults, and random faults, respectively.

Susceptibility of the memory to error has affected both the physical structure and the circuit design of the Illiac. Unlike the remainder of the machine, a pluggable chassis is associated with each of the forty digital positions of the memory. Three controls for each of forty cathode-ray tubes are readily available for adjustment. A separate test rack is used for preliminary selection of cathode-ray tubes and for fault isolation within a pluggable chassis.

The Arithmetic and Control Unit

Arithmetic and control units of Illiac are a complex arrangement of a few types of direct coupled logical circuits, circuits in which tubes are used in an on-off fashion. These are best described from a functional viewpoint.

In the arithmetic unit, flip-flop registers are used for number storage; gates are used for number transfers from one register to another. Numbers in two registers are added with a parallel logical adder, subtraction being carried out by using a complement. Halving and doubling is done by shifting numbers right or left. Two registers are used to perform a shift by gating from the first to the second and then back to the first with the digits displaced one position to the right or to the left. Multiplication and division are performed as sequences of additions or subtractions with shifts. Since the computer is a parallel one, corresponding circuits for each digit are activated simultaneously.

In order to localize a fault in the arithmetic unit we have to find both the digital position and circuit involved. Although an arithmetic error may be discovered as a single digit error, it does not always follow that it occurred in the indicated digital position as it may have been shifted before it was discovered.

The control circuits supervise the sequencing required in the arithmetic unit, the selection and execution of instructions, and the use of the memory. A particular circuit is identified by its function, and failures are localized by interpretation of the malfunctioning produced.

The sequencing circuits of the control are designed so that the completion of one operation initiates the next. This allows circuits to operate at their natural speeds and causes certain faults to stop the computer.

The Input-Output Unit

The Illiac is equipped with a photoelectric tape reader, a tape punch, and a teletypewriter. These input and output devices perform mechanical operations under the control of electronic impulses supplied by the computer. Faulty operation results when a mechanical part is out of adjustment.

DETECTION PROGRAMS

The maintenance engineer of an electronic digital computer must be able not only to localize faults quickly when they occur, but he must also be able to minimize the chance of faults occurring during scheduled operation time. For the latter purpose, a stringent program which thoroughly tests all parts of the computer is needed. We call such a program a detection program. The detection program is designed to exercise each component of the computer through all its possible states. Furthermore, the duty cycle has to be high enough so that all parts of the computer are tested under dynamic conditions. Certain circuits of the computer are connected to many other circuits. For example, a clear driver is used to clear simultaneously all the digits of a 40 digit arithmetic register to zeros or to ones. To test this circuit, it is not necessary to try all of the 2^{40} combinations of digits, because it is known that the maximum and minimum load conditions occur as the registers are filled with ones and zeros. Thus, using these special cases, it is possible to test these circuits adequately without trying all the many combinations. It will be noted, however, that such circuits need specially devised tests.

It is almost unnecessary to state that the test program should be designed so that an absolute minimum number of errors escapes detection. For example, in testing multiplication, we must test all of the digits of the double length product and in testing division we must verify that the remainder is correct.

We are at present using Leapfrog III as a detection program on the Illiac and will describe it in some detail. It is called the "leapfrog" because it has been arranged to "leap" through the memory so that the entire memory is tested. The leap is such that each word of the leapfrog occupies every position in the memory for about one second. Thus every memory position is subjected to all of the different intensities of use from the various kinds of storage in the program.

The memory is tested by a "comparison test" which takes place as the leapfrog is moved through the memory. Fig. 1 shows in diagrammatic form how the program is moved through the memory. At any one time, copy 3, which we call the working copy, is using copy 2 as the raw material to manufacture copy 1. As each word of copy 2 is translated to become a word of copy 1 it is also compared with the corresponding word of copy 5. If we trace the history of a particular copy at a given position in the memory, we discover it is manufactured (as copy 1), tested for correctness (as copy 2), used (as copy 3), and again tested (as copy 5). This ensures that the program is always checked before it is used, thus giving the maximum chance that a memory error will be found before it causes the leapfrog to act incorrectly. It also ensures that errors occurring in copies numbered 3, 4, or 5 are also detected.

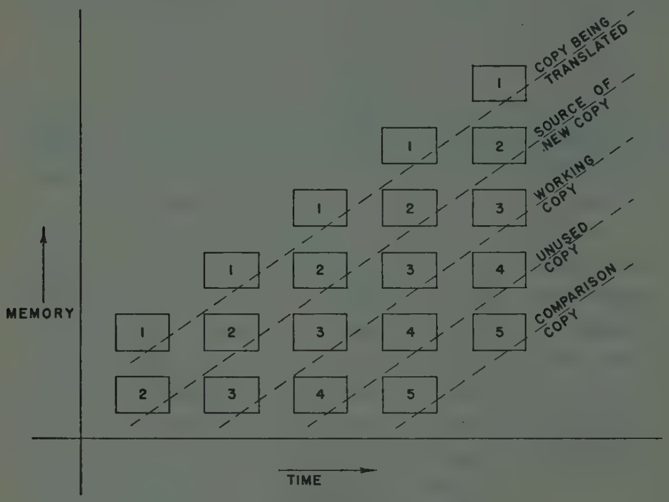


Fig. 1—Motion of the Leapfrog.

The leapfrog contains a stringent arithmetic test. This is split into two parts, a multiplication test and a division test. Both these tests use, and therefore test, other instructions besides multiplication and division. The tests are based upon identities such that all the digits of the numbers involved are checked and any single-digit error will be detected. The numbers used in the arithmetic test are pseudo-random numbers generated from the intermediate results of the previous arithmetic tests. The randomness of these numbers ensures that each digital position of the arithmetic unit is tested under all conditions.

Besides the two tests already mentioned there are additional tests which are performed only once per leap. These additional tests, which are listed in Table II, check certain common circuits of the Illiac under maximum load conditions.

The leapfrog is used to check the serviceability of the Illiac at least twice daily, and is also run during intervals when there is no other demand for computer time. As a result of this policy, and since the leapfrog is more stringent than programs used for calculation, nearly all intermittent faults are first detected by the leapfrog.

TABLE II

INDIVIDUAL TESTS OF THE LEAPFROG*

NAME	EFFECT
Multiplication	A general test of the arithmetic unit, including the use of multiplication instructions.
Division	A general test of the arithmetic unit, including the use of division instructions.
Comparison	Compares copy 2 with copy 5 so that memory errors are detected.
Carry test	Tests the full propagation and collapse of the carry in the adder.
Ones test Zeros test	Tests the functioning of the registers when full of ones or zeros. This essentially tests common driver circuits of the arithmetic unit.
Logical order test	This tests the logical instruction. Every digital position is tested in all conditions.
Shift counter test	This tests every digital position of the shift counter and recognition circuits.
Input-output test	This tests the ability of the input-output unit to read and punch in all digital positions.
Occasional input-output test	This tests the ability of the input unit to ignore certain characters and read correctly a group of characters, and tests the punch while continuously punching.

* Note: The first three tests are done 128 times per leap, the next six tests are done once per leap and the last test once per 128 leaps.

FAULT ISOLATION

When a fault has been detected, it is isolated and repaired as quickly as possible. Unfortunately, there is no simple step-by-step procedure which is applicable for isolation of all types of faults. We shall, however, discuss the isolation procedures applicable to a majority of intermittent failures encountered in operation of the Illiac.

We have noted that the Illiac is composed of three classes of units; the memory circuits, the mechanical parts of the input and output, and the logical circuits of the control and arithmetic unit. The first step in the resolution of a failure is the isolation of the fault to one of these units. Once this is done, a more detailed analysis is needed to define more precisely the location of the fault. The methods of analysis are as varied as the faults.

Our fault isolation methods are based upon the fact that nearly all faults are first detected by the leapfrog. It has been possible to incorporate into the leapfrog many of the features of an isolation program without affecting its stringency as a detection program. In the sections which follow, we describe the isolation features of the leapfrog, and also the more precise localization techniques which are necessary.

The Isolation Properties of the Leapfrog

The first leapfrog test was written for the ORDVAC[1] while it was at the University of Illinois. Although it was a stringent detection test, the ORDVAC leapfrog was unsatisfactory for the isolation of intermittent faults. The reason was that a long time elapsed before some errors were repeated so that it proved desirable to extract as much information as possible from each error as it occurred. The following features of the isolation program have therefore been incorporated in the versions of the leapfrog prepared for the Illiac.

---

[1] The ORDVAC was built for Army Ordnance by the University of Illinois and has been in operation at the Aberdeen Proving Ground, Maryland, since March, 1952.

When the comparison test of the leapfrog fails, the corresponding words from copies 2, 3, 4, 5 are printed with their respective memory locations. The intermediate results of the translation are also printed, so that an error of translation can be distinguished from a memory error. If the memory is at fault, the digital position and location of the error can be found from the data.

When the arithmetic test fails, all the intermediate results are printed and the test is automatically repeated. This action of testing and printing continues until the test is satisfied. Thus, if we have an intermittent error, we eventually obtain a correct set of intermediate results. This allows us to determine within one or two instructions the place at which the error occurred. On occasions it has even been possible to determine which step of the multiplication has gone wrong.

Besides these diagnostic features, the arithmetic and the special tests are arranged so that intermediate results used further in the calculation are stored in two memory locations and these are also printed out. This allows us, when one of these tests fails, to say definitely if the memory or arithmetic unit was at fault. When one of the special tests fails, a test identifying number and the intermediate results are printed to enable us to determine the nature of the fault.

The words and numbers are printed out in sexadecimal (base 16) notation, rather than the decimal system, because this is more helpful in diagnosing binary faults. The layout of the printed results has been chosen so that the error is as obvious as possible.

Occasionally a memory fault causes the working copy to become incorrect. In this case a special routine is used to read the leapfrog from the input tape and compare it with the working copy in the memory. The program prints discrepancies so that we can determine the nature and location of the memory fault.

Isolation Procedures

Because the leapfrog is a stringent detection test there are practical limitations to its diagnostic powers. When an error has been detected with the leapfrog further steps are often required to isolate the fault. However, it is relatively simple to find faults in the input, output, or memory circuits from the data supplied by the leapfrog.

Fault Isolation in the Mechanical Parts of the Input-output: Failure of an input-output test of the leapfrog indicates whether the tape reader or punch is at fault. Simple programs which test the faulty mechanism at a higher duty cycle are then used if required. Such failures are generally cured by mechanical adjustment.

Fault Isolation in the Memory: A memory fault is first isolated by the leapfrog to a particular digit of a word in the memory. A cathode-ray oscilloscope is then switched to the chassis of the failing digital position. By inspecting the wave forms displayed, it is usually possible to discover whether the chassis or cathode-ray tube is at fault. If the cathode-ray tube is at fault, the trouble can often be cured by adjusting the controls of the cathode-ray tube; but occasionally replacement of a cathode-ray tube is necessary. Faults which occur in a circuit of a chassis are diagnosed on a separate test rack after the faulty chassis has been replaced by a spare. No attempt is made to isolate a fault within a chassis while it is in the computer.

Fault Isolation in the Control or Arithmetic Unit: Faults in the arithmetic or control unit are usually caused by bad vacuum tubes or faulty connections. Circuits in this part of the Illiac have been conservatively designed, and failures of components other than tubes have not occurred.

Intermittent faults are caused either by shorted tubes, bad solder connections or by marginal circuit operation resulting from tube deterioration. When an intermittent fault is encountered we endeavor to increase the error rate. This can be done by increasing the duty cycle in the suspected part of the computer by a specially designed program written for that purpose. For intermittent shorts the error rate can be increased further by vibrating the suspected part of the computer with a hammer. With the program to give indication of the computer failures, we can discover the element of the computer most sensitive to vibration. If the error is due to marginal operation, then an alteration of a power supply voltage will often cause the error to become persistent, so that it can be traced. If the fault cannot be reduced to a persistent one, then measurements are made in the suspected circuits, either with a voltmeter or with an oscilloscope.

In the arithmetic unit, the technique of interchanging two parallel units is often used to verify other indications during the final localization process.

The effects of faults in the arithmetic unit and in the control are quite different and are usually easy to distinguish. Since each circuit of the control is associated with a control function, a faulty control circuit can be traced by careful observation of the effects of the malfunctioning. In the arithmetic unit, a faulty circuit initially causes a single digit error; the error may, however, be propagated before it is detected in such a way that the circuit at fault is difficult to find.

The computer is used as a versatile test instrument for localization of some intermittent control faults and for nearly all intermittent arithmetic unit faults. Usually the fault is detected by the leapfrog so that some localization clues are available; for example, it may be known that the fault caused an error during a multiplication. For the more difficult faults, a sequence of isolation programs is used, each successive program being shorter and applicable to a smaller part of the computer than the previous one. The programs used in the final localization of the faults are usually very short and are written on the spot, being discarded when the fault is found. Often the program can be reduced to two instructions, using a special mode of operation of the Illiac known as "instruction pairs." In this mode of operation two instructions are set up on a forty digit flip-flop register and obeyed alternately, with continually increasing addresses (modulo 1024).

The Programmed Multiplication Test: The isolation programs used for localization of faults are as varied as the faults themselves. An example of one of the more complicated isolation programs is the programmed multiplication test, designed to localize faults causing errors during a multiplication.

The Illiac performs a multiplication as a sequence of right shifts and additions. During the multiplication, the duty cycle is high in many parts of the arithmetic unit, and some highly intermittent faults occur only during multiplication.

A multiplication can be characterized as a two dimensional array of digits as shown in Fig. 2a. In a parallel machine one of these dimensions is the digital position in the registers and the other is the step of the multiplication (or time).

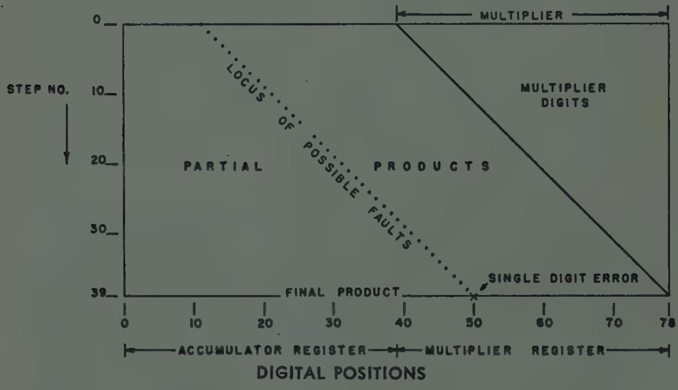

MULTIPLIER
STEP NO.
0
10
20
30
39
LOCUS OF POSSIBLE FAULTS
MULTIPLIER DIGITS
PARTIAL PRODUCTS
SINGLE DIGIT ERROR
FINAL PRODUCT
0
10
20
30
40
50
60
70
78
ACCUMULATOR REGISTER
MULTIPLIER REGISTER
DIGITAL POSITIONS

Fig. 2a—Multiplication with single digit error in product.

From a single digit error in a product we can find the relationship between the digital position at which the error may have occurred and the corresponding step. This relationship is represented by the dotted line of Fig. 2a. Unfortunately, not much information is given about the position or step at which the error occurred. The programmed multiplication test is used to isolate such a fault.

The test consists of two parts. The first part is a programmed multiplication and is used to generate in tabular form the two dimensional array of digits. The second part is a series of 39 partial multiplication tests, each of these tests splitting a single multiplication into two partial ones; the first simulates the initial n steps and the second simulates the last $(39-n)$ steps of the multiplication. The tabular values of the programmed multiplication are used for comparison with the final values of the first partial multiplication and are used as initial conditions for the second one.

When a partial multiplication test fails, information is provided for fault localization as indicated in Fig. 2b. An error resulting from a single faulty digital position may be detected in any of 39 digital positions of the product. On the other hand, if the error is detected by a partial multiplication test the range is reduced as shown on the diagram.

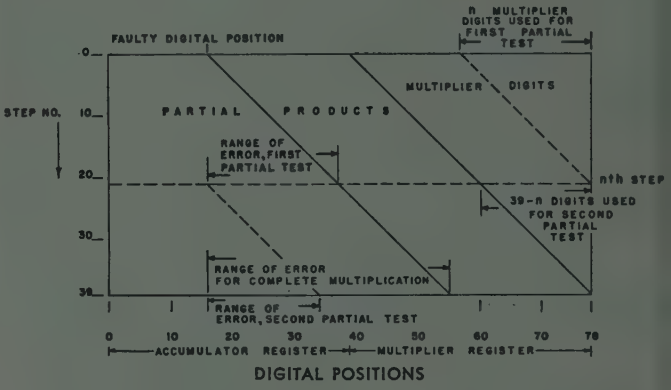

n MULTIPLIER DIGITS USED FOR FIRST PARTIAL TEST
FAULTY DIGITAL POSITION
STEP NO.
0
10
20
30
39
MULTIPLIER DIGITS
PARTIAL PRODUCTS
RANGE OF ERROR, FIRST PARTIAL TEST
nth STEP
39-n DIGITS USED FOR SECOND PARTIAL TEST
RANGE OF ERROR FOR COMPLETE MULTIPLICATION
RANGE OF ERROR, SECOND PARTIAL TEST
0
10
20
30
40
50
60
70
78
ACCUMULATOR REGISTER
MULTIPLIER REGISTER
DIGITAL POSITIONS

Fig. 2b—Fault localization with partial multiplication tests.

Sometimes an oscilloscope is needed for the final localization of the fault. The oscilloscope presents a cross section of the two dimensional array of digits, that is, a sequence of digits at a particular digital position. This display can be compared with the appropriate column of the table calculated by the programmed multiplication test, thus helping in the final stages of the isolation of the fault.

COMPUTER MAINTENANCE

Occasionally certain controls have to be altered to keep the computer in good adjustment. Such adjustments pertain to the memory, input, or output unit, as the rest of the computer is designed using components in on-off circuits. A typical adjustment is the optimization of the read-around ratio using the intensity control of a cathode ray tube.

To facilitate such adjustments, servicing programs have been written. The programs supply appropriate test conditions to the unit being adjusted and detect malfunctioning. A typical servicing program is the read-around adjustment program. This program continually scans the memory for points of low read-around ratio and indicates these points. If an adjustment is made while this program is running, the effect on the read-around ratio is easily seen, so that the optimum control setting can be discovered by trial and error.

In order to prevent gradually deteriorating components from causing errors during the regular scheduled operating time, marginal tests are performed periodically. There is no marginal testing equipment built into the Illiac, and the tests are performed by altering the power supply voltages, ac and dc. The leapfrog is used to detect the point at which a circuit fails, the printed error indication being kept as a record. When the tolerance range of any voltage becomes too small for satisfactory performance, the components causing the trouble are localized and replaced.

During the past nine months much more trouble has been caused by shorted tubes and open filaments than slowly deteriorating tubes so that few failures have been prevented in this manner. However, as the Illiac ages, these marginal tests should prove more valuable.

CONCLUSION

Diagnostic and servicing programs are essential for the efficient maintenance of an automatic digital computer. Since the engineer's knowledge of the computer and the power of the test programs are functions of one another, one would expect the diagnostic and servicing programs to be continually improved, especially with a new computer. It is our opinion that only by frequent and intensive searches for the weak elements, can one maintain the degree of reliability required for a truly serviceable computer, and furthermore, the degree of reliability which can be maintained is determined by the power of the test programs.

ACKNOWLEDGMENT

The material presented in this paper describes the joint efforts of the staff members of the Digital Computer Laboratory of the University of Illinois. The authors are especially indebted to Professor J. P. Nash of the Computer Laboratory for his many helpful suggestions during preparation of the paper.

The Logistics Computer*

R. S. ERICKSON†, ASSOCIATE, IRE

Summary—**The design and construction of a special-purpose electronic computer designed especially for logistics data-processing is described. The special characteristics required in this type of computer are listed together with the major design features incorporated to provide the particular characteristics. The logic of the computer is covered briefly and the method of programming is indicated. Constructional details as they affect operation and maintenance of the computer are also discussed.**

INTRODUCTION

THE LOGISTICS COMPUTER is a special-purpose fixed-sequence electronic computer designed for use in research concerning logistics data-processing methods.

The computer is at present located at George Washington University, Washington, D. C., and is being used by the Logistics Research Project there. The computer was delivered in mid-February, 1953, and was ready for operation by March 1. Punched paper-tape input-output equipment was originally supplied with the computer. Additional input-output equipment for handling magnetic tape was also developed.

Some of the major special characteristics that were deemed necessary for a logistics computer are listed below. These characteristics were used as guideposts during the design of the computer. With each special characteristic is listed the design feature which contributes most to providing the desired characteristic.

Desired Characteristic	*Design Feature*
1. Ability to process large masses of numerical data.	1. High-speed magnetic tape input-output equipment (in addition to punched tape equipment).
2. Ability to perform a relatively simple sequence of arithmetic operations repeatedly on successive, similar units of data.	2. Fixed-sequence type of operation.
3. A large internal memory.	3. A magnetic drum with storage capacity for 180,000 decimal digits.
4. Simple programming and operation.	4. Plugboard programming to specify desired instructions and their sequence.
5. Reliability.	5. Conservative design; provision for marginal checking.

MODE OF OPERATION

The logistics computer is basically a fixed-sequence machine designed to carry out one of two possible sequences on each successive numerical unit of data read in from either paper or magnetic tape. The routine or procedure which the machine will follow for each of the two sequences is defined prior to a problem by connections made on a plugboard. The two sequence routines may be altered from problem to problem but for any given problem they are fixed according to the plugboard.

The computer has two distinct modes of operation: (1) *tape control,* where successive units of numerical data are continually read in from either paper or magnetic tape, processed, and the results stored in the memory;

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 15, 1953. The work described in this paper was done under contracts Nonr-293(01) and Nonr-844(00) with the Office of Naval Research.

† Engineering Research Associates, Division of Remington Rand Inc., St. Paul. Minn.

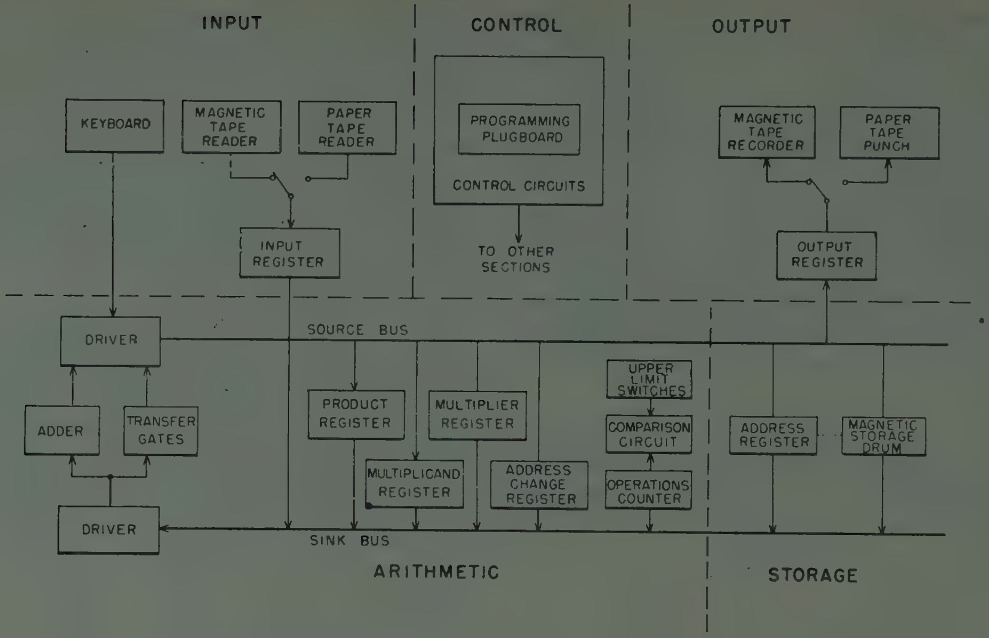

INPUT
CONTROL
OUTPUT
KEYBOARD
MAGNETIC TAPE READER
PAPER TAPE READER
PROGRAMMING PLUGBOARD
CONTROL CIRCUITS
TO OTHER SECTIONS
MAGNETIC TAPE RECORDER
PAPER TAPE PUNCH
INPUT REGISTER
OUTPUT REGISTER
DRIVER
SOURCE BUS
UPPER LIMIT SWITCHES
COMPARISON CIRCUIT
OPERATIONS COUNTER
ADDER
TRANSFER GATES
PRODUCT REGISTER
MULTIPLIER REGISTER
MULTIPLICAND REGISTER
ADDRESS CHANGE REGISTER
ADDRESS REGISTER
MAGNETIC STORAGE DRUM
DRIVER
SINK BUS
ARITHMETIC
STORAGE

Fig. 1—Block diagram of logistics computer.

or (2) *manual control*, where successive units of numerical data are obtained from its memory, processed, and the results either re-stored in the memory or read out to magnetic or paper tape.

Fifty-eight commands are available for forming instructions which may call for transfers, counts, jumps, read-outs, additions, subtractions, or multiplications. There is no division command as such; however, with some limitations division may be programmed.

The computer operates in the decimal system with a word-length of twelve decimal digits. Numbers are represented in a nine's complement system, in which the sign of the number is indicated by the value of the highest-order digit. A positive number is represented as its true (or absolute) value and always has a highest-order digit of four or less; a negative number is represented by its nine's complement and has a highest-order digit of five or greater.

Individual decimal digits are coded in an "excess-three" binary code which utilizes the ten middle of the sixteen possible combinations of a quartet of binary digits. The excess-three representation permits a nine's complement to be formed by merely complementing each binary digit.

The computer operates in a serial-parallel fashion. The decimal digits making up a word are transmitted and manipulated serially; the four binary digits representing each decimal digit are transmitted and manipulated in parallel.

Fig. 1 shows a block diagram of the computer. Although the names of the various registers indicate primary functions, the names are not intended to imply a limitation on the use of the registers. The capacity, in decimal digits, of each of the five arithmetic registers is given in the next column.

Register	*Capacity in decimal digits*
product	12
multiplicand	12
multiplier	6
address change	6
address	5

Transmission between the functional units is accomplished by means of a parallel bus system. Each register is able, on command, to read its contents onto the sink bus, and/or to receive input from the source bus. Read-out is nondestructive unless accompanied by a read-in, since each register is provided with a recirculation loop.

To transfer a number from one register to another it is necessary to specify (1) the source of the number, (2) the destination of the number, (3) whether it is to be a normal or complement transfer, and (4) the length, in decimal digits, of the number to be transferred. These basic pieces of programming information are referred to as commands. A number of these commands assigned to the same program step comprise an instruction. For example, if at some point in a program it is desired to transfer a twelve digit number from the multiplicand register to the product register, the instruction would consist of the following commands programmed as a single program step:

1. MCR: read-out transfer,
2. PR: read-in,
3. transfer: normal, and
4. cycle length: 12.

A number may be transferred to or from the magnetic storage drum in a similar manner. However, the transfer is not accomplished until the address indicated by the number in the address register is reached.

An arithmetic "add" or "subtract" instruction is formed similarly, except that (1) the desired arithmetic command replaces the simple transfer command and (2) the source of *both* original factors must be specified. Thus an add or subtract instruction will contain five commands.

Multiplication is a single-command instruction because the source and destination of the factors are fixed and may not be specified. A multiply instruction causes the number in the multiplicand register to be multiplied by the number in the multiplier register and the product to be added to the number in the product register. The time required for a multiplication depends upon the value of the digits in the multiplier, but will not exceed 14 msec.

Programming a desired sequence of operation is done by means of the programming plugboard shown on page 1328. Forty program steps are available, each of which may be used to define an instruction as described above. The step at which either of the two possible sequences is to begin is also specified on the plugboard.

Once the computer is started on a problem, the instructions are carried out in a numerically consecutive step-by-step manner unless one of several jump commands is used to modify the sequence. In *tape control* operation the sequence is initiated each time a complete tape entry is read. In *manual control* the sequence is started first by the manual start button on the operator's control panel, and thereafter by an appropriate jump command.

A six-digit decimal keyboard available on the operator's panel serves to either (1) hold a constant factor (or factors) for use during an operation; or (2) accomplish a manual transfer of numbers into any register (or registers) for testing or initial problem set-up.

MEMORY

The memory element of the computer is a magnetic drum 8½ inches in diameter and 15 long, capable of storing 180,000 decimal digits in their binary coded form. In order to allow the programmer to make efficient use of the drum the word-length, as used in the storage section of the computer, may be set from four to twelve decimal digits for a particular problem. If a word-length of twelve decimal digits is used, 13,200 words can be stored; whereas if a word length of four is used, 30,900 words can be stored.

A non-return-to-zero type of magnetic recording is used in the computer in which only the changes in polarity of the drum surface are significant. A monitoring flip-flop is used to remember the latest change in polarity. Since only one change of polarity is possible per recorded digit (as opposed to two in the conventional return-to-zero system) there exists, for equal resolution, a theoretical digit density ratio of 2 to 1 between the two systems. In the operating system this theoretical ratio is not quite realized since known zero digits must be provided at definite points to reset the monitoring flip-flop after switching to a new reading head. The monitoring flip-flop remembers only the change, not the polarity, therefore it is necessary that a known zero reset point be passed before reading can begin. In the logistics computer a known zero point was provided immediately ahead of each word recorded on the drum so that the access time was not increased beyond that inherent in the drum itself.

On the drum, the peripheral spot density is 140 per inch. This density, together with a 1,600 inch per second surface speed yields a 220 kc pulse rate.

INPUT-OUTPUT

Input data may be supplied to the computer on either punched paper tape or magnetic tape. Input rates of either 150 or 300 characters per second are available, the choice depending upon the time required to perform the programmed sequence of operations for each entry.

The input register assembles the data of a complete entry and, at the proper time, transmits it to the arithmetic section of the machine. A digit reversal is required since normal tape-preparation equipment punches tape with the highest-order digit first, and the computer operates on the data lowest-order digit first. This reversal is accomplished by shifting the input register $n-1$ times (where n is the register length) between the loading of each character as it is read from the tape.

Static magnetic-core memory units were used in the construction of the input register. These units provide sufficient speed for the low required shifting rate, and minimize the number of tubes. The maximum required shifting rate is 7 kc, which is well within the reliable shifting rate of the cores used. The register, which provides a circular shift, is four bits wide and eleven stages long. Ten of the eleven stages consist of pairs of magnetic memory units and are used in a conventional manner, being driven by even and odd advance pulses. The eleventh stage is composed of one core and a combination of flip-flop, gate and driver which functions as a loading platform for read-in or read-out operations.

Output data may be either punched on paper tape at a rate of approximately 10 characters per second, or recorded on magnetic tape at a rate of 600 characters per second. Either tape may be transcribed to a printed page at a rate of approximately eight characters per second.

Even though the transcription rate is the same, the magnetic tape has two advantages over the punched paper tape as an input-output medium. First, the magnetic tape may be used as a dump so that the computer may be used for other problems while transcription is in process. Secondly, and perhaps of greater advantage, is that the magnetic tape may be used to record data from the drum for use at a later date. Data so recorded needs no intermediate transcribing or editing before restorage on the drum.

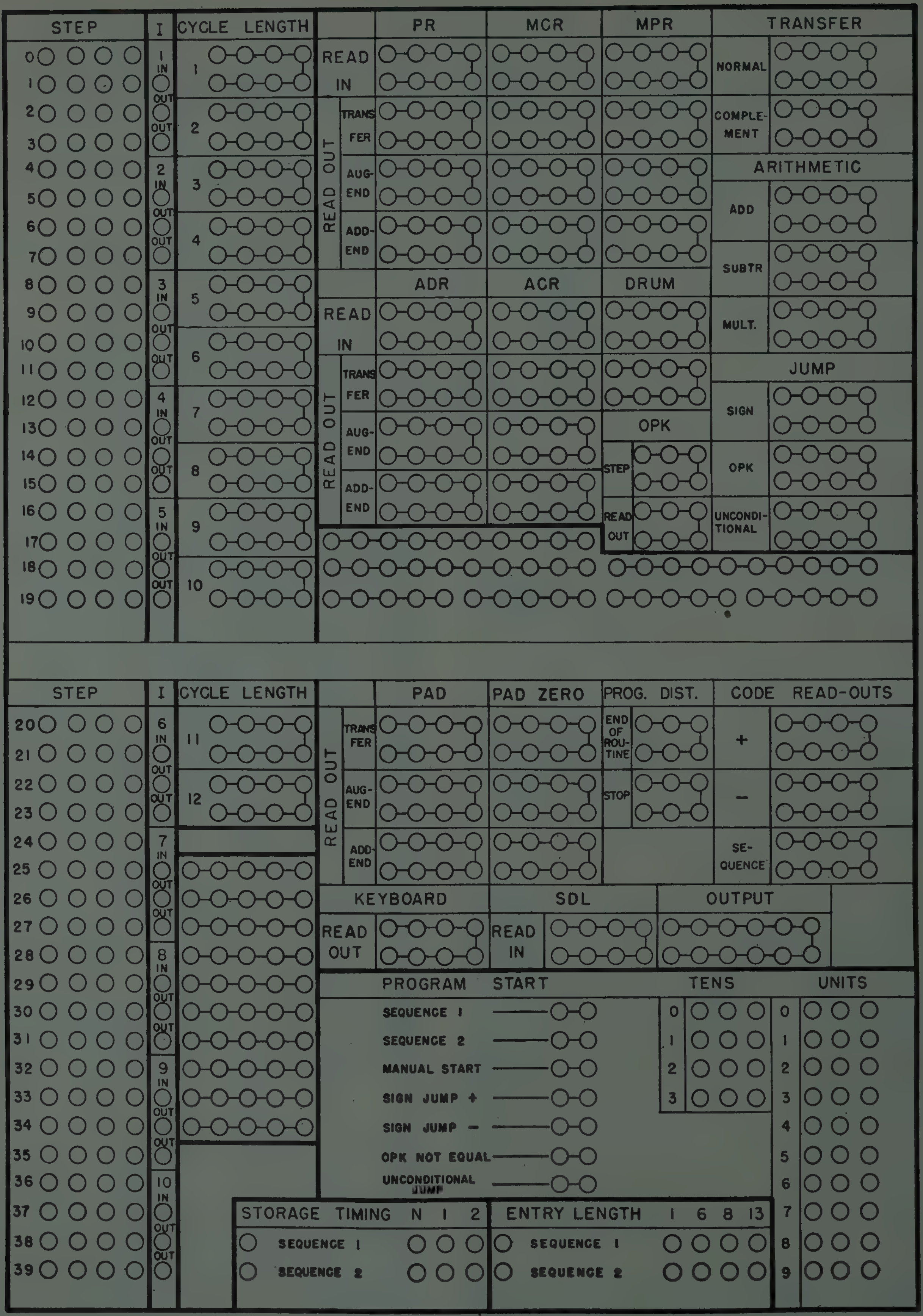

STEP
I
CYCLE LENGTH
PR
MCR
MPR
TRANSFER
READ IN
READ OUT
TRANSFER
AUGEND
ADDEND
NORMAL
COMPLEMENT
ARITHMETIC
ADD
SUBTR
MULT.
ADR
ACR
DRUM
JUMP
SIGN
OPK
STEP
READ OUT
UNCONDITIONAL
IN
OUT
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
1 2 3 4 5 6 7 8 9 10
STEP
I
CYCLE LENGTH
PAD
PAD ZERO
PROG. DIST.
CODE READ-OUTS
END OF ROUTINE
STOP
+
−
SEQUENCE
11
12
20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
KEYBOARD
SDL
OUTPUT
READ OUT
READ IN
PROGRAM START
TENS
UNITS
SEQUENCE 1
SEQUENCE 2
MANUAL START
SIGN JUMP +
SIGN JUMP −
OPK NOT EQUAL
UNCONDITIONAL JUMP
STORAGE TIMING N 1 2
ENTRY LENGTH 1 6 8 13
SEQUENCE 1
SEQUENCE 2

Fig. 2—The programming plugboard.

EQUIPMENT DESCRIPTION

Fig. 3 shows the installed computer. The computer is housed in three separate cabinets. The cabinet in the foreground contains the maintenance control panel (vertical), the operator's control panel (inclined), the programming plugboard, and the control circuits. The second cabinet contains the power control panel, arithmetic circuits and power supplies. A third similar cabinet, shown at the extreme right, contains the magnetic storage drum and associated control circuits.

The operating position shown in Fig. 4 provides convenient access to all operating controls and to input and output equipment. The control panel and plugboard are to the operator's right, the photoelectric tape reader and output tape punch are on the table. Magnetic tape input-output units, not delivered at the time the photograph was taken, are now located to the left of the operator. This places all the operating controls in a convenient console-like array.

Start-up and shut-down controls are located on the power control panel. This panel also controls a remote motor-generator set which supplies the bulk of the dc power for the equipment. Door interlock indicators, meters, and fuses are also located on the power control panel.

The maintenance control panel which is used for running self-checking problems is shown in more detail in Fig. 5. Special controls are provided to allow slow-speed operation and various degrees of step-by-step operation for diagnostic purposes. Switches are also provided which cause cyclic operation of some of the normally nonrepetitive operations. Neon indicators are provided for every flip-flop in the computer. Normal operating controls available on the adjacent operator's control panel are not duplicated on the maintenance control panel.

Individual air-conditioning units are provided for each cabinet. Cooled air from the conditioner is ducted to a plenum chamber in the lower portion of the cabinet. Individually-adjusted openings distribute the cooled air to each of the bays in the cabinet in accordance with their individual heat loads. The blowers are set to run continuously so as to maintain a static pressure in the plenum. The compressors are controlled by thermostats sensing the exhaust air of the cabinets. The thermostats are set to about 77 degrees so that the computer will not disturb the normal heat balance in the room. If the thermostats are set lower, the room temperature will drop provided the additional heat load in the room is not too great.

CONSTRUCTION DETAILS

All operating circuits are mounted on standard plug-in unit chassis of the type shown in Fig. 6. This chassis will accommodate a total of 22 miniature tubes, or 22 ERA pulse transformers, or any combination of 22 or less. Pulse transformers may also be mounted on the component boards located on the sides of the chassis. Connections to the cabinet circuits are made through a seventy-four pin connector located on the bottom of the

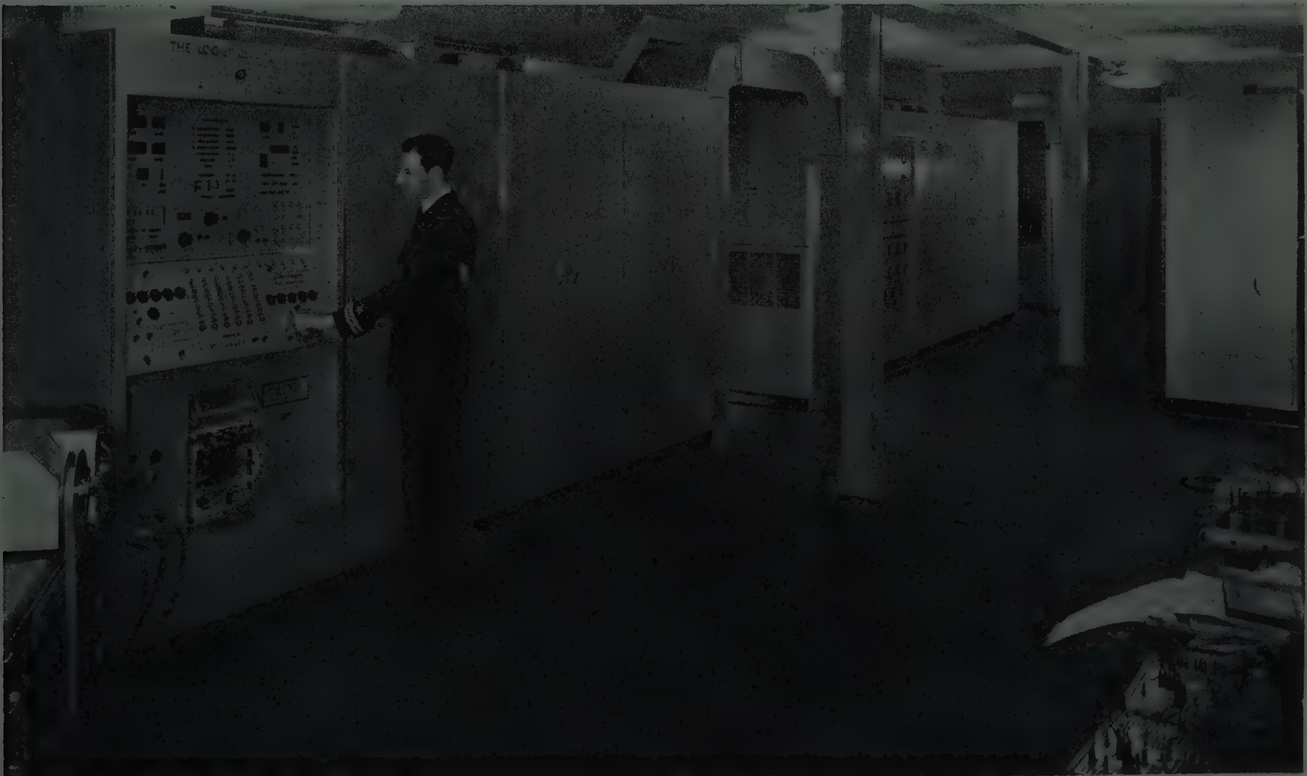


Fig. 3—This is an over-all view of the logistics computer installed at the George Washington University logistics research project.

chassis. A threaded extraction post equipped with a butterfly handle is used to secure the units in the cabinet. The same basic style of chassis is used for mounting relays and magnetic memory units. (See Fig. 7.)

The individual plug-in units are mounted in the cabinets as shown in Fig. 8. Several chassis have been removed to show the type of mounting. The indicators along the top of the cabinet are over-temperature warning lights. These lights indicate when the temperature in a given section exceeds 100 degrees Fahrenheit.

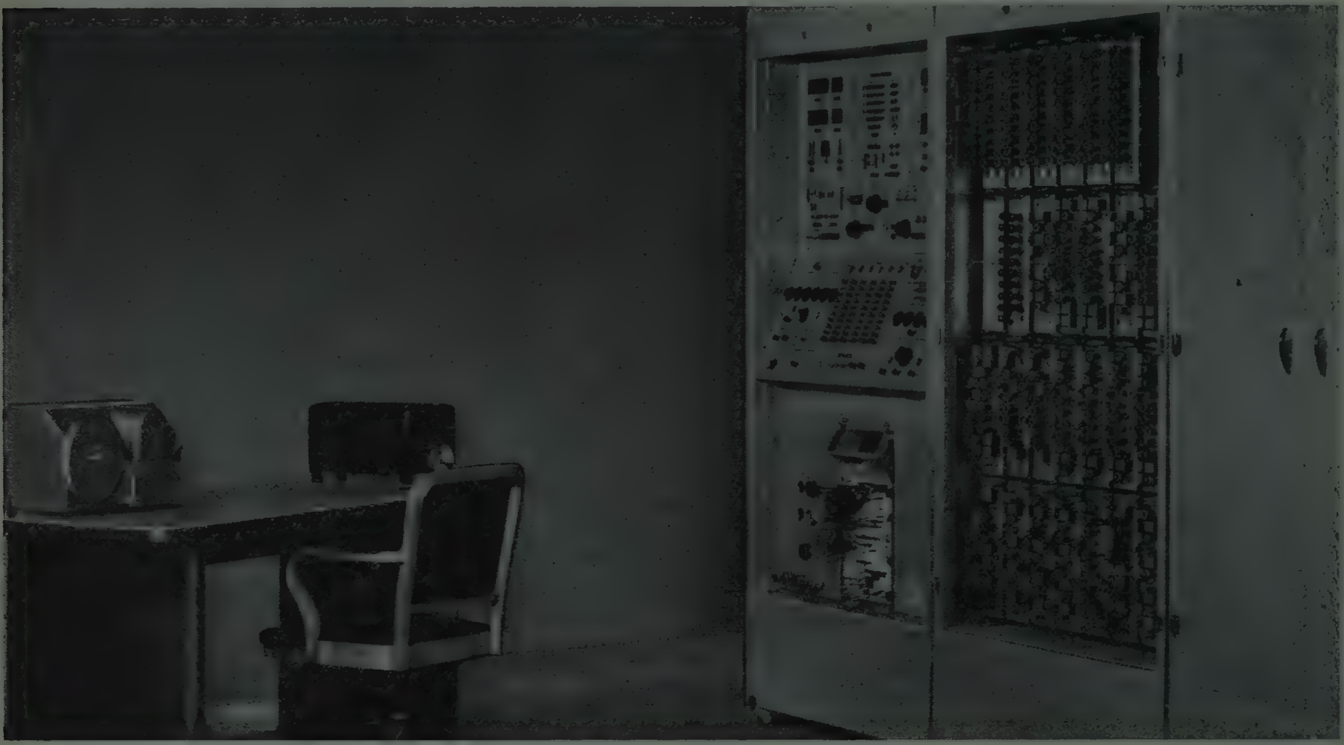


Fig. 4—This view of the operating position of the logistics computer shows the operator's panel, programming plugboard, paper-tape reader and paper-tape punch. One pair of doors have been removed to show chassis arrangement.

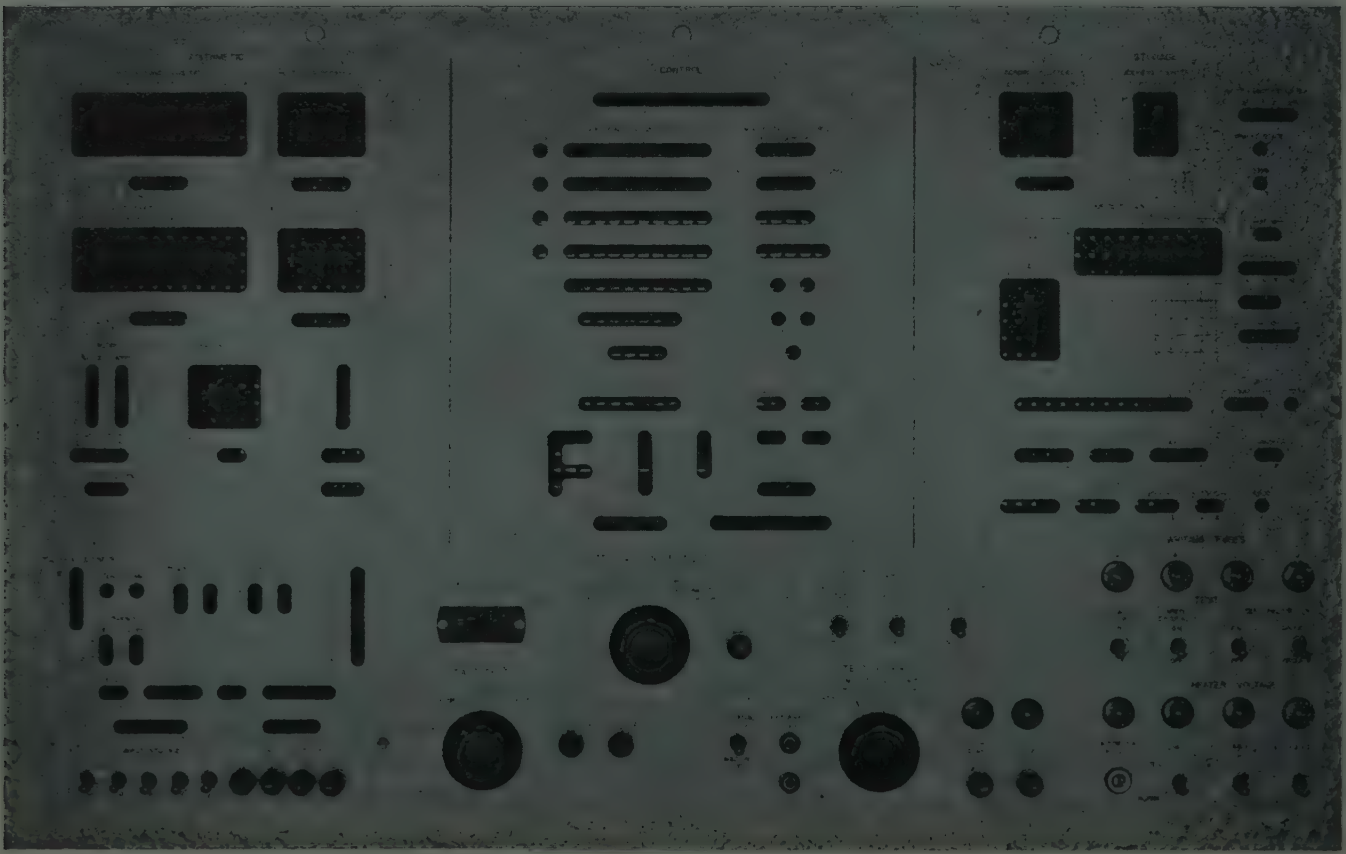


Fig. 5—Maintenance control panel.

Typical cabinet wiring is shown in Fig. 9. Two types of signal wiring are used: *Spaced wiring* is used for signals where the capacitance-to-ground or to other wires must be minimized (such as dc gate enables); *twisted-pair wiring* is used for pulses carried on balanced transmission lines. Filament transformers and their individual primary fuse protection are located in the upper portion of the cabinet. Cabinets are interconnected through terminal blocks such as those appearing on the left side of the cabinet.

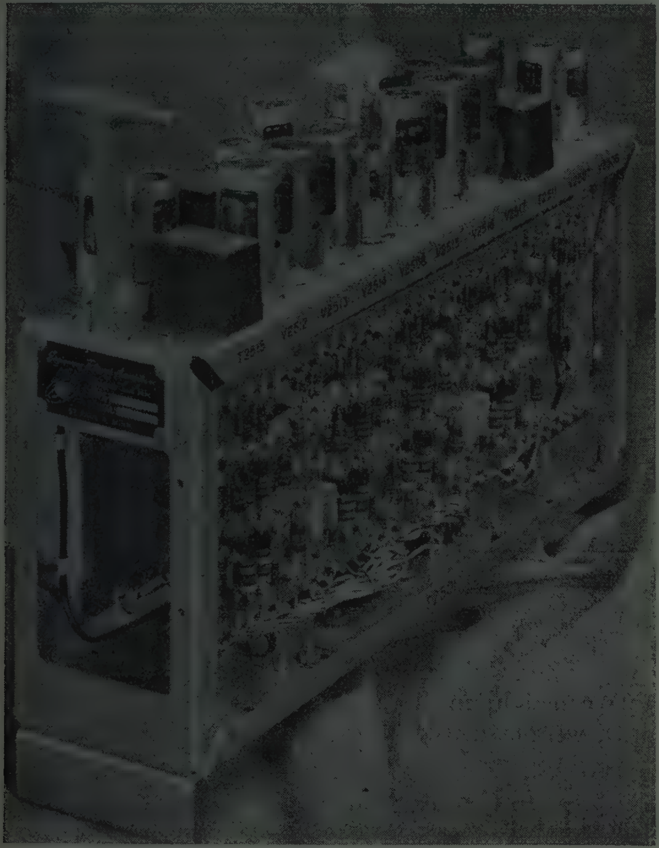


Fig. 6—Standard plug-in chassis.

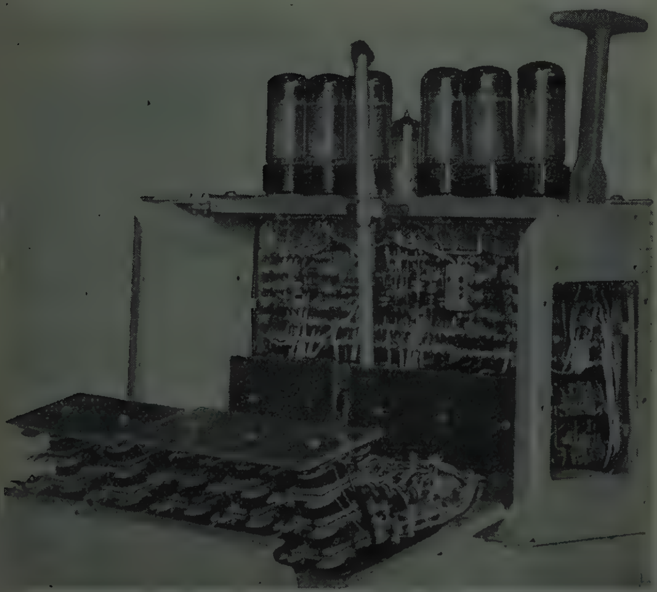


Fig. 7—Close-up of chassis shows in detail how static magnetic memory units can be mounted in standard plug-in chassis.

The portion of the storage cabinet that contains the magnetic storage drum is shown in Fig. 10. The eight plug-in chassis mounted above the drum contains relays used to connect writing circuits to the proper heads. The drum is provided with more than 200 heads and can store over 720,000 binary digits. A direct-coupled $\frac{1}{3}$ horsepower induction motor drives the drum at approximately 3,600 rpm.

MAINTENANCE AND CHECKING

Marginal checking techniques similar to those proven on the ERA 1101 computer have been employed on the logistics computer. The basic technique consists of reducing tube-heater voltage on each section of the machine, first individually and then together, while running self-checking test problems. A marginal check on the dual-path relay circuits employed in the computer is made by running self-checking test problems with only one of the two groups of relays energized.

Although a formal maintenance program has been set up and exact data on component life and reliability are being accumulated, the time is too short to attempt to draw any conclusions from the data collected to date.

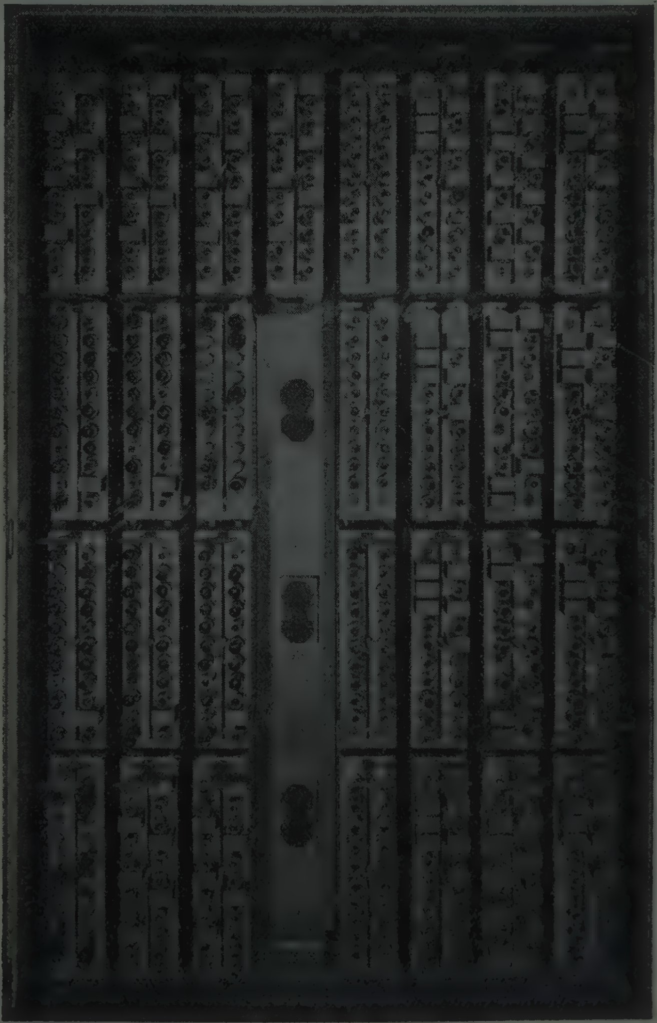


Fig. 8—A portion of the control cabinet of the logistics computer with several of the plug-in chassis removed.

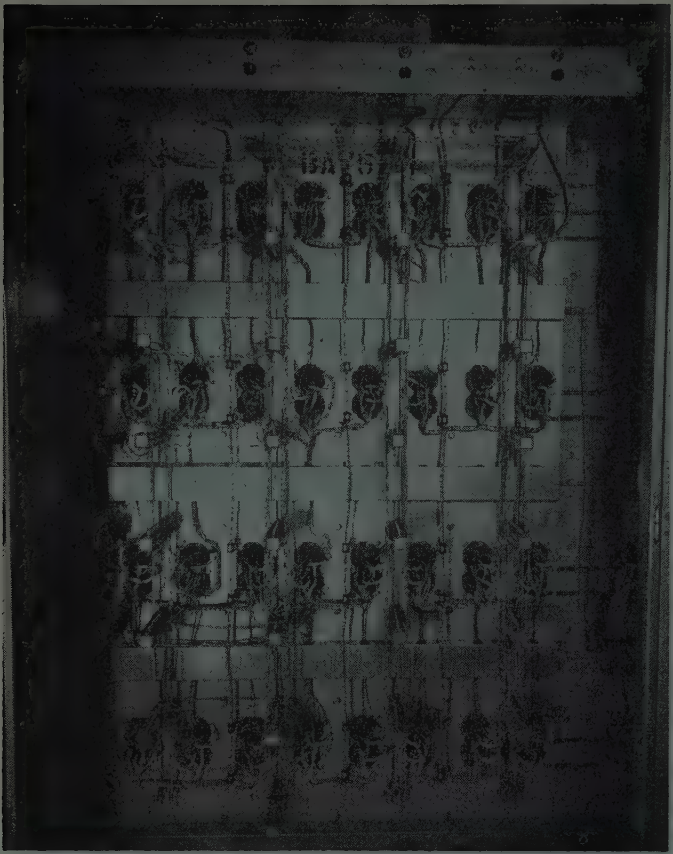


Fig. 9—Typical cabinet wiring.

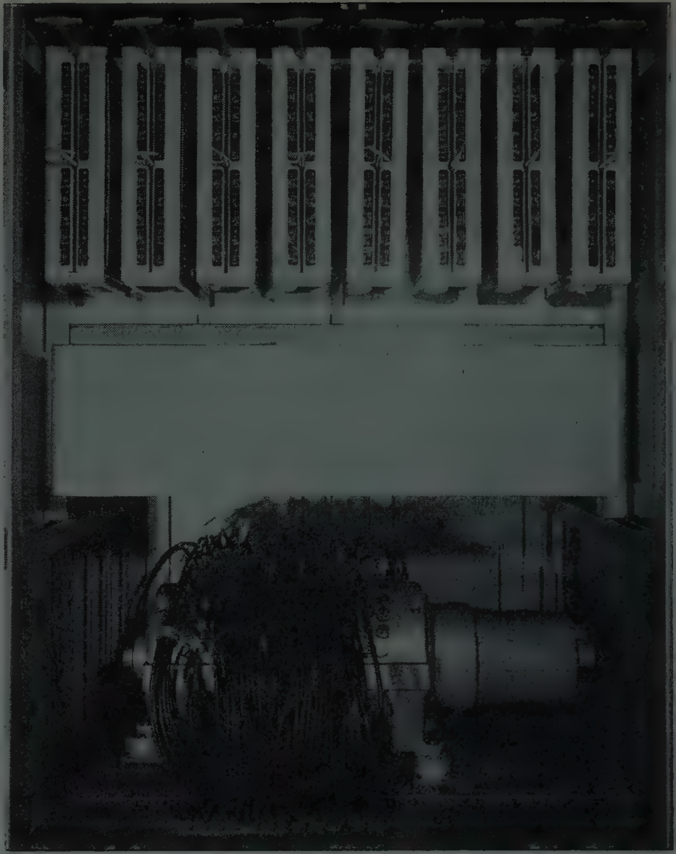


Fig. 10—This view shows how the magnetic storage drum is mounted in the storage cabinet.

ACKNOWLEDGMENT

During the design and development of this computer close liaison was maintained with the personnel of the ONR-sponsored Logistics Research Project at George Washington University, Washington, D. C. Many valuable contributions to the logical design of the computer were made by this group.

The Remington Rand Type 409-2 Electronic Computer*

LORING P. CROSMAN†, ASSOCIATE, IRE

Summary—The Remington Rand Electronic Computer, Type 409-2, does computations by arithmetic steps in sequence with a unique self-proving feature. Parallel inputs to ten vacuum-tube decades are added or directly subtracted into a 22-column Accumulator. The Accumulator is connected in a ring so that a number or pair of numbers can be shifted to any position. Decimal positions are automatically handled by a Decimal Computer. Signs are handled algebraically. The total electron tube complement includes 1476 vacuum tubes and 1128 cold-cathode gas diodes. Most of these are designed and manufactured especially for computer use.

Inputs are brought to the Accumulator, using a Call Line for each complete number, from three types of storage:

1. Variables from a tabulating card reading block of Sensing Switches; 2. Constants from manually settable Constant Switches; and 3. Intermediate results from Storage Relays.

Outputs are delivered to Punching Storage from Intermediate Storage, in one or two blocks. Results are punched into the same tabulating card or following cards, as may be desired. Programming is directed by interchangeable Plug Boards. There are 40 Calculating Steps and 6 special steps: Clear, Set I, Set II, Sort I, Sort II and Trip.

Each Calculating Step has 5 addresses and a process designation: 1st Operand; Process (+, −, ×, ÷); 2nd Operand; Result; Next Step if Result is "plus"; and next step if Result is "minus." Each step is automatically proved by a reverse process and repeated if the stored result is wrong so that progress to the next step is impossible until the preceding step has checked itself correct.

A Reproduce feature provides for storing alphabetical or numerical information for punching into following cards, or transferring to other Fields of the same card.

INTRODUCTION

THE REMINGTON RAND Electronic Computer, Type 409-2, reads information from punched cards, performs one or more sequences of arithmetic steps, and punches results into the same card from which the information was read, or into following cards.

---

* Decimal classification: 621.375.2. Original manuscript received by The Institute, May 18, 1953; revised manuscript received June 26, 1953.

† Remington Rand Inc., Laboratory of Advanced Research, South Norwalk, Conn.

For example: $[(A \times B)/(C+D)]-E=P$ is done in a sequence of four arithmetic steps. 1, Multiply: $A \times B$; 2, Add: $C+D$; 3, Divide: $(A \times B) \div (C+D)$; and 4, Subtract: $[(A \times B)/(C+D)]-E$. Each step is proved automatically, by reverse process, without programming, before the following step is initiated. This will be explained later. The complete computer as shown in Fig. 1 consists of two units, the Card Sensing-Punching Unit and the Electronic Computing Unit. These units are interconnected by multiconductor cables. The general organization is indicated by the diagram of Fig. 2.

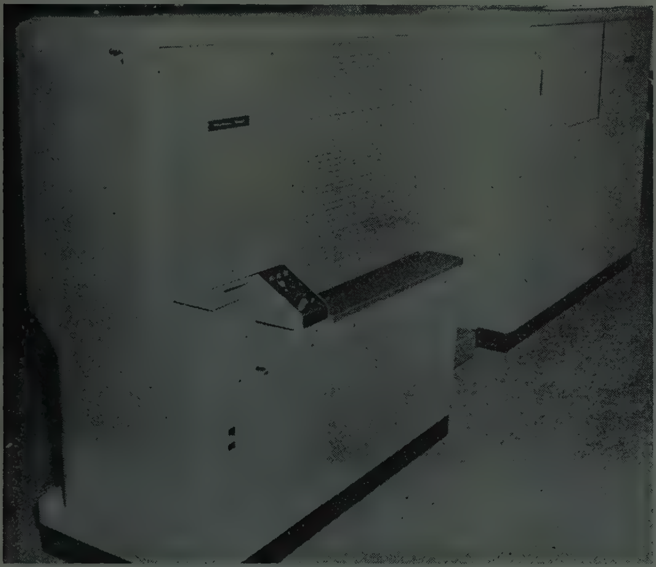


Fig. 1—The complete Electronic Computer assembled for operation, Sensing-Punching Unit at left, Electronic Computing Unit at right. The two units are interconnected by multi-conductor cables. Routine operating controls and indicators are on the sloping panel in foreground.

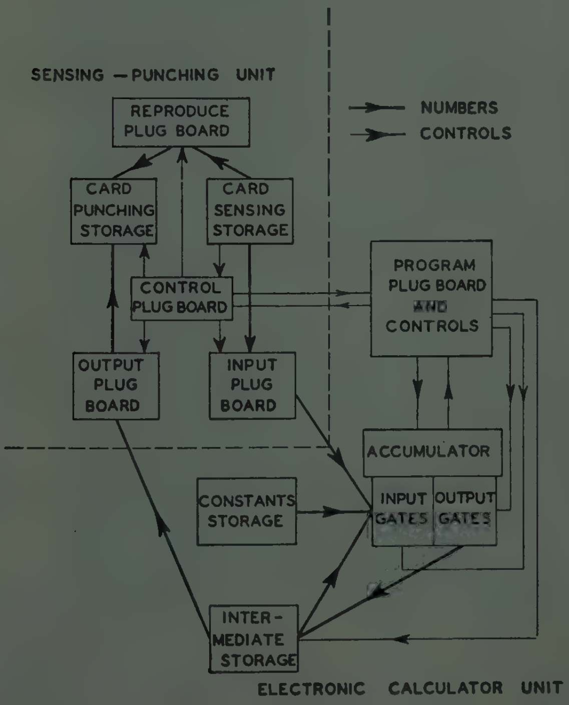

SENSING — PUNCHING UNIT
REPRODUCE PLUG BOARD
NUMBERS
CONTROLS
CARD PUNCHING STORAGE
CARD SENSING STORAGE
CONTROL PLUG BOARD
PROGRAM PLUG BOARD AND CONTROLS
OUTPUT PLUG BOARD
INPUT PLUG BOARD
ACCUMULATOR
INPUT GATES
OUTPUT GATES
CONSTANTS STORAGE
INTER-MEDIATE STORAGE
ELECTRONIC CALCULATOR UNIT

Fig. 2—Logical organization of the 409-2 Electronic Computer with routing of numbers indicated by heavy lines and control functions by light lines.

DECADE

Since every digital computation is basically a series of counting operations, let us first consider the Decade Unit. Like most of the electronic circuitry of the machine, this is housed in a box-like pluggable chassis structure (Fig. 3). The tubes are mounted in the back of the chassis. These are mostly Type 5964, designed particularly for computer operation. The circuit components are mounted in "cages" (Fig. 4) which are plugged into the front side. Each cage is directly opposite the tube with which it is related. Projecting on both sides of the chassis are silver plated, beryllium copper contacts which make all electrical connections with the fixed frame wiring. All of the tube sockets, cage sockets and contacts are interconnected by wiring within the chassis. Coarse-thread jack screws fastening into frame members, one at each end, facilitate quick change of chassis.

This construction puts the tubes on the inside of the machine where there is a ventilating air stream. The cages may be removed without disturbing the chassis and almost every junction in the circuits may be probed at the outer ends of the cage wires, even while the machine is running.

The Decade Chassis has 21 double triode tubes. Six of these are in Eccles-Jordan flip-flop circuits, each having two stable states. They are arranged in a biquinary fashion, and can count either forward or backward.

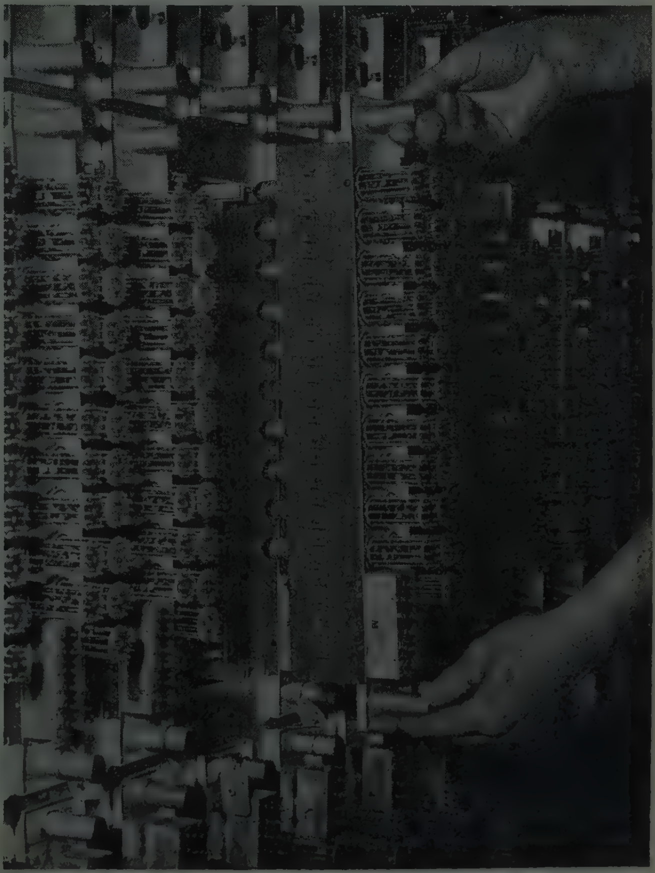


Fig. 3—Typical 24 Tube Chassis, tubes toward inside of machine, pluggable cage opposite each tube for components in its circuits. Each chassis has contacts for all electrical connections on either side and coarse-threaded screw at each end for quick change.

One flip-flop, which is the "bi" of the biquinary counter, determines whether the digit is odd or even. One state of this flip-flop, which we shall call the "off" condition, has no numerical significance. The other state, which we shall call the "on" condition, has a value of 1.

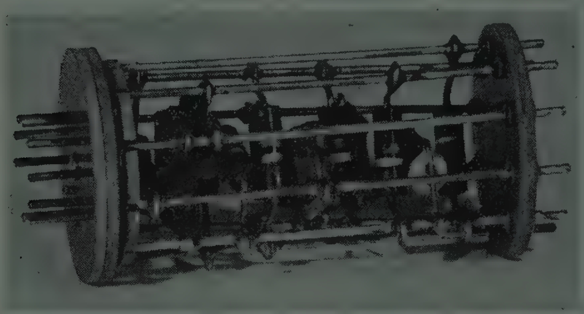


Fig. 4—A Typical "Cage." Each resistor and capacitor is soldered between two of the ten wires, all but one of these wires projecting through the base to fit a miniature 9-pin socket. The wires radiate heat and serve as probe points.

When the counter stands at zero this odd-even flip-flop is "off." A single pulse to this stage turns it "on," counting 1. A second pulse switches it "off" and an output from the "off" side goes through a gate to the "quinary" part of the counter. This part has five flip-flops each with its "off" or "on" condition. The "on" states of these flip-flops have values of 0, 2, 4, 6 and 8, with never more than one stage "on" at a given time. When the counter stands at zero, the 0 flip-flop is "on." Input pulses to this quinary ring go to all five stages and serve to turn "off" whichever one is "on." The stage which goes "off" gives an output pulse to the next stage to turn it "on." In the process of addition this next stage is the one of higher value and in subtraction it is the next of lower value.

Thus, in the above example when the second pulse turns the 1 stage "off" its output goes through an addition gate to the ring of five, turns off the 0, which turns "on" the 2 stage. A third pulse to the 1 stage turns it "on" again and we have a count of $2+1=3$. When we come to the tenth pulse it turns "off" the 1 stage, which turns "off" the 8 stage and the latter turns on the 0 stage, and also a carry storage flip-flop. The carry takes place after the addition of a digit when the output resulting from turning "off" the carry storage stage goes to the 1 stage of the next higher order decade.

Input pulses to the Decade do not all go to the 1 stage. In fact, it never gets more than one or two pulses in adding or subtracting a digit. Other pulses go directly to the ring of five. For instance, to add 9 there are four pulses to the ring of five and one to the 1 stage. Each pulse to the ring counts a value of 2, thus nearly doubling in effective value the 40-KC pulse rate.

There are two switching gates at the output of each stage of the biquinary counter, six addition gates and six subtraction gates. Normally all of these gates are closed, which condition facilitates the shifting of numbers in the accumulator to be described later. When addition is called for by the program all six of the addition gates are opened so as to advance the counter 0, 1, 2, 3, 4, etc., while in subtraction it goes the other way, 0, 9, 8, 7, etc.

Counting in either direction may be unique in electronic computers. At least it is unusual. Most machines add a complement in order to subtract. While this decade uses more tubes than the minimum requirements, it lends itself to simpler circuits elsewhere and uses a different set of gates in the proof. For each of the 6 counting flip-flops there is a shift tube for shifting the digit to the next higher order and receiving a digit from the next lower order.

ACCUMULATOR

The complete Accumulator has 22 decades. The ten lowest orders, columns 1 through 10, are connected to ten Input-Output chassis. A number having a maximum of ten digits is entered into the accumulator in parallel; that is, all digits at the same time. They are counted in, additively or subtractively as already described. Results leave the accumulator from the same ten columns on a single read-out pulse.

The 22 decades are connected in a ring; that is, each digit advances to the next higher order. The digit in column 1 goes to column 2. The one in column 2 goes to column 3, etc., and the digit in column 22 goes to column 1. All 22 shifts are simultaneous at a shift pulse. To shift a number one place toward the right requires 21 shift pulses. These pulses come from a multi-vibrator Shift Impulse Generator at the rate of 20 KC per second.

DECIMAL COMPUTER

Decimals are automatic. By setting a selector switch for each Card Field, Constant, and Intermediate Storage the programmer assigns a decimal place to all input and output numbers. A Decimal Computer takes care of all shifts.

The switches are wired so that either a true number of decimal places or its complement may be called as an input to the Decimal Computer. The heart of this computer is the Decimal Counter. This is a natural binary flip-flop cascade modified to have a radix of 22. It counts in only one direction, positively, and repeats when it reaches 22. In other words, $22=0$. This counter normally stands at 0. During a Calculating Step the number of decimal places of each operand is added or subtracted (by adding the complement on 22) in the Decimal Counter. The number of shifts in the Accumulator is also counted to keep track of the decimal point location.

When the first operand is entered in the Accumulator its decimal position is subtracted in the Decimal Counter. In addition or subtraction the decimal position of the second operand is added in the Decimal Counter. This gives a difference which is the number of column shifts required to align the decimal points. The first operand which is now in the Accumulator is shifted while counting until the Decimal Counter reaches 22, i.e. 0. After adding or subtracting the sum stands in the Accumulator with the same number of decimal places as the second operand. Before storing, the above procedure is repeated, subtracting the decimal position of the second operand, or sum, from that of the storage and shifting the sum to decimal alignment.

Decimal positions in multiplication and division are handled in a similar manner.

INPUTS AND OUTPUTS

As shown in Figs. 5 and 6, ten Input-Output chassis are located directly across from the first ten columns of the Accumulator on the other side of the Electronic Computer Unit frame.

Except in the Accumulator, which uses the biquinary code described above, all numbers are represented in the Remington Rand "90-column" Code that is used in the punched cards. Each column has six hole positions. The values of these positions, from top to bottom, with a single hole punched in the column are: 0, 1, 3, 5, 7, 9. When the 9 position is punched and another hole is punched in the 1, 3, 5 or 7 position the values are 2, 4, 6 or 8 respectively. This code is readily translated into and out of the Accumulator code by vacuum-tube circuits.

All ten digits of an input number are translated simultaneously at a rise in voltage of a call line related to the storage location of the number. This is accomplished by means of specially designed sub-miniature gas diodes whose characteristics are given in Table I, page 1336.

There are six gates in each chassis for passing count-

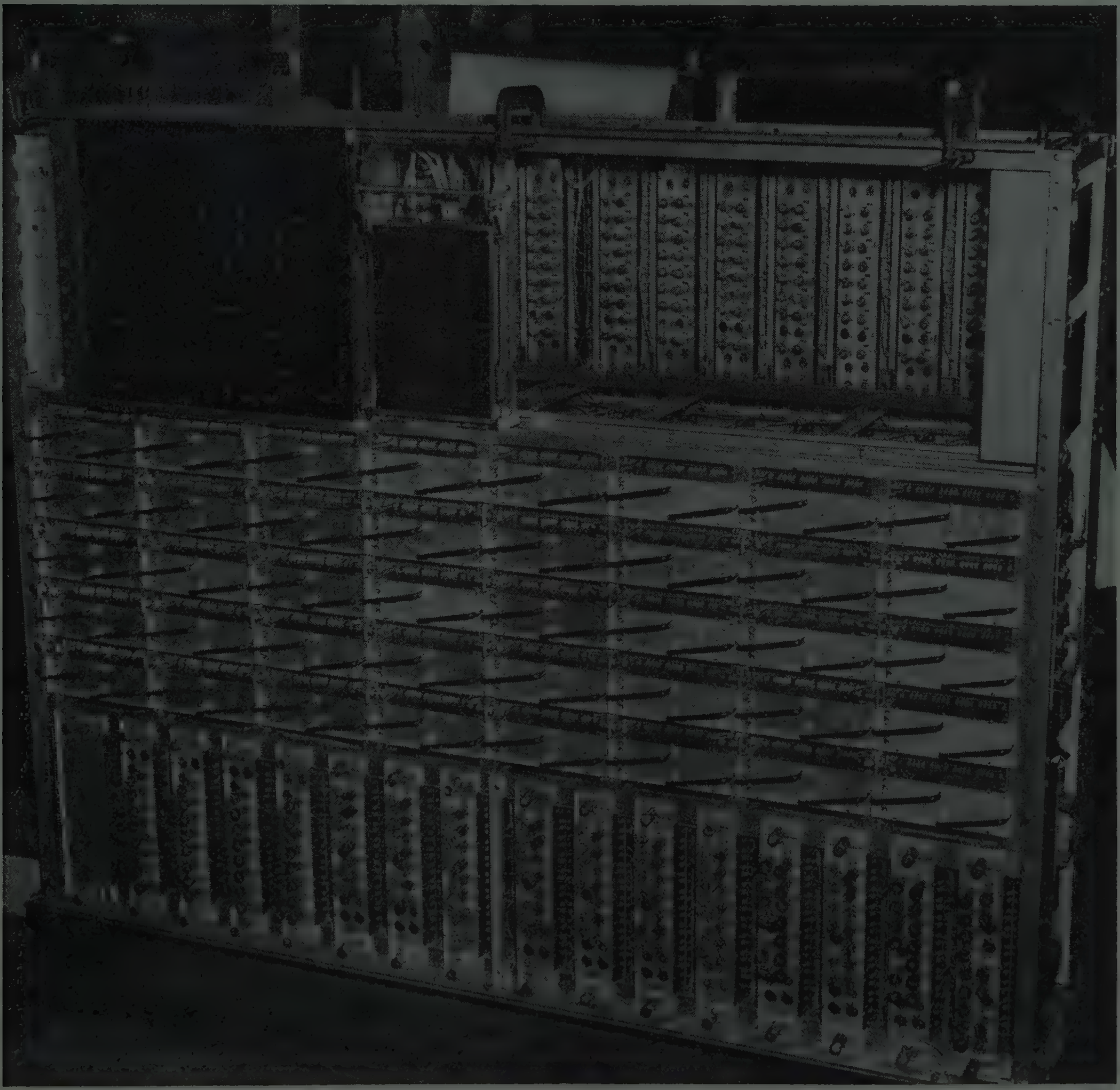


Fig. 5—Front side of Electronic Computer Unit with covers removed. Constants and Program Plug Board at upper left, tube side of Step Sequence Chassis at upper right. Intermediate Storage relay chassis (with diagonal handles) occupy full length in center. The Call Line Bias Chassis is the first at lower left and Input-Output Chassis are at lower right and center. Clamps at top are used only in final assembly and test.

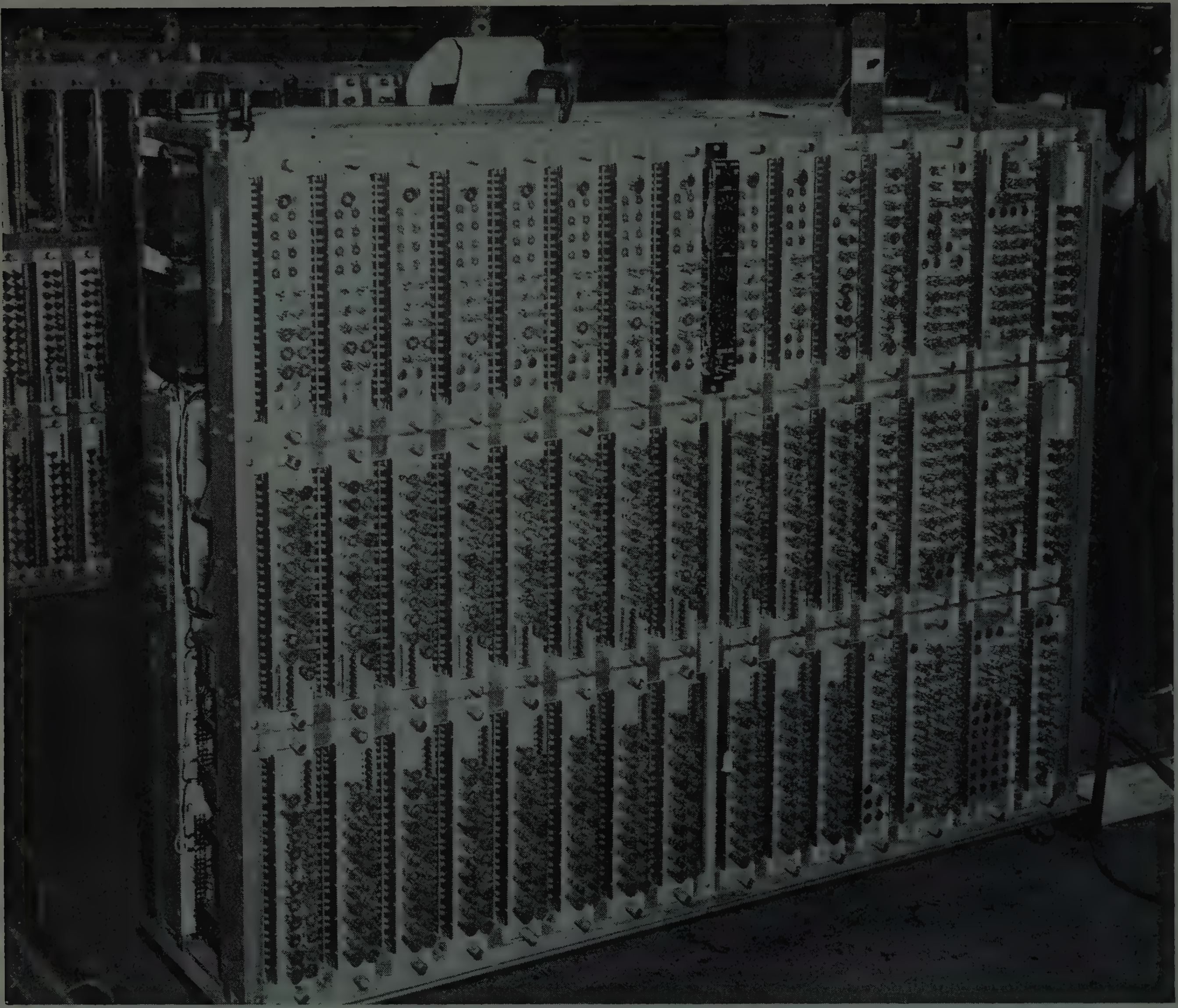


Fig. 6—Rear of Electronic Computer Unit with covers removed. There are ten Step-Sequence chasses (top row left) and twenty-two Accumulator chassis, first 11 columns (lower left) and columns 12 to 22 (middle left). Controls and Routines chassis are at right, top to bottom, including Decimal Computer and Service Switches.

ing pulses to the corresponding Decade of the Accumulator. The translator circuits open appropriate gates so that pulses from the Registration Impulse Generator (RIG) will be counted. Two gates control pulses to the odd flip-flop, or 1 stage. The third controls a single pulse to the ring of five to count a value of 2. The fourth passes 2 pulses for a count of 4. The fifth passes 3 pulses for a count of 6, and the sixth passes 4 pulses for a count of 8. For each add or substract registration, the RIG makes one cycle, producing timed pulses over six lines.

The Input Gates read numbers from three kinds of storage; namely, punched card Sensing Storage, Constant Storage and Intermediate Storage. The Output Gates deliver numbers only to Intermediate Storage.

The Sensing Storage consists of single-pole normally-open switches. There are 90 columns in the card with six hole positions in each column, making a total of 540 hole positions. There are 540 Sensing Switches, each occupying an area of $\frac{1}{4}'' \times \frac{5}{32}''$ which is the spacing of the hole positions. The 540 pins press lightly, but positively

TABLE I

Type 6332 Gas Diode Characteristics

	Min.	Ave.	Max.
Anode Supply Voltage,* DC	100	—	— Volts
Breakdown Voltage, DC	—	80	— Volts
Voltage Drop, DC	50	55	60 Volts
Regulation, DC (.2 to 1.5 ma.)	3	—	5 Volts
Current, DC	0.2	0.6	1.0 Milliamperes
Breakdown Time†			50μ seconds

* Tube should never pass current with reversed polarity.
† With 100 volts DC applied.

against the card being sensed and those which find holes in the card close the related switches. The switches latch closed and constitute storage for all information in the card, while the pins retract and the card is fed to the adjacent punching station.

The card columns are grouped in Fields. For example, a very simple invoicing problem would have a Field for Quantity, another for Unit Price, perhaps a one-column Field for the size of the unit (each, doz., gross, hundred, etc.) and maybe a Field for discounts which apply. The card is designed with enough columns in each Field to handle the largest number ever encountered in the work.

A plug-board on the Sensing-Punching Unit (Fig. 7) groups the connections for each Field, indicates the decimal location and, if required, makes connections to read one or a combination of holes which show whether the number is positive or negative. Each Field is connected to a Call Line so that the Program can call for whichever Field it needs and register the number in the Accumulator. There are 9 call lines for a maximum of 9 Fields.

The so-called Block Sensing described above is fast, requiring only about 20 milliseconds to change from one card reading to the next.

Constant Storage consists of manually settable decade switches (Fig. 8). Twenty constants, varying in capacity from 4 to 10 digits, may be stored for use by the program. Each has a settable decimal position switch, a plus or minus sign switch, and a Call Line for signals from the Program.

Intermediate Storage (Fig. 5) has a capacity of 8 ten-digit numbers.

These numbers are stored in relays, five for each digit and one sign relay for each number (Fig. 9). A pair of holding contacts on each relay retains the information. A second pair communicates with the Input Gates to the Accumulator and a third pair handles the output to Punching Storage.

As just described, the card reading or Sensing Storage, the Constant Storage, and the Intermediate Storage furnish the inputs to the Accumulator. The Intermediate Storage also communicates its stored results to Punching Storage (Fig. 10) via a panel of the Sensing-Punching Unit Plug Board (Fig. 7). This panel groups the Field columns of the card for punching results and also assigns the decimal position of each Field.

Punching Storage consists of 540 small magnets, one for each possible hole position in the card. These magnets trip interposers which block pins in the Punch Setting mechanism. All of the magnets related to the result numbers may be actuated by a single signal from the Electronic Computing Unit to a thyratron powered from the AC supply line. Thus the actual punching of the card does not take time out from the calculation. If the calculation is not finished before the Sensing-Punching machine cycle reaches normal, the clutch fails to trip for continuous operation and the machine stops till the signal comes. Thus no program can be too long for the

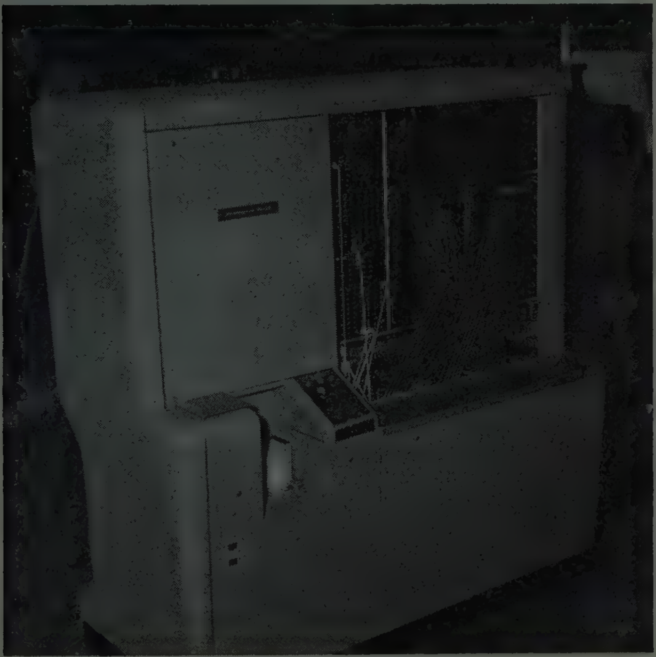


Fig. 7—The Sensing-Punching Unit with panel board uncovered. The card feeding magazine is in pocket at left, operator controls and indicators at right of magazine. The four plug-board panels are: (1) Calculator Input (lower center) with Decimal Setting Switch at left of each row; (2) Control Panel (vertical at left) which is plugged for controls and minus signs, Input in upper part and Output in lower part; (3) Calculator Output Panel (lower right) with Decimal Switches for setting decimal location of each row or field at the right; (4) Reproduce Panel (top right) containing 90 sockets for grouping of fields for alpha-numeric reproduction.

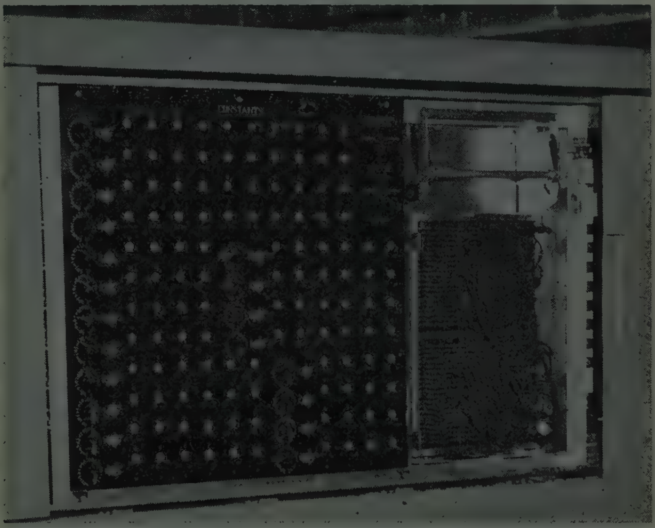


Fig. 8—The Constants Panel at upper left of Electronic Computer Unit has 20 rows of decade switches, plus or minus toggleswitch and a Decimal Setting switch at left end of each row. Program Plug Board, at right of Constants, has interchangeable panels with patch cords.

machine cycle. On some programs most of the cards feed at the continuous rate of 150 cards per minute while an occasional card may take longer.

Calculating Step

In the Program Plug Board there are forty Calculating Steps, each one just like all the others. Each step uses what might be called a five-address system. The first address locates the first operand, which may be any one of the 37 input numbers already enumerated; namely 9 Card Fields, 20 Constants, and 8 Intermediate Storages. One of four routines, add, subtract, multiply, or divide is designated in each step. The second address locates the second operand, again any one of the 37 inputs. The third address chooses one of the 8 Intermediate Storages for the result. Any number previously deposited there will be cleared automatically during the calculation. The fourth address indicates the next step to be performed in case the result is positive and the fifth address indicates the next step if the result is negative.

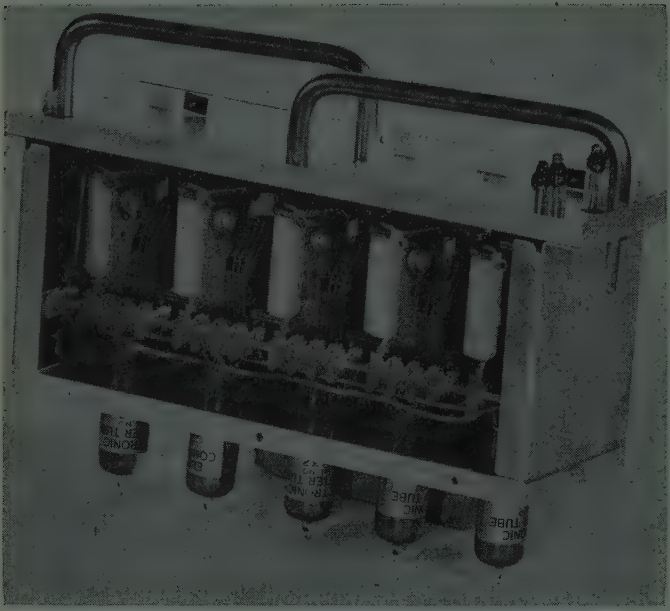


Fig. 9—An Intermediate Storage Relay chassis with phenolic side cover removed. Each side of a twin triode tube serves as a gate for one relay coil and each relay has 3 single-pole normally-open pairs of contacts.

Each of the 40 Calculating Steps calls for a subroutine which is common to all of these steps. First the Accumulator and the Intermediate Storage which is to receive the result are cleared to zero. Then a binary number locating the decimal position of the first operand is entered in the Decimal Computer, the sign is noted in the algebraic sign computer, and the first operand is registered (added) in the Accumulator.

The final signal from the above subroutine starts one of the four process routines, add, subtract, multiply, or divide.

The add and subtract routines enter the decimal position and sign of the second operand, shift the first operand to decimal alignment, call the second operand, add or subtract, enter the decimal position of the Intermediate Storage, shift the result to decimal alignment, add the number in storage which should be 0 and store the result including its sign. Before the result is stored, an overcarry may indicate a complementary number. A negative sign is temporarily stored in a flip-flop and the step is repeated from the beginning with signs reversed. This insures a true number result with a negative sign which is then stored. The proof of the result will be explained later.

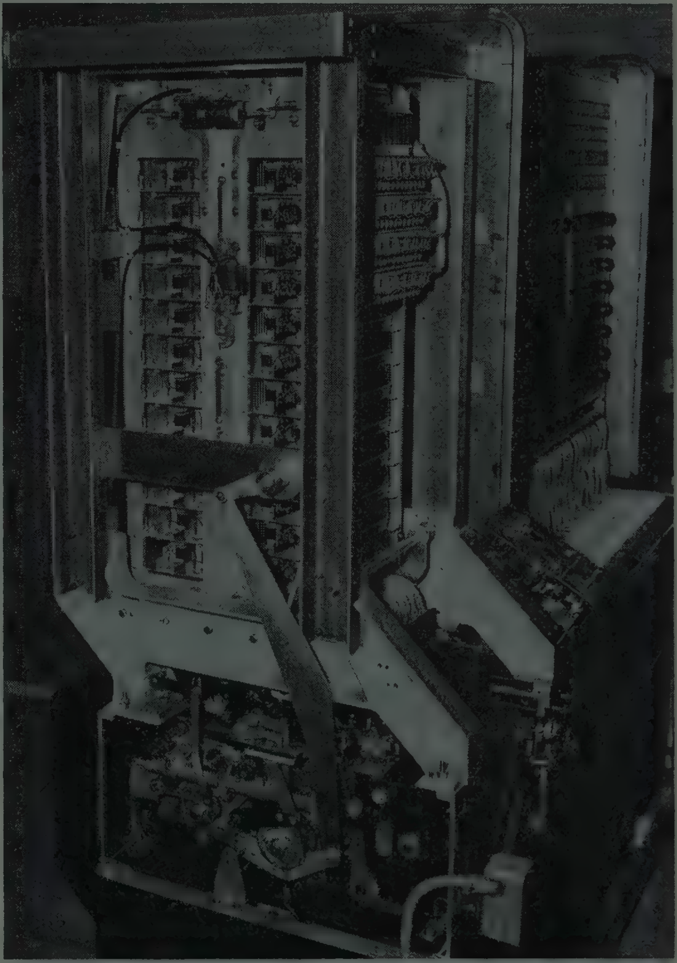


Fig. 10—The Sensing-Punching Unit with covers removed. Card feeding, sensing and punching mechanism is at lower center with Card Feeding Magazine and cables from Sensing Switches between sloping channels of frame at right front. Card Receiving Magazines are at bottom left and Punching Storage with shelves of Actuator Magnets at upper front.

The multiply routine enters the decimal position and sign of the multiplicand, shifts the multiplier (1st operand) till its first significant digit stands in column No.

22, adds the multiplicand, subtracts 1 from column 22 as many times as necessary to reduce that column to 0, shifts both multiplier and partial product till the next digit not equal to 0 appears in column 22, etc., till 10 shifts have taken place. The whole product, having a maximum of 20 digits, shifts until its first significant figure is in column 22. Columns 1 to 11 are cleared and the first 11 digits of the product are retained. All shifts have been added in the Decimal Computer. The decimal position of the Intermediate Storage enters, the products shifts to decimal alignment and is stored. Since the maximum capacity of all storages is 10 digits, one or more of the less significant figures are dropped when storing. The number of digits retained depends upon the plugging of the Output Panel of the Plug Board (Fig. 7). If rounding is required, at least one extra digit is stored, then another Calculating Step adds 5 in the next lower order than the desired least significant figure and when storing in that step the extra digits are dropped. In the beginning of the multiply routine both factors are tested and if either or both are found to be 0, the remainder of the routine is jumped over leaving the storage at 0.

The divide routine enters the decimal position and sign of the divisor (2nd operand), shifts the dividend (1st operand) till its first significant digit stands in column 22, subtracts the divisor and adds 1 in column 12 as many times as necessary to produce an overcarry from column 11. Then the divisor is added and 1 subtracted in column 12 once. The partial quotient and remainder are shifted one column, and the above operation is repeated 10 times after the first successful subtraction giving an eleven digit quotient, and the remainder is cleared. The decimal position of the storage is entered, the quotient is shifted to decimal alignment and stored. In the beginning of the divide routine the two operands are tested for 0. If the dividend is 0 and the divisor is not 0 the rest of the routine is jumped over leaving the storage at 0. If the dividend is not 0 and the divisor is 0 the program may stop the machine and light an indicator N/0, or sort out the card and proceed to the next card, or treat the result as if it were 0. If the dividend is 0 and the divisor is also 0 the program may stop the machine and light an indicator 0/0, or sort, or call the result 0 as above. It is not necessary to make the same choice for 0/0 as for N/0.

Square root, trigonometric functions, logarithms, etc., are handled by an iteration in the program.

PROVING

Every calculating step is proved by a reverse process. The programmer does nothing to accomplish this proof and has no control over it. In each step, after the result is stored, the routine calls for a proof routine which uses the add, subtract, multiply or divide routines in a different order. The result is read back into the Accumulator and operated upon by the two operands to produce a result which should be 0. These operations are as follows: Addition, $A+B=Y$; Proof: $Y-B-A=0$; subtraction, $A-B=Y$; Proof: $Y+B-A=0$; multiplication, $A\times B=Y$; Proof: $Y\div B-A=0$; division, $A\div B=Y$; Proof: $Y\times B-A=0$.

The result of the proving routine is tested for a value of 0 in the Accumulator. When it is not 0 it is usually because the less significant digits were dropped when storing, so a 1 is added in column 1 and the test repeated. If the proof result is still not 0 a signal is given to go back to the beginning of the step and try again. Or, if the programmer chooses, this signal may cause a new beginning of the whole program. The latter choice is not a good one if totals are being accumulated from card to card.

Thus the result of each calculating step, including the setting of storage, is proved before proceeding to the next step. Because of the self-checking feature, such things as intermittent grid-to-cathode shorts and marginal conditions definitely are prevented from causing arithmetical errors and may be allowed to exist until the trouble is frequent and thus easy to locate, or until an urgent job is finished.

PROGRAMMING

Programming is done by wiring a plug board with "patch cords" or jumpers. The 40 calculating steps described above are arranged in 40 rows beginning with #1 at the top. There are six other steps which will be described presently.

At the beginning of a "run" of cards the first cycle of the Sensing-Punching Unit feeds a card into the Sensing Chamber where it stops while the machine continues into its second cycle. Early in this cycle the Sensing Switches are set and a Calculator Start signal is given to the Computer Unit via a patch cord in the Program Plug Board which chooses the first step to be performed. Usually this is calculating step #1 although it may be any other. The Calculator Start signal can be programmed to be contingent upon the presence or absence of a certain hole or combination of holes in the card so that some cards are passed through without calculating.

After the first step has been calculated and proved either the fourth or fifth address is called depending on the sign of the result. Both addresses may call the same step or different steps and if the result can have but one sign a single patch cord is sufficient. Often the choice of a next step is a logical consideration. For example, in a payroll there may be several methods of payment, piece work, day work, etc., each class requiring a different sequence. If it happens that some Field is used on one class of card and not on others, a step can subtract a constant of 1 from the least significant column. If any value is punched in that Field the result will be positive and call for proceeding to the appropriate sequence. If no value is found the result will be negative and can call for another step which may be another logical test. A coded Control Position in some column can be treated in a similar fashion. A Control Position which means "male" to the operator may mean "3" to the computer and be compared with one or two constants.

Each Intermediate Storage is usually used many times. In logical steps the numerical value of the result means nothing so the storage can be used again on the next step. Most results are not needed except as an input to a succeeding step and as soon as that step has been figured the storage is available for another number.

All Intermediate Storages retain their numbers until cleared. Clearing is done in several ways: A Clear and Start switch on the Computer Unit enables the operator to clear all storages at the beginning of a run or after an interruption. As already described each step clears its particular storage during the computation. Sometimes a Calculating Step, such as subtracting any constant from itself, is used for the sole purpose of clearing a certain storage. One of the six steps other than the Calculating Steps is a Clear Step. This step may be entered from any other step and may be plugged to call for any other step after clearing. The storage or storages cleared by this step depend on a double throw switch for each storage.

Any result which is required to be punched in the card must be transmitted to Punching-Storage before clearing. If the programmer finds that no more storages are available because of outputs already stored he may call for entering another special step called Set I. This step will deliver any selected group of results to Punching-Storage and then call for the next step of the programmer's choice. Thus the storages relieved by Set I can be used for further calculation.

Another special step, Set II, will then be called for at the completion of the calculation.

Two other special steps are Sort I and Sort II. These are usually used after a logical choice where it is decided to separate this card from the deck. Either step causes the card to be ejected into a second receiving magazine. The reason for two such steps is that the outgoing address is usually different.

The sixth and last special step is the Trip. This is the final step of every program which announces to the Sensing-Punching Unit that it should either continue to run, or start again if it has stopped to await the filling of Punching-Storage.

After the Trip signal all results in Intermediate Storage are still retained. Some of these results may be useful in calculating the next card. For example, one or more storages may be used to accumulate subtotals, totals, and grand totals. Again, groups of two or more cards may be used for a single problem.

REPRODUCE

When the job involves groups of cards there is usually a header card at the beginning of a new group and often a trailer card for receiving totals, etc.

In the Sensing-Punching Unit Plug Board there is a panel marked Reproduce (Fig. 7). This panel can be plugged to pick up either alphabetical or numerical information from a header card and hold it for punching into the same or different Fields of following cards. Information may be sensed or read from one or more Fields and punched into other Fields of the same card.

At the same time there may be a computation (of prices, for instance) in the header card, the results of which are applicable to each of the following cards. These results may be computed by a special sequence consisting of regular program steps, and held in Punching Storage for reproduction in following cards, or in Intermediate Storage if the information is needed as input constants.

A trailer card may have its own special sequence in the program for recording totals, clearing related storages, etc.

SERVICE FEATURES

The complete complement of 1476 vacuum tubes and some of the 1128 cold-cathode gas diodes are mounted in four sizes of chassis which contain from 18 to 48 tubes each (Fig. 3). There are 428 relays mounted in another style of chassis (Fig. 9). Circuits are arranged so that each chassis serves a function which is recognizable to the serviceman. All chasses are pluggable, for quick change, and every probe point is accessible after removing a panel of the cover case.

A serviceman's switch panel under the covers of the Computing Unit enables him to stop the program not only at any step, but at any point within a step. Indicator lights enable him to read the Accumulator at that point in the program.

ACKNOWLEDGMENT

Development of the Model 409-2 Computer has been personally encouraged since its initiation by J. H. Rand and A. M. Ross with immediate executive direction of Gen. L. R. Groves. E. H. Dreher and his Laboratory Tabulator Department staff have been responsible for development of the Sensing-Punching Unit. Electronic Computer Department staff members have made valuable contributions to circuit design and construction features of the Electronic Calculating Unit, and J. A. Randmer has contributed in the development of special electron tubes. Acknowledgment also is made to J. J. Lamb for suggestions and editorial assistance in the preparation of this paper.

* * *

An Automatic Telephone System Employing Magnetic Drum Memory*

W. A. MALTHANER†, AND H. E. VAUGHAN†, SENIOR MEMBERS, IRE

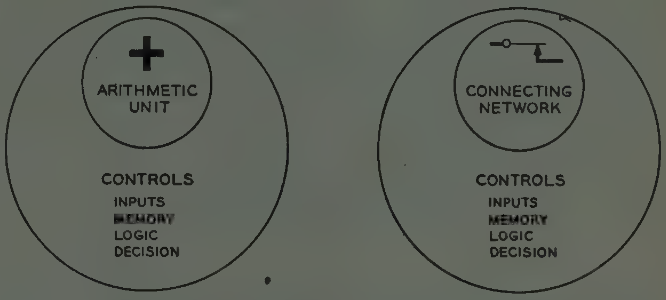
Summary—The use of magnetic drum memory in an automatic telephone switching office is described. A capacitive scanner acts as a time-division connector through which information generated by subscribers' telephone sets is conveyed to storage on magnetic drums. Information thus accumulated is combined with "permanent" information on the magnetic drums, processed in accordance with built-in programs and dispatched to control call switching circuits. Technical feasibility of this system has been demonstrated by the construction and successful operation of a large-scale laboratory model.

INTRODUCTION

IN ITS ELEMENTARY form an electrical switch is a two-value device, i.e. one which gives either an open or a closed circuit. It is actuated by corresponding binary control signals. From this basic concept switching systems of great complexity have been designed and built. These systems accept large quantities of input information; they combine it with permanently stored information; and they process the information through a sequence of internal operations under the control of a built-in program or under the control of input orders to obtain some final desired objective. Systems in which the desired output is simply a new set of information signals derived from the input data under control of stored orders are called computers. In such systems switching is merely the means by which some control signals process other control and data signals.

The common control telephone switching system may be considered as a kind of computer. In it, however, the final objective is the accurate establishment of paths which connect subscribers together and over which flows information that is not to be processed. In establishing these paths the input data are processed in computer-like circuits under control of stored orders. Thus, computers and switching systems are members of the same family. Either member of this family may be represented by a simple diagram as in Fig. 1. In the computer, represented by Fig. 1a, there is an arithmetic unit which performs the calculations desired by the customer. In an analogous position in the switching system, Fig. 1b, is a connecting unit which establishes the circuit desired by the subscriber. In neither case can this service section operate by itself. It must always have associated with it a control unit which includes input, output, memory and logic devices.

The automatic telephone switching system described in this paper is known as the DIAD system. The name DIAD, which refers primarily to the control parts of the system, is composed of the first letters of the words *Drum Information Assembler and Dispatcher*. This name emphasizes the fact that much of the input information is assembled in a magnetic drum memory, is processed and re-recorded on the drum, and from there is dispatched to control the connecting network and to supply control information to more remote parts of the over-all system. The recording of this information and the performance of the logic functions used in processing it are carried out by means of vacuum tubes and germanium diodes.



(a) (b)

Fig. 1—Comparison of computer and telephone system.
Fig. 1a—Computer. 1b—Telephone system.

DIAD was undertaken as a system project. The purpose of this project was mainly the study of the cooperation and interaction of several switching techniques and switching tools that had already been demonstrated separately. They were brought together not only to study a possible system as a whole but also to find out how these different pieces affect each other. In the basic design of this system a large size, heavy traffic telephone central office of 10,000 lines and 2,000 inter-office trunks was assumed. Its construction, of course, has been highly skeletonized.

A simplified diagram of the DIAD system is shown in Fig. 2. Here, subscriber lines are shown entering the connecting network from the left and inter-office trunks are shown leaving it at the right. The subscriber lines are continuously monitored by means of a capacitive scanner. Information as to the condition of the line and any request for service is recorded on the surface of the line drum in a slot which is permanently assigned to the particular line. From here a request for service is transferred to the trunk drum and recorded in the slot associated with a trunk that is capable of serving this particular request. From this trunk drum, orders are dispatched to the connecting network to establish the connection needed in this office and information is dispatched over the trunk to the distant office to permit completion of the call there.

---

* Decimal classification: 621.385×621.375.2. Original manuscript received by the Institute, June 23, 1953.

† Bell Telephone Labs., Inc., Murray Hill, N. J.

The DIAD System

In the following paragraphs the magnetic drum and associated scanner, the switching network and control system are described. Over-all operation of the switching system is treated by tracing the processes used in setting up a call from one subscriber to another. Many of the special features necessary in a commercial telephone system were omitted. The last part of the paper is concerned with the skeletonized laboratory system.

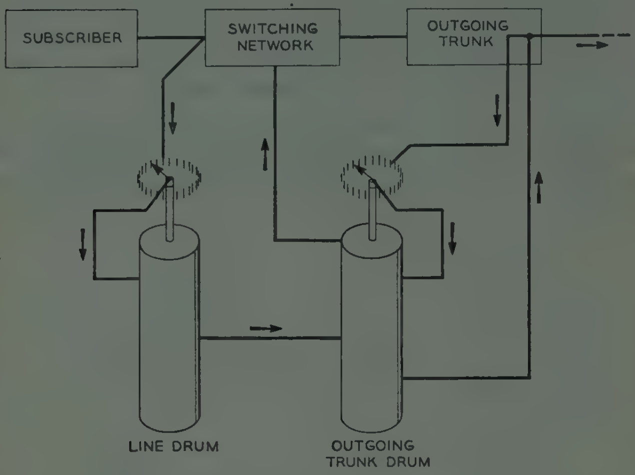


Fig. 2—General plan of DIAD.

A. Magnetic Drum and Capacitive Scanners

The magnetic drum provides storage for two classes of information. One class is the temporary detailed information relating to calls present in the system. Information in this class is accumulated during the establishment of a call, may be altered by the control circuits and is cleared from the memory when the call is removed from the system. The basic source of such temporary information is the telephone subset used by the subscriber. The capacitive scanner acts as a time-division connector through which information from subscribers' lines or from the trunks to which they have been connected is conveyed to the temporary storage channels of the magnetic drums. The other class of information defines the existing equipment designations and arrangements within the system. Data identifying the individual lines and trunks, and the class of service to which they are entitled or which they provide is an example of this type of information. Such information may be altered only by action on the part of the operating staff and is often referred to as the "permanent" information.

A small section of the magnetic drum and the capacitive scanner associated with it are shown diagrammatically in Fig. 3.

The rotating member of the capacitive scanner which carries a small electrode or plate past a cylindrical array of 1080 fixed plates is mounted on the same shaft as the drum. The moving plate forms a small capacitor with each fixed plate in succession so that the voltage condition on each fixed plate appears on a common output as a time-division signal approximately 60 times per second. Each line or trunk which is to supply information to the control circuits and magnetic drum is connected to a fixed plate in such a scanner.

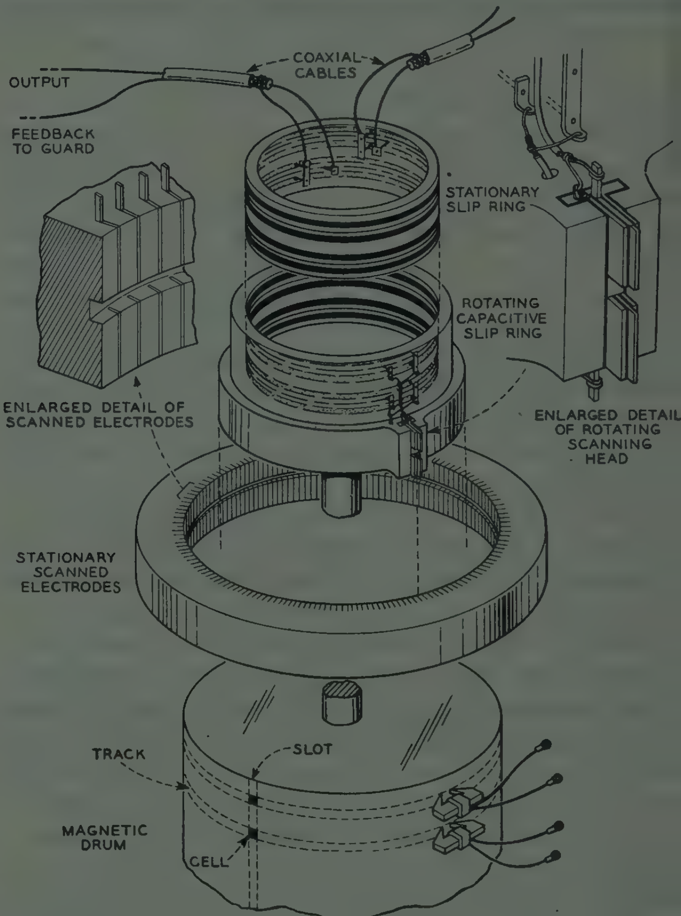

OUTPUT
FEEDBACK TO GUARD
COAXIAL CABLES
STATIONARY SLIP RING
ROTATING CAPACITIVE SLIP RING
ENLARGED DETAIL OF SCANNED ELECTRODES
ENLARGED DETAIL OF ROTATING SCANNING HEAD
STATIONARY SCANNED ELECTRODES
TRACK
SLOT
MAGNETIC DRUM
CELL

Fig. 3—Exploded diagram of scanner.

The area under a magnetic head during the time that one fixed plate is being scanned is called a cell. The aggregation of all cells which pass under one head is called a track and the aggregation of cells simultaneously under all the heads is called a slot. Each fixed plate of the scanner thus indexes a slot, and information both temporary and permanent pertaining to the line or trunk connected to the fixed plate appears in that slot. In the operation of the drum, information regarding a line or trunk is read from a number of the cells along one slot, acted upon by the control circuits and necessary changes in the information are made on the same revolution of the drum while this slot is still under the influence of the heads. Detailed treatment of this "single pass" method of operation is the subject of a companion paper, "Combined Reading and Writing on a Magnetic Drum" by J. H. McGuigan.

The mechanical characteristics of the drum used in the laboratory system are given in Table I.

TABLE I

Diameter	12″
Length	10″
Mounting	Vertical
Cells per track	1080
Tracks per inch	10
Speed	3450 rpm
Plating	Nickel cobalt

Referring again to the scanner, shown diagrammatically in Fig. 3, the rotating scanning plate is connected to the rotating plate of a capacitive slip ring. The scanner output is taken from a cathode follower connected to the concentric stationary plate of the capacitive slip ring. On each side of the scanning slip rings is a shield slip ring assembly. The output of the scanner cathode follower is connected back through these shielding slip rings to the shield of the scanning plate so that the loss due to combination of the low scanner coupling capacitance and the capacitance to ground is reduced.

The scanner has its mechanical characteristics outlined in Table II.

TABLE II

Fixed plates	.008″ wide, 1″ long
Fixed plate spacing	.040″ center to center
Space between plates	Grounded section insulated from plates
Scanning plate	.008″ wide, 1″ long, shielded
Scanning air gap	.006″ ±.0005″
Scanning capacitance	.2 $\mu\mu$f

The scanner associated with lines recognizes only two voltage conditions on these lines. The trunk scanner and its associated circuitry recognize five trunk voltage conditions: ground, high positive, low positive, high negative and low negative.

B. Switching Network

The switching network of this system was designed to connect any of 10,000 subscriber lines to any of 2,000 circuits known as trunks. The network uses reed-diode crosspoints[1] in a four stage array. Each crosspoint contains a relay with three metallic contacts, plus a cold cathode gas diode. Two of the contacts are used for the talking path, while the third contact and the gas diode are used for control purposes. In the first two stages the lines are switched to intermediate concentration points, known as junctors. In the last two stages distribution from these junctors to the outlets or trunks is accomplished. Information in the form of voltage steps is sent from the drum section of the system to the switching network controller which is made up chiefly of relays and cold cathode gas tubes. The network controller then applies voltage marks to the control leads of the crosspoints at the proper line and trunk terminals of the network. These voltage marks cause the gas diodes in the crosspoints connecting to the marked terminals to break down and trace idle paths leading toward the center of the network. A further selecting process causes the crosspoints of one of these idle paths through the network to be operated, after which the controller is released. When a connection is established in this system it is locked up. The release of a connection is controlled by information dispatched from the drum section after it has assembled the order for this action. The network and its controller require 0.023 seconds to establish a connection and 0.018 seconds to release a connection. The total of these two intervals is the time required for the network to serve any call and is well within the design objective of 0.050 seconds. Since control of the network is a function of an output of the control system, and the control system is the basic subject of this paper, no further treatment of the operation of the switching network will be given.

C. Control System

The control section of the system contains a number of control circuits subdivided in a manner which permits operations to be performed by one functional unit at the same time that operations on other calls are being performed by other functional units. Furthermore, the design is such that only a single functional unit of each type is required.

The number of common control circuits provided in a telephone switching system must be sufficient to comply with the service demands of practically all the subscribers with negligible delay when the number of such service demands is at its maximum. The number of each type of circuit to be provided depends on the maximum rate at which its functions are required and upon the total length of time one circuit of the type takes to perform these functions. This time per single usage is known as the holding time and includes subdivisions of time for gaining access to the circuit, for the registration of orders and data in it, for connecting it to the equipment to be controlled, for actually executing the control orders and for restoring it to the normal idle condition. Obviously the number of control equipments required will be reduced if their holding time is reduced. The fundamental objective, of course, is to reduce holding times sufficiently that only one of each type of control unit will be required. This can be done only by introducing higher speed devices into the telephone system.

One section of the control system serves lines and another serves trunks. One magnetic drum and its associated circuits may be associated with 1,000 lines or 1,000 trunks. Thus, the large office under consideration would require at least twelve drums. Bits of data representing an address or other information for a particular line or trunk are registered on or removed from the drum in parallel rather than as a series of pulses. Each decimal digit is coded into a five place binary number which is single error indicating, two of the five places always being filled.

---

[1] W. A. Malthaner and H. E. Vaughan, "An electronically controlled automatic switching system," *Bell Sys. Tech. Jour.*, May, 1952.

A check is performed on all data each time it is read from the memory. If the data conforms to the code, control functions proceed. If an error is detected, a trouble mark is recorded on the drum slot containing this data. The control system takes information generated by a subscriber and records it in memory until an amount has been accumulated which is sufficient for use in the next program step.

A built-in program directs the information through the main stages. Information is transferred from one drum to another. In the course of this operation the information removed from any drum must be stored in a temporary register until the next storage position is located. The temporary registers are vacuum tube devices and the logical functions of control are performed by combinations of tubes and germanium diodes. Programing is accomplished by a series of call progress marks, one of which is written on the drum each time a new stage in the program is reached. At several stages in the program a decision is made as to which subroutine is to be followed. For instance, the end of dialing may occur after one, three or seven digits. The dialed information is checked against permanently registered information to see whether sufficient information is at hand after each of the above mentioned digits. When sufficient information has been accumulated, the program proceeds to the next step. After completion of dialing, information is dispatched to the switching network and when necessary to the signaling transmitter. The control system provides a three digit dialing register for each subscriber and a complete dialing register for each trunk. The control circuits for the subscriber register are used on a time division basis with each subscriber having access to the register for 16 microseconds every 1/60 of a second. In common control systems it is advantageous that the directory number bear no relation to the location of a line or trunk on the switching network. This requires a translation function. The control system provides a bilateral translating function so that if a subscriber's directory number is known, his equipment number or the designation of his position on the switching network can be found, and vice versa. Thus, the location on the network may be readily changed to equalize the traffic offered to each switch.

Interoffice signaling in this system is performed by pulse-code-modulation using double-sideband carrier. The code is two-out-of-five and digits are sent at the rate of 150 digits per second with a 1,500 cycle per second carrier. A dc "signaling connect" signal is sent from the originating to the terminating office. The terminating office in turn starts the originating office transmitter by sending to it a 2,250 cycles per second "start" tone.

This brief discussion of the switching network and control system serves as an introduction to the operation of the system.

Tracing a Call

The over-all operation and interpretation of the functions may be more readily understood by tracing the steps in setting up a call in the system as described in the following paragraphs. A functional block diagram of the system used to connect a subscriber in one office to a subscriber in another office of the same type is shown in Fig. 4.

A. Accumulation of Dialed Office Code

To place a call in this system, a subscriber merely removes the handset from the telephone cradle and immediately begins to dial in the conventional manner. No dial tone is provided since one of the segments on the line scanner and an associated slot on the line drum are permanently assigned to each line and are always immediately available. Closures and opens of a subscriber line are detected by use of the line scanner, and control the Dialing Assembler circuit. Tracks on the line drum are used by the Assembler to provide a record of the condition of the line on the previous scan and of the initial line closure. Other tracks are used in timing the duration of a scanned condition. The use of the scanner and these auxiliary memory and timing tracks permit, among other things, the recognition of each dial pulse and each interdigital interval. The pulses of each digit dialed are counted and accumulated in other tracks on the drum slot.

B. Selection and Assignment of Outgoing Trunk

The first three digits dialed are used, after accumulation on the line drum, to select and assign to the calling line a slot on the trunk drum corresponding to an idle trunk to the destination designated by these digits. This office code dialed by a subscriber is held in the Dialed Information Dispatcher and is matched in the Out Trunk Selector against office codes read from successive slots of the trunk drum. When an idle trunk to the proper destination is thus found, the trunk is marked busy and assigned to the calling subscriber by recording the equipment number of the calling subscriber in the trunk drum slot.

C. Accumulation of Dialed Line Number

The digit register space on the line drum is cleared as a trunk is selected. The subsequently dialed numerical digits of the called line directory number are accumulated on the line slot by the Dialing Assembler and transferred one at a time through the Dialed Information Dispatcher to storage on the assigned slot of the trunk drum. The proper trunk slot is located by matching in the Called Number Assembler between the line equipment number which accompanies a dialed digit from the line drum and line equipment numbers previously recorded on the trunk drum in the trunk selection process.

D. Establishment of Originating Talking Path

As soon as the complete called number is stored on the trunk drum, the equipment number of the calling line and the equipment number of the assign trunked are read from the drum into the Switching Information Dispatcher and used to establish a corresponding path through the switching network.

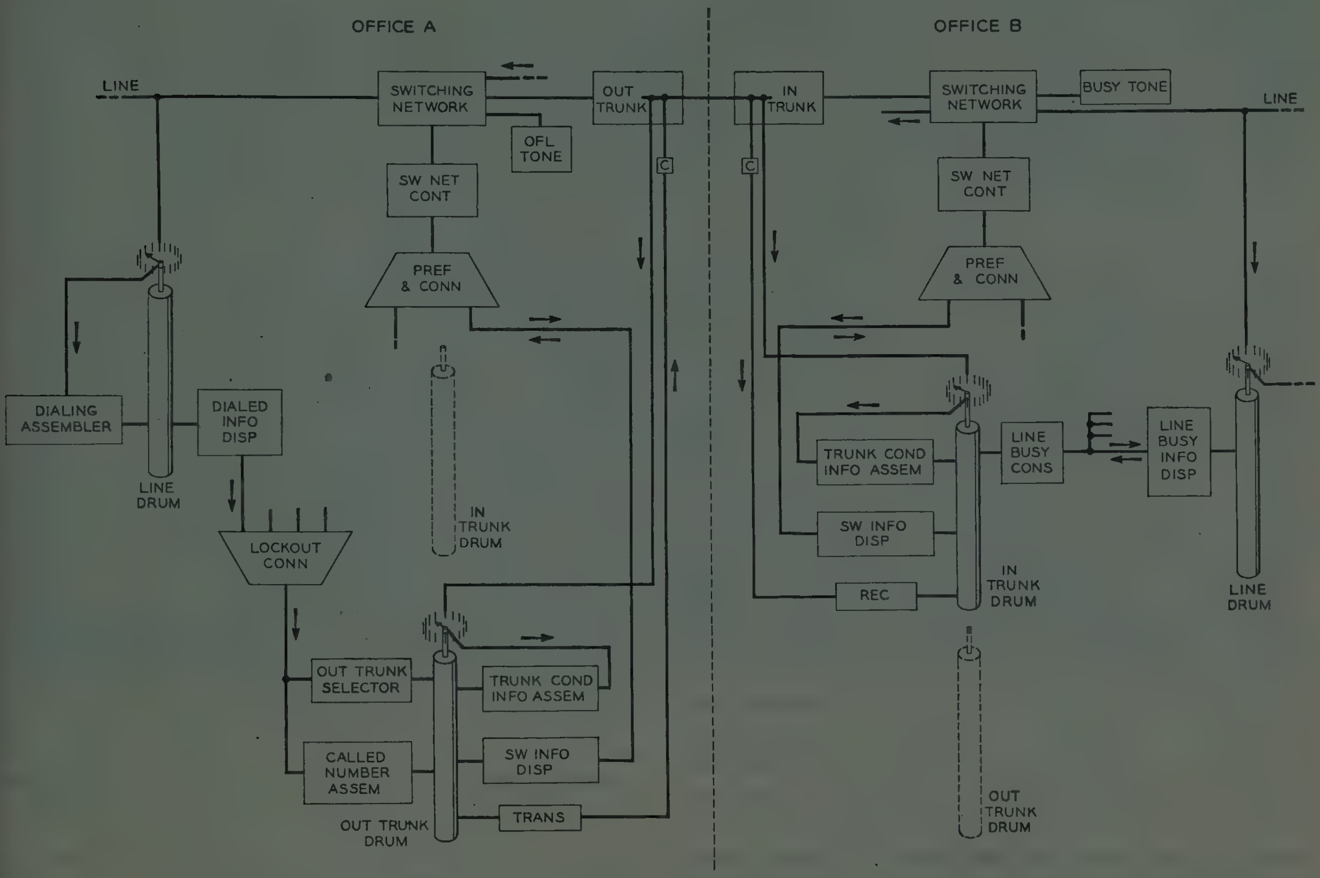

OFFICE A
OFFICE B
LINE
SWITCHING NETWORK
OUT TRUNK
OFL TONE
SW NET CONT
PREF & CONN
C
DIALING ASSEMBLER
DIALED INFO DISP
LINE DRUM
LOCKOUT CONN
IN TRUNK DRUM
OUT TRUNK SELECTOR
TRUNK COND INFO ASSEM
CALLED NUMBER ASSEM
SW INFO DISP
TRANS
OUT TRUNK DRUM
IN TRUNK
SWITCHING NETWORK
BUSY TONE
LINE
C
SW NET CONT
PREF & CONN
TRUNK COND INFO ASSEM
LINE BUSY CONS
LINE BUSY INFO DISP
SW INFO DISP
REC
IN TRUNK DRUM
LINE DRUM
OUT TRUNK DRUM

Fig. 4—Two-office block diagram.

E. Interoffice Signaling

When the connection between the calling subscriber and the outgoing trunk has been established, information from the trunk drum slot to the Signaling Dispatcher and Transmitter causes interoffice signal transmitting equipment to be connected to the outgoing trunk. A "connect" signal is then transmitted from the originating office and detected by use of the trunk scanner in the terminating office, and information from the trunk drum slot in the terminating office causes signal receiving equipment to be connected to the incoming trunk. The signal receiver informs the signal transmitter of its presence by transmitting a voice frequency "start tone" over the trunk for a short interval. In response the transmitter sends the line directory number of the called subscriber to the terminating office by pulse code modulated signals. In the terminating office the received number is recorded on the trunk drum slot corresponding to the trunk in use.

F. Translation of Line Directory Number to Equipment Number

Before a connection through the switching network can be established to the called line whose directory number is now stored on an incoming trunk slot, the idle or busy condition of the line must be ascertained and a corresponding line equipment number obtained. For this information the trunk drum through the Line Busy Consulter consults the Line Busy Information Dispatchers at the line drums using the line directory number as an address. The called line equipment number, or a substitute if the line is busy, when received from a line drum is recorded on the trunk drum in the proper slot.

G. Establishment of Terminating Talking Path

This line equipment number and the equipment number of the incoming trunk are then read from the drum into the Switching Information Dispatcher and used to establish the final section of the talking path through the switching network.

H. Ringing, Answer and Busy Tone

Ringing is applied to the called line by the incoming trunk. It is removed on the answer of the called subscriber at which time conversation may begin. The answer condition is recognized by use of the trunk scanners and recorded on the trunk drums in both the calling and called offices. If the called line is busy, the call is terminated through the switching network to a source of tone which the calling subscriber recognizes as a busy signal.

I. Hang-Up Operations

The trunk and line scanners are also used to detect the hang-up of subscribers. The duration of a hang-up condition is timed by the drum circuits and after a minimum interval the release of connections through the switching network is ordered by the trunk drums. After the release of such a connection, the temporary call information is erased from the drums.

SKELETONIZED LABORATORY SYSTEM

As mentioned above, the paper design of the system was for a heavy traffic 10,000 line office. Time studies were made to be sure that each common control functional unit would handle the information offered to it in the busy hour. The actual laboratory system constructed for feasibility, operation and maintenance studies was skeletonized, to conserve manpower and space. However, most of the functions in the paper system were included as the skeletonization was in the number of bits used for an address or identification rather than in the number of functions.

The system uses a single magnetic drum to serve both line and trunk drum sections. Two scanners each equipped with forty scanned plates are coupled to the drum. The spacing of the plates is the same as that required for accommodating 1080 plates in this circumference. All of the vacuum tube and germanium diode circuits, the signaling system, and the switching network are contained in ten standard relay rack cabinets, 19 inches wide by 7 feet high, set on a raised platform. Cabling between bays is in ducts located under the platform. A forced air system is used to remove much of the heat dissipated in the system. Two of the bays house the line drum section; two, the trunk drum section; and one, the signaling system. Two of the bays house the switching network and its controls. The switching network has been skeletonized to 27 lines and 12 trunks, but about half of the control required for a full size office has been provided. The other three bays house power supplies and miscellaneous control equipment. The laboratory setup is shown on Fig. 5.

CIRCUITRY

Temporary storage and logic circuits are used as an intermediate means for assembling and dispatching drum information. Although the time slot allotted to each line or trunk is 16 μsec, in "single pass" operation the time between the start of reading and the start of writing is only 2 μsec. Since several functions must be carried out in sequence in this period, the circuits must respond in tenths of μsec. This requirement increases the equipment layout and construction problems if economy is to be observed with respect to power furnished by regulated supplies. The circuitry in parts of the system where such speeds obtain is what might be termed "high impedance-high voltage" circuitry. The magnitude of pulses and steps is in the order of 60 v from source impedances which vary from 3,000 to 7,500 ohms. The majority of the circuits are connected to each other on a dc basis. In some cases impedance transformation is afforded by cathode followers.

Where information is passed from one drum section to another, the holding times of the control circuits may vary from a few μsec to several milliseconds, thus requiring that circuits used for these functions also operate at relatively high speed. When information is dispatched to control switching or signaling circuits the holding times are several msec and thus the response of these circuits may be considerably slower.

The logic circuits use vacuum tubes and germanium diodes. Approximately 1,100 vacuum tubes and 2,200 germanium diodes are used. More than three-fourths of the tubes used are 2C51 while several 5687 tubes are used where more power is required. The regulated dc voltage supplies range from +300 to −150 v. The total power consumed in the system is approximately 10 kw.

DEMONSTRATION BOARD

A demonstration and maintenance board in the form of a functional block diagram was built. In each block neon indicator lamps connected to the system show which functional blocks are in use, the condition of the register units, and give an indication of the call progress marks. This display board is shown mounted above the laboratory bays in Fig. 5. A manual control console is provided with a group of keys which are connected to the controlling gates of the circuit associated with each functional block. By this means a call may be allowed to proceed step by step under manual control with the lamps giving a visual picture of the operation of the system. In a similar manner the maintenance man can trace a call through step by step and when a stage in trouble is reached, he can cause the visual indication to be held or repeated. When all keys are normal, calls proceed automatically at the regular speed.

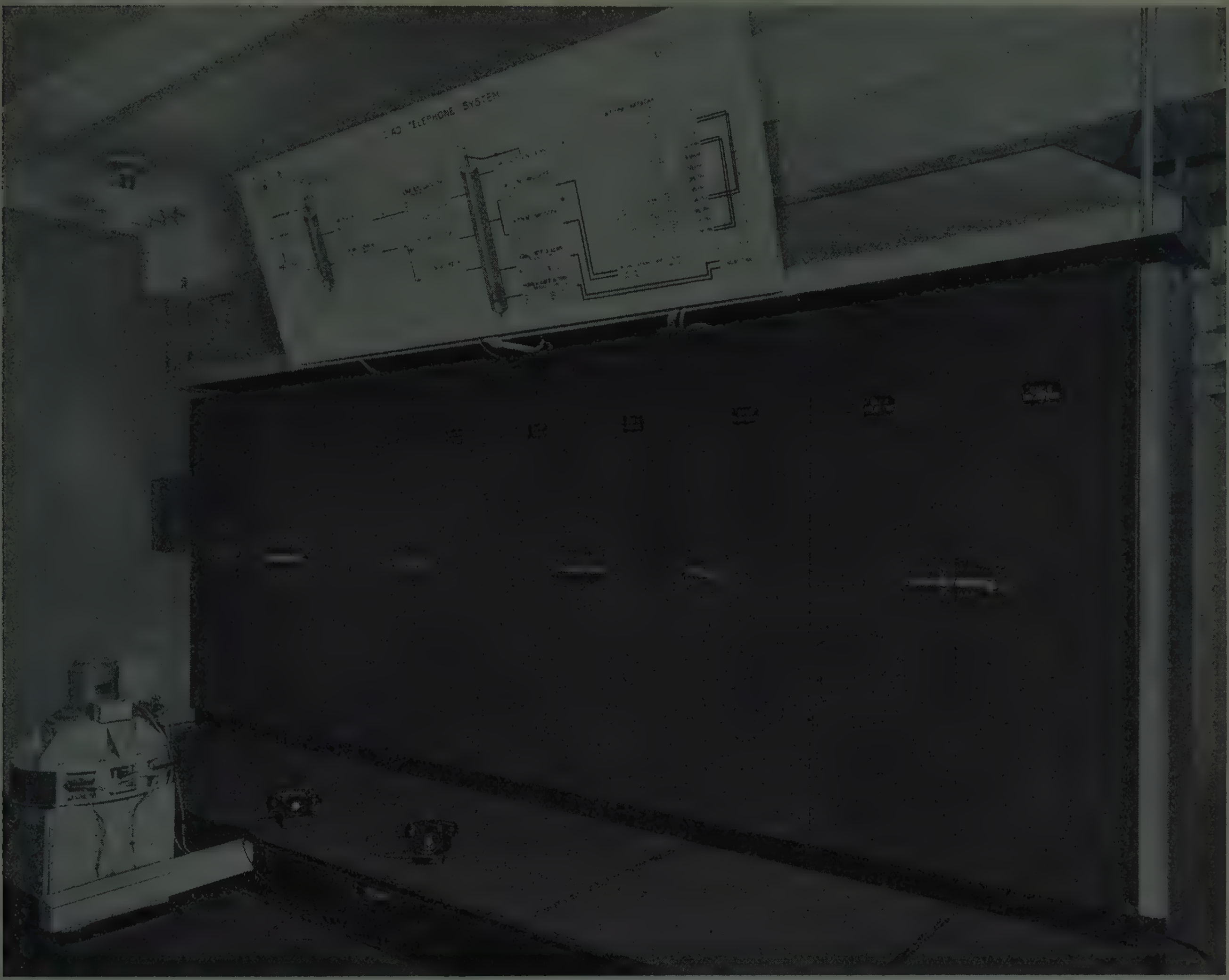


Fig. 5—Laboratory installation.

CONCLUSIONS

The construction and test of the laboratory system has shown that such a system is technically feasible and has set a course for the investigation of advanced circuit techniques applicable to switching. During the laboratory phase of this system new tools, such as the ferroelectric storage cell, have been developed and transistors have become more readily available. The use of these new tools would do much to reduce both the size and power consumption of the system. Recent advances in the art of switch configuration would also tend to simplify the system.

ACKNOWLEDGMENT

The success of a project of the magnitude of DIAD is dependent on the effort of many people. The accomplishments in the magnetic drum and scanner field were the work of J. H. McGuigan, O. J. Murphy, W. A. Cornell and N. D. Newby. The magnetic drum unit in the laboratory system was designed and furnished by F. G. Buhrendorf and H. A. Henning. The switching network is the work of S. T. Brewer, E. Bruce and G. Hecht. Mechanical design is due primarily to J. F. Muller. Acknowledgment must also be given to numerous other associates who assembled and tested the actual system.

* * *

Machine Aid for Switching Circuit Design*

CLAUDE E. SHANNON†, FELLOW, IRE AND EDWARD F. MOORE†, ASSOCIATE, IRE

Summary—The design of circuits composed of logical elements may be facilitated by auxiliary machines. This paper describes one such machine, made of relays, selector switches, gas diodes, and germanium diodes. This machine (called the relay circuit analyzer) has as inputs both a relay contact circuit and the specifications the circuit is expected to satisfy. The analyzer (1) verifies whether the circuit satisfies the specifications, (2) makes systematic attempts to simplify the circuit by removing redundant contacts, and also (3) obtains mathematically rigorous lower bounds for the numbers and types of contacts needed to satisfy the specifications. A special feature of the analyzer is its ability to take advantage of circuit specifications which are incompletely stated. The auxiliary machine method of doing these and similar operations is compared with the method of coding them on a general-purpose digital computer.

INTRODUCTION

SOME OPERATIONS which assist in the design of relay circuits or other types of switching circuits can be described in very simple form, and machines can be constructed which perform them more quickly and more accurately than a human being can. It seems possible that machines of this type will be useful to those whose work involves the design of such circuits.

The present machine, called the relay circuit analyzer, is intended for use in connection with the design of two terminal circuits made up of contacts on at most four relays. The principles upon which this machine is based are not limited to two terminal networks or to four relays, although an enlarged machine would require more time to operate. Each addition of one relay to the circuits considered would approximately double the size of the machine and quadruple the length of time required for its operation. This type of machine is not applicable to sequential circuits, however, so it will be of use only in connection with parts of the relay circuits which contain contacts, but no relay coils.

OPERATION OF THE MACHINE

The machine, as can be seen from Fig. 1, contains sixteen 3-position switches, which are used to specify the requirements of the circuit. One switch corresponds to each of the $2^4=16$ states in which the four relays can be put. Switch number two in the upper right hand corner, for instance, is labeled $W+X+Y'+Z$, which corresponds to the state of the circuit in which the relays labeled W, X, and Z are operated, and the relay labeled Y is released.

The three positions of this switch correspond to the requirements which can be imposed on the condition of the circuit when the relays are in the corresponding state. Since any single relay contact circuit assumes only one of two values (open or closed) the inclusion of a third value (doesn't matter, don't care, or vacuous, as it has been called by various persons) merits some explanation. If the machine, of which the relay circuit being designed is to be a part, only permits these relays to take on a fraction of the 2^n combinations of which n relays are capable, then it will not matter what the circuit does in the excluded states. The user indicates the optional nature of these requirements by placing the corresponding switches in the "don't care" positions. With these options, there is a wider range of circuits satisfying the requirements, and hence more likelihood that a circuit with fewer contacts will suffice. The sixteen 3-position switches thus permit the user not only to require the circuit under consideration to have exactly some particular hindrance function, but also allow the machine more freedom in the cases where the circuit need not be specified completely.

In order to make a machine of this type to deal with n relays (this particular machine was made for the case $n=4$), 2^n such switches would be required, corresponding to the 2^n states n relays can assume. In each of these states the circuit can be either open or closed, so there are 2^{2^n} functionally distinct circuits. But since each switch has 3 positions, there are 3^{2^n} distinct circuit requirements specifiable on the switches, which in the case $n=4$ amounts to 43,046,721. Thus, the number of problems which the analyzer must deal with is quite large, even in the case of only four relays.

The left half of the front panel of the machine (see Fig. 1) is a plugboard on which the circuit being analyzed can be represented. There are three transfers from each of the four relays, W, X, Y, and Z brought out to jacks on this panel, and jacks representing the terminals of the network are at the top and bottom. Using patch cords, it is possible to plug up any circuit using at most three transfers on each of the four relays. This number of contacts is sufficient to give a circuit representing any switching function of four variables.

If the specifications for the circuit have been put on the sixteen switches, and if the circuit has been put on the plugboard, the relay circuit analyzer is then ready to operate.

With the main control switch and the evaluate-compare switch both in the "evaluate" position, pressing the start button will cause the analyzer to evaluate the circuit plugged in, i.e. to indicate in which of the states the circuit is closed by lighting up the corresponding indicator lamps.

Turning the evaluate-compare switch to the "compare" position, the analyzer then checks whether the

---

* Decimal classification: 621.375.2×R257. Original manuscript received by the Institute, May 28, 1953; revised manuscript received June 29, 1953.

† Bell Telephone Laboratories, Inc., Murray Hill, N. J.

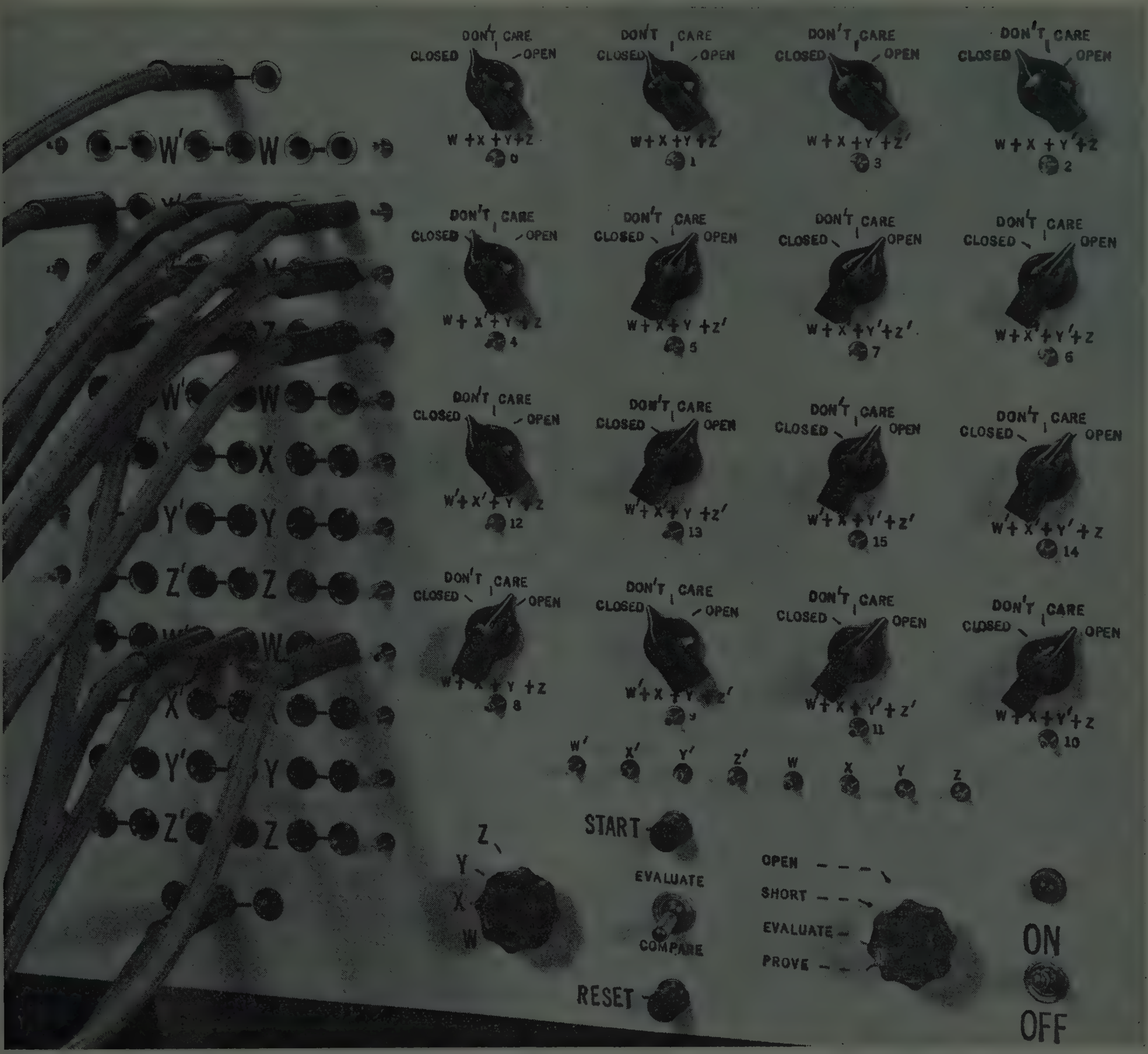

DON'T CARE
CLOSED
OPEN
W+X+Y+Z
0
W+X+Y+Z'
1
W+X+Y'+Z'
3
W+X+Y'+Z
2
W+X'+Y+Z
4
W+X'+Y+Z'
5
W+X'+Y'+Z'
7
W+X'+Y'+Z
6
W'+X'+Y+Z
12
W'+X'+Y+Z'
13
W'+X'+Y'+Z'
15
W'+X'+Y'+Z
14
W'+X+Y+Z
8
W'+X+Y+Z'
9
W'+X+Y'+Z'
11
W'+X+Y'+Z
10
W'
W
X
Y'
Y
Z'
Z
W'
X'
Y'
Z'
W
X
Y
Z
START
EVALUATE
COMPARE
RESET
OPEN
SHORT
EVALUATE
PROVE
ON
OFF

Fig. 1—View of front panel of the relay circuit analyzer.

circuit disagrees with the requirements given on the switches. A disagreement is indicated by lighting the lamp corresponding to the state in question. If a switch is set for closed and the actual circuit is open in that state, or vice versa, a disagreement is indicated, but no disagreement is ever registered when the switch is set in the "don't care" position, regardless of the circuit condition. The compare position, while it gives information equivalent to that given in the evaluate position, gives it in a form more convenient for noticing errors.

After a circuit has been found which agrees entirely with the requirements, the main control switch is then turned to the "short test" position and the start button is pressed again. The machine then determines whether any of the contacts in this circuit could have been shorted out, with the circuit still satisfying the requirements. The machine indicates on the lamps beside the contacts which ones have this property.

It may be surprising to the reader that anyone would ever need the assistance of a machine to find a contact which could be shorted out without affecting its circuit. While this is certainly true of simple examples, in more complicated circuits such redundant elements are often far from obvious (particularly if there are some states for which the switches are in the "don't care" position, since the simplified circuit may be functionally different from the original one, as long as it differs only in the "don't care" state). It is often quite difficult to see the simplification in these cases.

The analyzer is also helpful in case the circuit being analyzed is a bridge, because of the complications involved in tracing out all paths in the bridge. The circuit shown in Fig. 2 is an example of a circuit which was not known to be inefficiently designed until put on the analyzer. It determined in less than two minutes (including the time required to plug the circuit into the plugboard) that one of the contacts shown can be shorted out. How likely would a human being be to solve this same problem in the same length of time?

After the short test has been performed, putting the main control switch in the "open test" position permits the analyzer to perform another analogous test, this time opening the contacts one at a time.

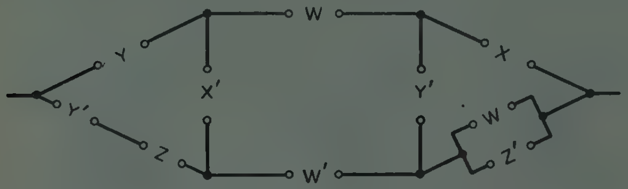


Fig. 2—The relay circuit analyzer was able to simplify this circuit, removing one contact, in less than two minutes total time. Can you do as well?

These two particular types of circuit changes were chosen because they are easy to carry out, and whenever successful, either one reduces the number of contacts required. There are other types of circuit simplification which it might be desirable to have a machine perform, including various rearrangements of the circuit. These would have required more time as well as more equipment to perform, but would probably have caused the machine to be more frequently successful in simplifying the circuit. Using such techniques, it might be possible to build a machine which could design circuits efficiently starting from basic principles, perhaps by starting with a complete Boolean expansion for the desired function and simplifying it step by step. Such a machine would be rather slow (unless it were built to operate at electronic speeds, and perhaps even in this case), and not enough planning has been done to know whether such a machine is practically feasible. However, the fact that such a machine is theoretically possible is certainly of interest, whether anyone builds one or not.

Another question of theoretical interest is whether a logical machine could be built which could design an improved version of itself, or perhaps build some machine whose over-all purpose was more complicated than its own. There seems to be no logical contradiction involved in such a machine, although it will require great advances in the general theory of automata before any such project could be confidently undertaken.

To return to the relay circuit analyzer, a final operation which it performs is done with the main control switch in the *prove* position. Pressing the start button and moving the other 4-position switch successively through the W, X, Y and Z positions, then certain of the eight lamps W, W', X, X', Y, Y', Z, Z' will light up. The analyzer has carried out a proof as to which kinds of contacts are required to synthesize the function using the method of reduction to functions of one variable, which will be explained in a forthcoming paper. The analyzer here ignores whatever circuit has been plugged in the plugboard, and considers only the function specified by the sixteen 3-position switches. If every circuit which satisfied these specifications requires a back contact on the W relay, the W' light will go on, etc.

If, for instance, seven of the eight lights are on, any circuit for the function requires at least seven contacts, and if there is, in fact, a circuit which uses just seven, the machine has in effect, given a complete proof that this circuit is minimal. Circuits for which the machine can give such a complete proof are fairly common, although there are also circuits (which can be shown to be minimal by more subtle methods of proof) which this machine could not prove minimal. An example is the circuit of Fig. 2. This can be simplified by the analyzer to a circuit of nine contacts, but in the *prove* position the analyzer merely indicates that at least eight contacts are necessary. It can be shown by other methods that the 9-contact circuit is minimal. But at any rate, the analyzer always gives a mathematically rigorous lower bound for the number of contacts.

The small size and portability of this machine depends on the fact that a mixture of relay and electronic circuit elements were used. The gas diodes are particularly suited for use where a small memory element having an associated visual display is required, and the relays and selector switches are particularly suited for use where the ability to sequence and interconnect, using only a small weight and space, is required. In all, the relay circuit analyzer uses only 24 relays, 2 selector switches, 48 miniature gas diodes, and 14 germanium diodes as its logical elements.

It may be of interest to those familiar with general purpose digital computers to compare this method of solution of this problem on such a small, special-purpose machine with the more conventional method of coding it for solution on a high-speed general-purpose computer. One basic way in which the two methods differ is in the directness with which the circuits being analyzed are represented. On a general-purpose computer it would be necessary to have a symbolic description of the circuit, probably in the form of a numerical code describing the interconnections of the circuit diagram, and representing the types of contacts that occur in the various parts of the circuit by means of a list of numbers in successive memory locations of the computer. On the other hand, the relay circuit analyzer represents the circuit in a more direct and natural manner, by actually having a copy of it plugged up on the front panel.

This difference in the directness of representation has two effects. First, it would be somewhat harder to use the general-purpose computer, because the steps of translating the circuit diagram into the coded description and of typing it onto the input medium of the computer would be more complicated and lengthy than the step of plugging up a circuit directly. The second effect is in the relative number of logical operations (and hence, indirectly, the time) required by the two kinds of machines. To carry out the fundamental step in this procedure of determining whether the given circuit (or some modification of it obtained by opening or shorting a contact) is open or closed for some particular state of the relays, requires only a single relay operate time for the relay circuit analyzer. However, the carrying out of this fundamental step on a general-purpose digital computer would require going through several kinds of subroutines many times. There would be several ways of coding the problem, but in a typical one of them the computer would first go through a subroutine to determine whether a given contact were open or closed, repeating this one for each contact in the circuit, and then would go through another subroutine once for each node of the network. Altogether this would probably involve the execution of several hundred orders on the computer, although by sufficiently ingenious coding this might be cut down to perhaps 100. Since each order of a computer takes perhaps 100 times the duration of a single logical operation (i.e., a pulse time, if the computer is clock-driven), actually what takes 1 operation time on one machine takes perhaps 10,000 on another.

Since 10,000 is approximately the ratio between the speed of a relay and of a vacuum tube in performing logical operations, this gain of about 10,000 from the directness of the representation permits this relay machine to be as fast at this kind of problem as a general-pupose electronic computer.

This great disparity between the speeds of a general-purpose and of a special-purpose computer is not typical of all kinds of problems, since a typical problem in numerical analysis might only permit of a speed-up by a factor of 10 on a special-purpose machine (since multiplications and divisions required in the problem use up perhaps a tenth of the time of the problem). However, it seems to be typical of combinatorial problems that a tremendous gain in speed is possible by the use of special rather than general-purpose digital computers. This means that the general-purpose machines are not really general in purpose, but are specialized in such a direction as to favor problems in analysis. It is certainly true that the so-called general purpose machines are logically capable of solving such combinatorial problems, but their efficiency in such use is definitely very low. The problems involved in the design of a general-purpose machine suitable for a wide variety of combinatorial problems seem to be quite difficult, although certainly of great theoretical interest.

CONCLUSIONS

An interesting feature of the relay circuit analyzer is its ability to deal directly with logical circuits in terms of 3-valued logic. There would be considerable interest in techniques permitting easy manipulation on paper with such a logic, because of its direct application to the design of economical switching circuits. Even though such techniques have not yet been developed, machines such as this can be of value in connection with 3-valued problems.

Whether or not this particular kind of machine ever proves to be useful in the design of practical relay circuits, the possibility of making machines which can assist in logical design procedure promises to be of value to everyone associated with the design of switching circuits. Just as the slide rule and present-day types of digital computers can help perform part of the routine work associated with the design of linear electrical networks, machines such as this may someday lighten much of the routine work associated with the design of logical circuits.

* * *

The Design of the Bendix Digital Differential Analyzer*

MAX PALEVSKY†

Summary—The error reduction scheme employed by the Bendix Digital Differential Analyzer, which utilizes both ternary intercommunication between integrators and trapezoidal integration, is described. A device for the variation and automatic resetting of initial conditions is discussed together with an example illustrating its operation. Finally, techniques employed for minimizing the size of the computer are considered.

INTRODUCTION

A DIGITAL differential analyzer, which is a device for the solution of differential equations, can be considered a digital analog of analyzers of the Bush type.[1-3] The several produced thus far have had some success but are limited in two respects.

First, and most important, the errors arising from the numerical process of integration—truncation and round-off errors—restrict the class of soluble problems and multiply the time required for the working of such problems as do admit of solution.

Secondly, slow input/output systems not only impede efficient use of the equipment, but impose precisional limitations on the solution of the problems involving empirical inputs.

In designing the Bendix Digital Differential Analyzer, the aim has been to obviate these difficulties and, by introducing a new technique, to extend the range of problems amenable to treatment by a digital differential analyzer. The necessity of limiting the cost and complexity of the equipments so as to justify the existence of a special purpose computer operated as a constant control upon this aim. The expedients employed to satisfy this control will be considered in the second part of this paper; the first part will deal with the mathematics of the computer.

PART I

A digital differential analyzer consists of a number of fixed program digital integrators serially performing simple quadratures. The equation of the fixed program heretofore employed has been $Z=\int ydx$ or more accurately, $\Delta Z=Y\Delta X$. Effectively, this is Euler or rectangular integration. The reason for the latter term can readily be seen from Fig. 1. The area under the curve is approximated by summing a series of rectangles each with the area $Y\Delta X$. While promoting computational ease, the crudeness of the approximation introduces a large error term.

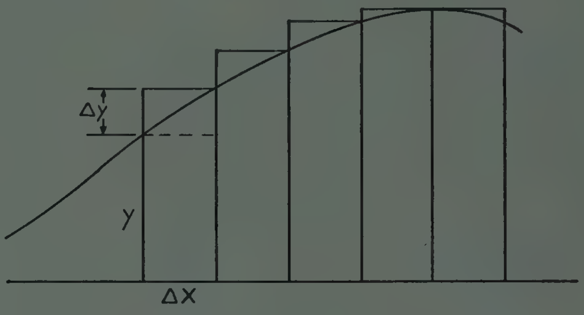


Fig. 1—Euler integration.

As a remedy the Bendix Digital Differential Analyzer employs what is commonly called the trapezoidal rule.

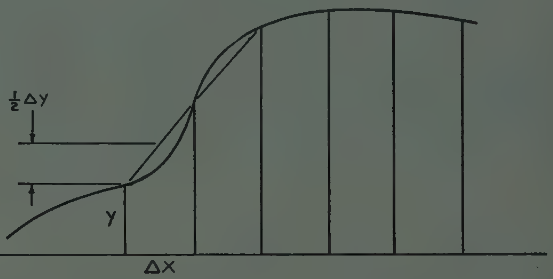


Fig. 2—Trapezoidal integration.

Here the fundamental area of integration is $(Y+\frac{1}{2}\Delta Y)\Delta X$ as illustrated in Fig. 2. The ratio of the new error term to the old is of the order of ΔX; where ΔX is some small fraction, the reduction is considerable.

A more serious source of error in many problems is round-off. This results not only from the finite length of the registers employed, but, in schemes hitherto used, from the binary system of integrator intercommunication. To understand the latter, it should be noted that functions are generated by the so-called "bootstrap" method; that is, the incremental inputs to a given in-

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 1, 1953.

† Research Analyst, Bendix Computer Division, Bendix Aviation Corp., Los Angeles, Calif.

[1] V. Bush, "The differential analyzer. A new machine for solving differential equations," *Jour. Frank. Inst.*, vol. 212, pp. 447–488; 1931.

[2] V. Bush and S. H. Caldwell, "A new type differential analyzer," *Jour. Frank. Inst.*, vol. 240, pp. 255–376; 1945.

[3] R. E. Sprague, "Fundamental concepts of the digital differential analyzer," Math. Tables and Other Aids to Computation, vol. VI, pp. 41–49; 1952.

tegrator are the outputs of other integrators. If each output must be either a plus or minus one, the round-off process introduces the error

$$-\Delta Z \leqq \epsilon \leqq +\Delta Z,$$

where $\Delta Z = Y\Delta X$. This is easily seen by considering an integrator that should have a zero output. Since -1 or $+1$ alone are available, the error will be a full unit of ΔZ. If this output is fed back into the integrator directly or through a short loop, the error is appreciable. In fact, in the event that such outputs are relatively frequent, the computation quickly becomes completely worthless. Generally, this occurs in two types of problems. If, in order to provide decision and adding elements, integrators are operated as servos, the error is large whenever the null position is reached. In like manner, an integrator holding a variable with a slowly changing integral will be unable to indicate those intervals in which the change is zero.

The solution adopted in the Bendix Digital Differential Analyzer is a ternary scheme of integrator intercommunication. Now the output of an integrator may be $+1$, 0, or -1, hence the error is

$$-\tfrac{1}{2}\Delta Z \leqq \epsilon \leqq +\tfrac{1}{2}\Delta Z.$$

Aside from the reduction in error, the additional equipment necessitated by ternary transfer is justified, it is felt, by the doubling of speed that immediately results. Probably the best way to see this is to consider the least significant binary digit in the Y register of a binary transfer computer. From the number of ΔY inputs and the number of iteration cycles, the value in this place can be deduced. Thus, for example, if there are three inputs, the ΔY number is always odd; hence, odd integration cycles will find a one in this place, and even cycles will find a zero. No significance may, consequently, be attributed to it. A ternary scheme restores the significance and, therefore, doubles the speed if the same precision is maintained.

A further reduction in the round-off error is effected by the method employed in mitigating the inefficiencies of decimal scaling. For reasons to be stated later, the computer operates in a coded decimal system. However, scaling in powers of ten permits fewer scale values than does scaling in powers of two. For example, between one and one million there are 20 binary as opposed to six decimal factors. Constant multipliers are, of course, the solution, but these may be one of two types. The first, indeed the only type used in previous machines, multiplies the output rate of an integrator by a fraction less than one. The round-off error in the original rate is not affected; however, it is augmented by the error resulting from the counting down process.

The second scheme—the one adopted—multiplies up the rate, hence the round-off is reduced by the factor of the multiplier. Two and five are provided and yield in our example 18 as opposed to the 20 scale factors of the binary system.

The provisions for error reduction and scaling ease so far discussed are logical outgrowths of earlier designs. An entirely new conception is embodied in the machine's mode of handling initial conditions. Once set into the machine, these may be reset at any stage in the computation by pressing a button. But more important, they may be varied as a function of any of the variables in the problem and then automatically reset so that computation is restarted from a new point. An example[4] is shown in Fig. 3. The differential equation

$$\ddot{Y} = AX + e^Y + C$$

is given with the boundary conditions

$$\dot{Y}_0 = -B \qquad \dot{Y}_f = 0$$

$$X_0 = 0 \qquad Y_f = 0,$$

the problem being to find Y_0 and X_f. The value of Y_0 is guessed, set onto the computer, and computation started.

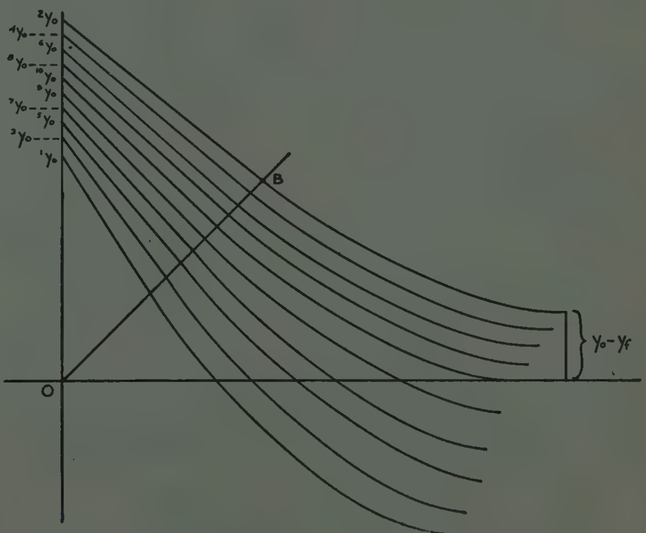


Fig. 3—Graph of the solution of $\ddot{Y} = AX + e^Y + C$ with split boundary conditions.

In addition to the normal use of Y_0 for generating one of the family of curves satisfying the equation, an error signal equal to Y_0 is set into a servo. The sum of the servo outputs is initially represented by that portion of the line OB extending from the origin to the curve Y.

---

[4] Appendix shows the integrator coding for this problem.

This intersection represents the null position and, since incremental values of Y are being fed into the servo, the output now "follows" the curve of Y. The output of the servo up to and including the point where $\dot{Y}=0$ will, therefore, be equal to $Y_0 - Y_f$. This output is first multiplied by a constant m, to reduce oscillations. The result is then used to generate $\Delta(e^Y)$, which is fed into the integrators holding e^Y as the initial condition of the next run. Computation is continuous until the boundary conditions are met, at which time the computer automatically stops.

If problems to be run on the computer involve no empirical functions and require no more integrators than are available, the input/output mechanisms are mathematically irrelevant. True, the actual time involved in communicating with the computer may be large when using a primitive scheme, but it is not of such an order as to render the computer useless. However, when empirical functions are involved, they must be supplied in incremental form at rates matching that of the computer.

The Bendix Digital Differential Analyzer operates at 100 iterations per second. To provide ternary inputs at this rate from a tape requires equipment that is prohibitively costly. Rather than reduce the machine speed to fit some slower device, a second order interpolation scheme has been introduced. This employs a slow tape reader of the teletype variety that reads second differences into a three integrator chain with the desired output rate. During computation over one interpolation interval, the value in the next interval is read into the initial condition channel from which, at a preassigned signal, it is read into the computation channels. This eliminates the need for stopping computation and is especially useful when a reversal in the independent variable causes a reversal in the direction of the tape.

Provision is also made for reading the second derivatives of variables onto a tape in a form that makes possible their re-entry into computation. This allows functions generated in one problem to be used in another and thus effectively increases the size of the computer. For example, consider the following system:

$$\ddot{Y} = AY + BZX + D\cos\theta$$

$$\ddot{\theta} = C\phi + D\sin^2\phi + Ae^{Z\theta}$$

$$\ln\phi = E\dot{\phi} + F\dot{Y} + \dddot{Z}$$

$$\ddot{W} = B\dot{Z} + G\dot{W} + De^{ZW}.$$

The first three equations may exhuast the capacity of the machine, but by using a tape, $\dddot{Z}$ can be punched and used as an input for the independent solution of the fourth equation. This technique is particularly useful in handling certain types of partials, and in the solution of sets of simultaneous linear equations in which some of the variables may be isolated.

Finally, problems involving step functions can be solved without stopping computation and manually changing the affected integrands. To effect this, a tape is prepared with the values to be held in each of the integrators at the beginning of each step. These numbers are read into the initial condition channel at preassigned values of the independent variable or under the control of one of the variables in the computation, and, at the proper time, entered into the computation channels.

PART II

The mathematical capabilities of the Bendix Digital Differential Analyzer described thus far represent a considerable extension of the usefulness of digital differential analyzers. But such an extension is only justifiable if the basic simplicity of operation generic to former digital differential analyzers is, in the main, retained. One requirement has complicated the problem from the start. Consultation with a wide range of individuals associated with the operation and maintenance of digital computers has indicated that the coding, scaling, and filling of the computer should be entirely in the decimal number system. But decimal addition is costly compared with binary addition and the number of adders required has to be considered. The integration scheme $\Delta Z = Y\Delta X$ requires two adders, as can be seen from Fig. 4.

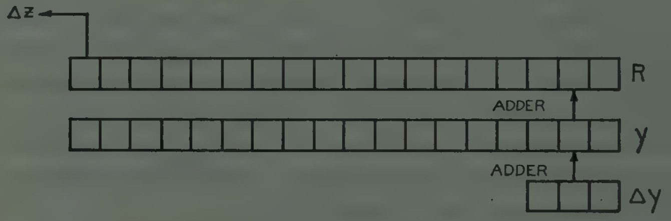


Fig. 4—Information flow to adders with Euler integration and serial adders.

ΔY is collected from the delay line holding the last output of each integrator and added to Y. This sum is simultaneously added to R and the overflows of R constitute ΔZ outputs. In the Bendix Digital Differential Analyzer,[5] however, $\Delta Z = (Y + \frac{1}{2}\Delta Y)\Delta X$ and ΔX may be zero in addition to +1 and −1. This requires the use of three adders, as seen in Fig. 5.

---

[5] Both $Y + \frac{1}{2}\Delta Y$ and $Y + 3/2\Delta Y$ must be generated because of the serial operation of the computer. An integrator with inputs that are the results of the previous iteration cycle must in effect extrapolate, hence the use of $Y + 3/2\Delta Y$. Also multiplication of two variables requires a slight modification that need not be discussed here.

Both Y and Y_D must be generated, in order to provide, respectively, the value of the function at the end of the interval, and its interpolated value that is used in the integration. A fourth adder is needed to add incremental changes into the initial condition channel. The inclusion of four serial decimal adders, however, is not feasible if the size of the machine is to remain moderate. The answer has been found in a rearrangement of information, together with the employment of one single decimal digit adder, operating serially.

Fig. 6 illustrates the scheme. The decimal digits of Y_D, Y, the initial condition of Y, and R are recorded sequentially in four parallel channels of a magnetic drum. The four additions are performed serially and the carries are fed through a delay chain so as to become available at the correct time. Each integrator has six decimal digits; a digit to provide for the one-halves resulting from the $\frac{1}{2}\Delta Y$ operation; a binary digit to the left of the decimal point, which allows the integrand to exceed one; and a sign digit. Multiplication by 2 and 5 is accomplished by varying the position at which overflows are taken from R.

Two devices are employed to limit the size and cost of the input/output equipment so as to make them consonant with that of the computer. The first is the use of a modified electric typewriter rather than a more elaborate machine. Using this, a type-out of previously specified variables can be controlled either by equal increments of the independent variable, or by preassigned values of any other variable, or both. A special channel on the drum holds the information to be typed out so that computation is not normally interrupted. If type-out signals are too closely spaced, the computer will stop to allow an operation in progress to be completed before the next information is accepted. Restarting is automatic. In addition, any one of the variables in the machine can be recorded on punched tape in a form that the input system will process.

The second device is the use of a single system, both for filling the computer and for the insertion of empirical

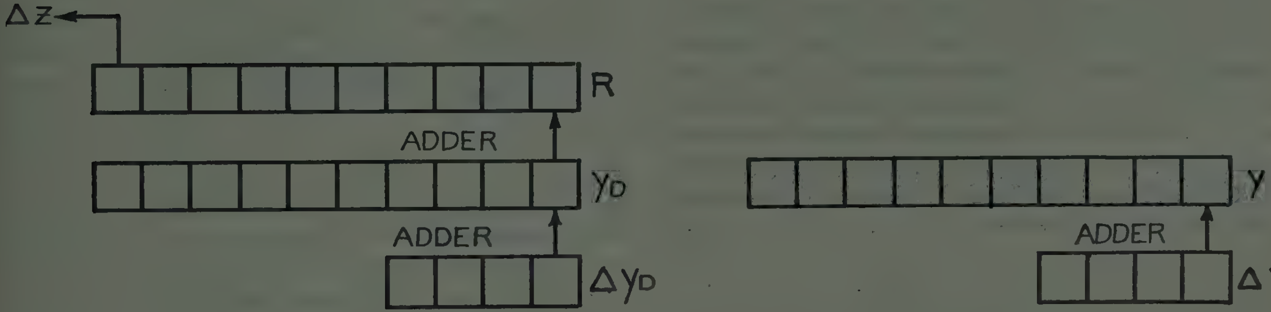


Fig. 5—Information flow to adders with trapezoidal integration and serial adders.

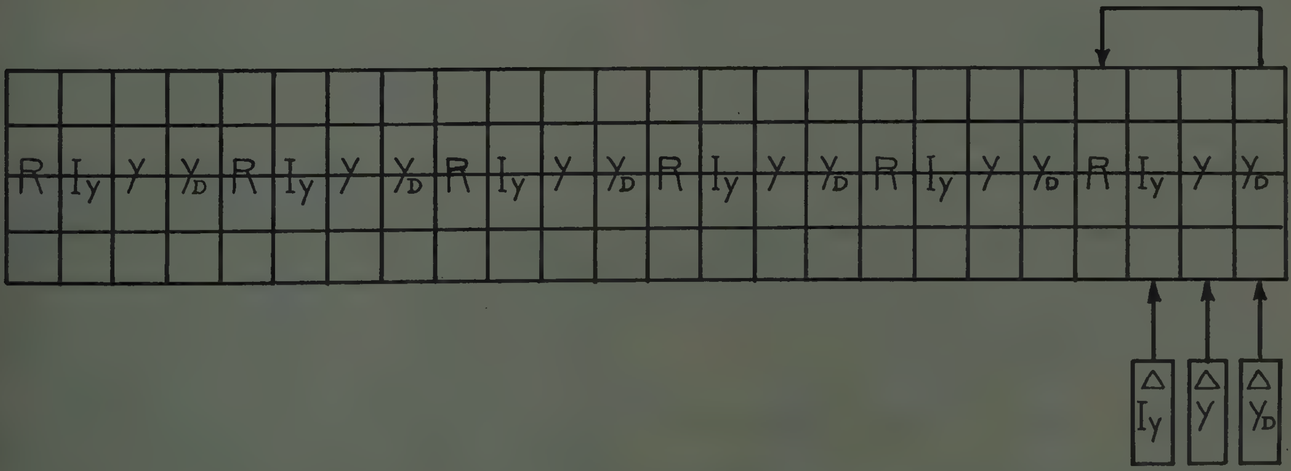

R I_y Y Y_D R I_y Y Y_D R I_y Y Y_D R I_y Y Y_D R I_y Y Y_D R I_y Y Y_D
ΔI_y
ΔY
ΔY_D

Fig. 6—Information flow to adders with trapezoidal integration and parallel adders.

and other functions needed in computation. This consists essentially of a bi-directional tape reader in conjunction with a stepping switch to sequence the operation. The following Table I shows an example of input copy. Less than five seconds is required to fill each integrator. The first two digits identify the integrator (sixty are provided), the next group are the initial conditions of the integrand, and the remaining digits specify control functions and addresses.

TABLE I

16	−196	150201	15	03	13	14	21	47
17	+035306	100001	58	04	16			
18	+14673	010510	59	16	18	36		
19	−00000000	130000						

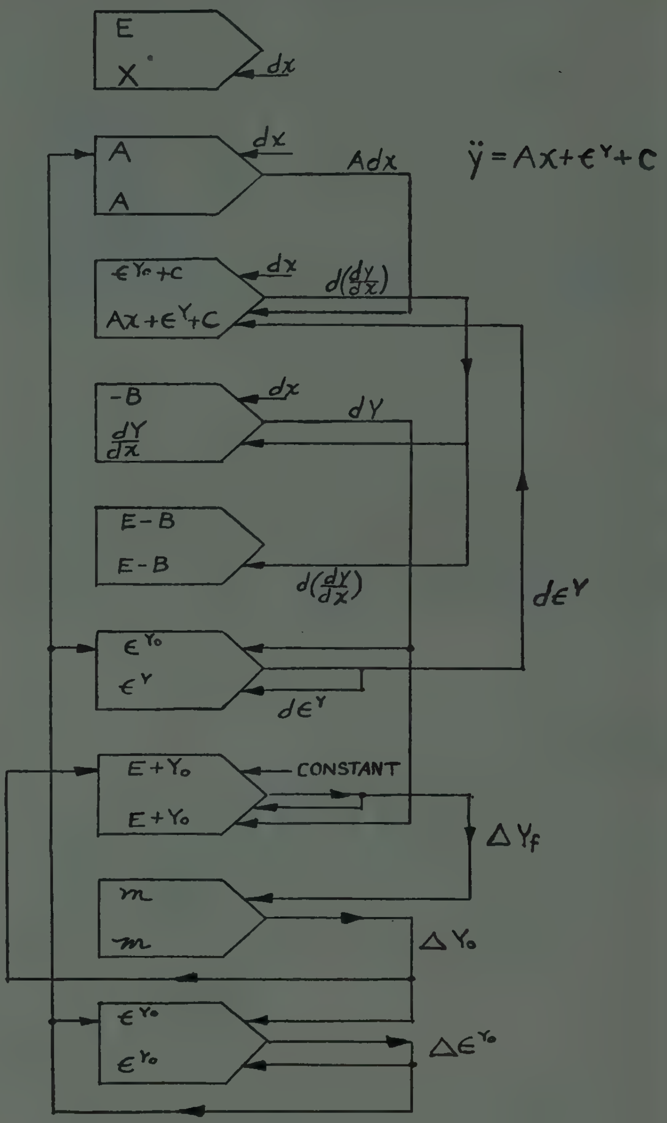
CONCLUSION

The Bendix Digital Differential Analyzer represents both a refinement and an extension of the digital differential principle. By using ternary transfer and a truncation correction, the error of the integration process is reduced. Further, the variable initial condition channel in conjunction with the automatic resetting device permits the treatment of a wider range of problems than has heretofore been possible on a digital differential analyzer. Finally, these improvements have been instituted without an inordinate increase in equipment—the Bendix Digital Differential Analyzer contains less than 125 flip-flop packages.

ACKNOWLEDGMENT

The author wishes to acknowledge the information and advice derived from discussions with R. M. Beck and G. W. Fairchild.

APPENDIX



Appendix—Integrator diagram for the solution of $Y = AX + e^Y + C$ with split boundary conditions.

* * *

Theory of Logical Nets[*]

ARTHUR W. BURKS[†] AND JESSE B. WRIGHT[†]

Summary—The aim of this paper is to place on a more rigorous basis the application of two-valued logic to digital computing circuits. To this end we study the formal properties of various logical nets some of which represent such circuits to a useful degree. A logical net is an array constructed from two primitive elements: a "stroke element," by means of which circuit components performing logical functions may be represented, and a "delay element," used in the representation of memory components.

With each net is associated a set of equations useful in studying the behavior of that net. Various types of nets (well-behaved, deterministic, well-formed) are precisely defined and properties of each type are correlated with properties of the associated sets of equations. The relations between the various types of nets are investigated and some study is made of the kinds of operations performed by each. Finally, the question: "To what class of nets do digital computer circuits correspond?" is discussed.

INTRODUCTION

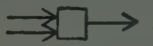
IT HAS BEEN shown by Shannon[1] and McCulloch and Pitts[2] how two-valued[3] symbolic logic may be employed to characterize the behavior of digital computing circuits; e.g., relay circuits,[4] digital electronic computing machines, neuron nets. The purpose of the present paper is to help place the application of two-valued logic to such circuits on a formal and rigorous basis.

We are concerned with two kinds of entities, logical *nets* and digital computing *circuits*. A net N usefully *represents* a circuit C (alternatively, *C physically realizes N*) when the physical behavior of C is mirrored in an idealized but nevertheless useful way by the logical behavior of N. To realize the purpose mentioned in the summary above, we will define various kinds of nets, study their formal properties and discuss the extent to which they can be physically realized.

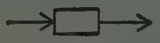
PRIMITIVE ELEMENTS

Since the physical components used in digital computing circuits perform either a logical function or a memory[5] function, or both, the logical analysis of these circuits is facilitated by employing distinct primitive elements for these two functions. Moreover, a single primitive is sufficient for each function, so only two primitive elements are required: the stroke element and the delay element.

A *stroke element* consists of a nucleus with two input *wires* and an *output wire* and is symbolized by:

 .

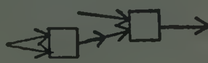
Each net wire has one of two states (0, 1) at each discrete point of time 0, 1, 2, 3, · · · . Moreover, for each time point t the output wire of a stroke element is in the state 0 if and only if both input wires are in the state 1 (Sheffer's stroke function). A delay element consists of a nucleus, an input wire, and an output wire, and is symbolized by:

 .

Each of its wires has one of two states (0, 1) at each discrete point of time, as in the case of the stroke element. The output wire of a delay element is in state 0 at $t=0$, and thereafter it possesses the state possessed by the input wire at the prior point of time.

A *net* is a finite array of elements interconnected so that only the free ends of wires are connected. A *junction* of a net is a point common to one or more ends of wires. If there is no arrowhead at a junction it is an *input junction;* otherwise it is an *output junction.* An output junction all of whose output wires are stroke element output wires is a *stroke output junction;* otherwise it is a *delay output junction.*

We have chosen these primitives because they possess all the following three properties: (1) nets of them are very useful in studying the behavior of digital computing circuits, (2) they are sufficiently simple to permit convenient logical analysis, and (3) small nets of them correspond to the physical components of digital computers. There are, of course, logically equivalent sets of primitives. The stroke element may be replaced by a conjunctive element and a negation element or by a disjunctive element and a negation element. The stroke element may also be replaced by a material implication element, the equivalent of:

 .

Material implication is not by itself a sufficient basis for the propositional calculus, but it and the constant falsehood 0 are;[6] the latter may be realized by:

---

[*] Decimal classification: 621.375.2. Original manuscript received by the Institute, March 9, 1953.

[†] University of Michigan, Ann Arbor, Mich.

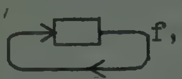
[1] Claude E. Shannon, "A symbolic analysis of relay and switching circuits," *Transactions AIEE*, vol. 57, pp. 713–723; 1938.

[2] Warren L. McCulloch and Walter Pitts, "A logical calculus of the ideas immanent in neuron activity," *Bull. of Math. Biophysics*, vols. 5–6, pp. 115–133; 1943–44. The diagrams used are similar to John von Neumann's modification of the diagrams herein; cf. Douglas R. Hartree, "Calculating Instruments and Machines," University of Illinois Press, pp. 97–111; 1949.

[3] Though the present paper is concerned exclusively with two-valued logic, its results are to a certain extent applicable to circuits containing wires having more than two significant states. This application can be made by allowing several wires of a logical net to correspond to a single wire of a physical circuit. Thus ten of the sixteen different states of four binary net wires can represent ten discrete electrical states of a single circuit wire.

[4] The theory developed here is directed mainly to electronic computer circuits, though it is to a degree applicable to relay circuits.

[5] The British "storage" is better than the American "memory" here, since what are called memory components do not by themselves recall or associate information, but only store it.

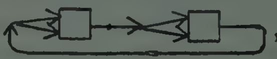


in our system, since $f_t \equiv 0$ for all t.

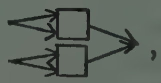
Finally, the delay element may be replaced, in the presence of the stroke element, by a binary counter with an input for counting and an output in the state 0 or 1 according to the state of the counter, or by a flip-flop with a set input, a reset input, and an output. It is not difficult to show that the equivalent of a delay element can be constructed from either of these and the stroke element.

WELL-BEHAVED NETS

For a net N to usefully represent a circuit C there must be a correlation between some of the wires, or sets of wires, of N and some of the wires, or sets of wires, of C such that the states of the designated wires of C are represented by the states of the corresponding wires of N. Now in any well-behaved circuit the state of every wire at every time t is determinate, and, moreover, all wires joined to the same junction are in the same state. Consequently, we are interested only in nets in which (1) the state of every wire is uniquely determined by the defining properties of the primitive elements and (2) the states of all wires attached to a given junction are the same. We shall call such nets well-behaved (w.b.).[7]



is not well-behaved because it does not meet the first requirement, while:



is not well-behaved because of the second requirement. Physical circuits composed of components which in isolation realize stroke elements and which are connected according to these diagrams would, of course, have some definite behavior (the wires of such a circuit might oscillate between two states), but this behavior would be controlled by factors we have deliberately omitted from our idealization and would not mirror the logical behavior of the nets.

In this section we shall define precisely the class of well-behaved nets. We begin by correlating to each net a set of logical equations descriptive of its behavior. Any propositional function of one variable which ranges over the natural numbers and whose values are 0 (false) and 1 (true) will be called, simply, a *function*. We associate with each junction of a net a distinct function *variable*. (These variables will also be used to name the junction and each of its wires.) A variable is an *input, output, stroke output*, or *delay output variable* according as its junction is an input, output, stroke output, or delay output junction. Finally, we *associate* with each net N a *set of equations* $E(N)$ obtained as follows. For each stroke element with input wires g and h and output wire f write the *stroke equation* $f \equiv Sgh$, and for each delay element with input wire g and output wire f write the *delay equation* $f \equiv Dg$. In accord with the interpretation of our primitives, the first equation is equivalent to $f_t \equiv \sim g_t \vee \sim h_t$ and the latter is equivalent to $f_0 \equiv 0$ and $f_{t+1} \equiv g_t$, where t ranges over the natural numbers. It is sometimes convenient to have an infinite sequence $E_0(N), \cdots, E_t(N), \cdots$ of sets of equations derived from $E(N)$ as follows: $E_0(N)$ is the result of replacing each stroke equation $f \equiv Sgh$ of $E(N)$ by $f_0 \equiv Sg_0h_0$ and each delay equation $f \equiv Dg$ of $E(N)$ by $f_0 \equiv 0$, while $E_t(N)$ (for each $t > 0$) is the result of replacing each $f \equiv Sgh$ by $f_t \equiv Sg_th_t$ and each $f \equiv Dg$ by $f_t \equiv g_{t-1}$.

Given any set of (delay and stroke) equations, a net with which this set is associated may be constructed as follows. Make a junction for each variable occurring in the given set of equations and label it with that variable. For each stroke equation $f \equiv Sgh$ place a stroke element from g and h to f and for each delay equation $f \equiv Dg$ place a delay element from g to f. We shall make the correspondence between nets and sets of equations one-one by arbitrarily identifying all sets of equations differing only with respect to the variables used and with respect to the order of the variables following a stroke operator.

The concept of a well-behaved net introduced informally in the first paragraph of this section may be precisely defined in terms of the uniqueness of the solution of the associated set of equations. A net N with input junctions $a^1, \cdots, a^J$ and output junctions $b^1, \cdots, b^K$ is *well-behaved* if and only if for each sequence of functions $a^1, \cdots, a^J$ $(J \geqq 0)$ there exists a unique sequence of functions $b^1, \cdots, b^K$ $(K > 0)$ such that the a^j's and b^k's satisfy $E(N)$. (Here and hereafter when $I = 0$, $f^1, \cdots, f^I$ is to be interpreted as denoting the null sequence.)

Some auxiliary notions, of use later, will now be defined. Let T be any *transformation* or mapping from a sequence of functions $f^1, \cdots, f^J$ $(J \geqq 0)$ to a function g.[8] If g is the same for all sequences, T is a *constant transformation*.[9] A transformation may be regarded as an operation on zero or more denumerable sequences of binary digits (0's and 1's), the values of the corresponding functions for $t = 0, 1, \cdots$. Thus the delay transformation D shifts the sequence it operates on one position to the right and places a zero at its beginning. A *junction* g of a well-behaved net N *realizes a transformation* T of I arguments ($I \geqq 0$) if, and only if, among the input junctions $a^1, \cdots, a^J$ of N there are I of them ($a^{h_1}, \cdots, a^{h_I}$) such that for each sequence of functions $a^1, \cdots, a^J$ the g which satisfies $E(N)$ is equal to $T(a^{h_1}, \cdots, a^{h_I})$. A junction which realizes a constant transformation is called a *constant junction.*

---

[6] Alonzo Church, "Introduction to Mathematical Logic," Princeton University Press, Princeton, N. J., part I, p. 3; 1944.

[7] It is worth noting that a circuit might be well-behaved for a certain combination of inputs and not for others. This suggests defining a concept of well-behavedness for nets which is relative to a certain class of input sequences. However, it is simpler to work with an absolute sense of well-behaved net and this is what will be done here.

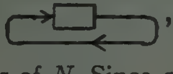
[8] If a transformation T_1 of I arguments $(I \geqq 0)$ and a transformation T_2 of J arguments $(J > I)$ are such that there exists a sequence of numbers $i_1 < i_2 < \cdots < i_I \leqq J$ such that for all $f^1, \cdots, f^J$ $T_1(f^{i_1}, \cdots, f^{i_I}) = T_2(f^1, \cdots, f^J)$, then T_1 and T_2 shall be called the same transformation.

[9] The values of the function g itself are not necessarily the same. There is a constant transformation to the sequence 010101 . . . .

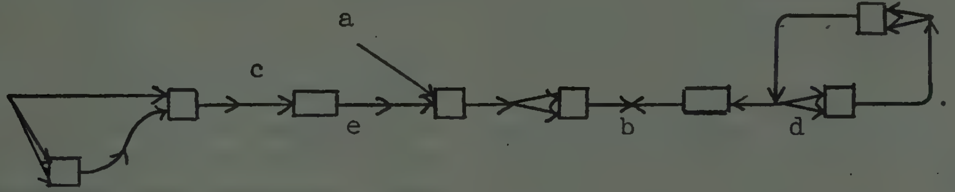
A constant transformation to g is *periodic* if and only if there are natural numbers x and y, $x>0$, such that for every natural number n, $g_{t+nx+y} \equiv g_{t+y}$.

Theorem I: *Every constant transformation realized by a well-behaved net is periodic.*

Proof: Consider a w.b.n. N with junctions $g^1, \cdots, g^K$ where g^1 is a constant junction. Form $\overline{N}$ from it (with each g^K becoming $\bar{g}^K$) by connecting:


,

to all input junctions of N. Since g^1 realizes a constant transformation, $\bar{g}^1$ realizes the same transformation. Since every junction of $\overline{N}$ is a constant junction, there is a single matrix M satisfying $E(\overline{N})$, where the rows of the matrix give the solution for the $\bar{g}^k$'s and the columns $m_0, m_1, \cdots$ give the state of $\overline{N}$ for times $0, 1, \cdots$ respectively. $\overline{N}$ has at most 2^K states, and hence for some x and y, $m_x = m_{x+y}$. Form a new matrix M' such that for $t<x$, $m_t' = m_t$ and for $t \geqq x$, $m_t' = m_{t+y}$. We will prove that $\bar{g}^1$ is periodic by showing that $M = M'$. Any matrix satisfies $E(\overline{N})$ if and only if (1) the first column satisfies $E_0(\overline{N})$ and (2) for every t greater than 0 the $t-1$st and t'th columns satisfy $E_t(\overline{N})$. But if t_1 and t_2 are both greater than zero, $E_{t_1}(\overline{N})$ and $E_{t_2}(\overline{N})$ differ only in their arguments. Hence, condition (2) is equivalent to all pairs of adjacent columns, relabelled for $t=0$ and $t=1$, satisfying $E_1(\overline{N})$. Now any pair m_{t-1}' and m_t' ($t>0$) satisfies $E_1(\overline{N})$ in this way, for all pairs m_{t-1} and m_t satisfied $E_1(\overline{N})$ in this way, and m_{x-1}', m_x' is the same pair as m_{x-1}, m_x (since $m_x = m_{x+y}$). Since $\bar{g}^1$ is periodic, g^1 is also.



A transformation T from $a^1, \cdots, a^J$ to g ($J \geqq 0$) is *primitive recursive* whenever g can be defined by the operations of primitive recursion and substitution from the successor function, the constant functions, the identity functions, and $a^1, \cdots, a^J$.[10]

Theorem II: *There are primitive recursive transformations not realized by well-behaved nets.*

Proof: For example, the constant transformation to, $f_t \equiv 1$ for t a perfect square, $f_t \equiv 0$ otherwise (i.e. 1100100001 $\cdots$) is clearly a primitive recursive transformation, yet it is a constant transformation which is not periodic and hence by *Theorem* I it cannot be realized by any well-behaved net. It is worth noting in this connection that because of its infinite tape a Turing machine[11] is not a net in our sense.

DETERMINISTIC NETS

Not all well-behaved nets are physically realizable. Consider N_1 shown in the diagram below. It is well-behaved, with $c_t \equiv 1$ (for all t) and hence $b_0 \equiv 0$, $b_{t+1} \equiv a_{t+1}$ and finally $d_t \equiv a_{t+1}$. Thus, junction d "anticipates" the future state of input junction a, and the delay element db performs a kind of inverse delay or predictive operation. Obviously no circuit can perform such a predictive function, for there is no circuit component which can mirror the behavior of the delay element db. More generally, delay elements are intended to represent mechanisms in which signals on input wires cause signals to appear, after a suitable delay, on output wires, and we are interested primarily in nets which allow this interpretation. In other words, we are interested in nets in which all delay elements perform a memory or storage, rather than anticipatory or predictive function. We will call nets of this kind deterministic nets.

Consider next N_2, formed from N_1 by joining a and e. N_2 is well-behaved, with $e_0 \equiv 0$, $e_{t+1} \equiv 1$, $b_t \equiv e_t$, and $d_t \equiv 1$. Though the constant transformation to d can, in this case, be realized by a well-formed net which can in turn be physically realized (*Theorem* XIII), it is nevertheless the case that the delay element db performs in N_2 a predictive rather than a memory function, and that hence N_2 is not *deterministic.* That db does behave in this way may be seen by examining $E_0(N_2)$, $E_1(N_2)$, etc. $E_0(N_2)$ does not determine a unique value of d_0; rather, both $d_0 \equiv 1$ and $d_0 \equiv 0$ satisfy $E_0(N_2)$. It is only when $E_1(N_2)$ is considered that the possibility of $d \equiv 0$ is excluded. This analysis leads directly to one definition of deterministic net. Let N have input junctions $a^1, \cdots, a^J$ ($J \geqq 0$) and output junctions $b^1, \cdots, b^K$. First definition: N is *deterministic* if and only if for each sequence $a_0^1, \cdots, a_0^J; \cdots; a_t^1, \cdots, a_t^J$ ($t \geqq 0$) there exists a unique sequence $b_t^1, \cdots, b_t^K$ satisfying the union of $E_0(N), \cdots, E_t(N)$.

---

[10] S. C. Kleene, "Recursive predicates and quantifiers," *Transactions AMS*, vol. 53, p. 42; 1943. (In this definition, function is used in a sense broader than that defined earlier in this section, since it includes any single-valued function of one or more natural numbers whose values are natural numbers.)

[11] A. M. Turing, "On computable numbers, with an application to the Entscheidungs-Problem," *Proc. London Math. Society*, vol. 42, pp. 230–265; 1936–37.

Where a net with input junctions is involved, this definition means roughly that the states of the input junctions for the past and the present determine the states of the output junctions for the present. An alternative conception of determinism is that of the state of the net at the immediate past $(t-1)$ and the state of the input junctions at the present (t) determining the state of the output junctions at the present. Since this conception is also useful, we will give a second definition of determinism and then prove that the two definitions are equivalent. Second definition: N is *deterministic* if and only if both of the following hold: (1) for each $a_0^1, \cdots, a_0^J$ there exists a unique $b_0^1, \cdots, b_0^K$ such that $a_0^1, \cdots, a_0^J; b_0^1, \cdots, b_0^K$ satisfies $E_0(N)$; and (2) if $t>0$ then for each $a_0^1, \cdots, a_0^J; \cdots; a_{t-1}^1, \cdots, a_{t-1}^J$ and $b_0^1, \cdots, b_0^K; \cdots; b_{t-1}^1, \cdots, b_{t-1}^K$ satisfying the union of $E_0(N), \cdots, E_{t-1}(N)$ and each $a_t^1, \cdots, a_t^J$, there exists a unique $b_t^1, \cdots, b_t^K$ such that $a_{t-1}^1, \cdots, a_{t-1}^J; a_t^1, \cdots, a_t^J; b_{t-1}^1, \cdots, b_{t-1}^K; b_t^1, \cdots, b_t^K$ satisfies $E_t(N)$. (If $J=0$ various of the sequences involved are to taken to be the null sequence as before.)

Theorem III: *The two definitions of determinism are equivalent.*

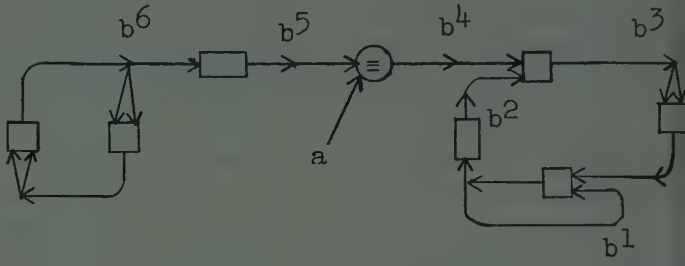
Proof: That the second definition implies the first may be shown by a simple induction. The proof that the first definition implies the second is as follows. Let N be deterministic by the first definition. Then $a_0^1, \cdots, a_0^J; \cdots; a_{t-1}^1, \cdots, a_{t-1}^J$ determines a unique $b_0^1, \cdots, b_0^K; \cdots; b_{t-1}^1, \cdots, b_{t-1}^K$ satisfying the union of $E_0(N), \cdots, E_{t-1}(N)$; and both of these sequences plus $a_t^1, \cdots, a_t^J$ determine a unique $b_t^1, \cdots, b_t^K$ satisfying the union of $E_0(N), \cdots, E_{t-1}(N)$ plus $E_t(N)$. But since $E_t(N)$ involves only the a^i's and b^k's at $t-1$ and t, it follows that the $a_{t-1}^1, \cdots, a_{t-1}^J; a_t^1, \cdots, a_t^J; b_{t-1}^1, \cdots, b_{t-1}^K$ determines a unique $b_t^1, \cdots, b_t^K$ satisfying $E_t(N)$. This last argument makes use of the fact that long-term memory (memory lasting more than one unit of time) in a net is the result of a succession of unit delays. This would not be the case, for example, if we had an additional two-wire primitive element capable of n units of delay, $n>1$; if that were the case the two definitions would not be equivalent.

Theorem IV: *Every deterministic net is well-behaved.*

Proof: This is obvious from the definitions.

We shall next define some concepts which will be of use in characterizing nondeterministic as well as other kinds of w.b.n. Any junction to which two or more output wires are connected is a *multiple junction.* A junction f *directly drives* a junction g if and only if f is the input of a stroke element whose output is g. (The input of a delay element does not directly drive its output.) f *drives* g if and only if there exists a sequence $f^1, f^2, \cdots, f^I$ such that f^1 is f, f^I is g, and f^i directly drives f^{i+1} for $i<I$. The driving relation is transitive: if f drives g and g drives h then f drives h. A *stroke cycle* is a sequence of junctions $f^0, \cdots, f^{I-1}$ such that $f^{i \text{ Mod } I}$ directly drives $f^{(i+1) \text{ Mod } I}$.

It will be observed that N_1 and N_2 contain multiple junctions, stroke cycles and delay elements. Not every nondeterministic w.b.n. contains a multiple junction, however, as the following net proves:



where the circle with the equivalence sign in it represents a net (constructable from stroke elements) realizing $b^4 \equiv (b^5 \equiv a)$. $b_t^1 \equiv 1$ and hence $b_{t+1}^2 \equiv 1$, also $b_t^3 \equiv 1$. These two equations imply that $b_{t+1}^4 \equiv 0$, which in turn implies that $b_{t+1}^5 \equiv \sim a_{t+1}$. Since $b_t^6 \equiv b_{t+1}^5$, it follows that $b_t^6 \equiv \sim a_{t+1}$, and so the net is nondeterministic.

Theorem V: *Every nondeterministic w.b.n. contains a stroke cycle and a delay element.*

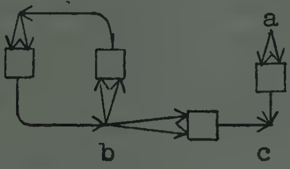
Proof: It will be simpler to give the proof of the first part in the next section (following *Theorem* X). The second half may be stated alternatively: every w.b. *stroke net* (a net constructed exclusively of stroke elements) is deterministic. The proof of it is as follows: Let N be a w.b. stroke net with input junctions $a^1, \cdots, a^J$ and output junctions $b^1, \cdots, b^K$. Then $E(N)$ contains no delay equations, all functions in $E_t(N)$ have t as an argument (never $t-1$), and hence the state of the net at t cannot place any restrictions on the state of the net at $t-1$, and vice versa. Therefore, for each $a_t^1, \cdots, a_t^J$ there is a unique $b_t^1, \cdots, b_t^K$ satisfying $E_t(N)$, since for each $a^1, \cdots, a^J$ there is a unique $b^1, \cdots, b^K$ satisfying $E(N)$. The basic idea of this proof can be employed to prove a stronger result concerning w.b. stroke nets, namely:

Theorem VI: *All transformations realized by w.b. stroke nets are truth-transformations.*

The concept of truth-transformation is defined as follows. Some transformations T (from $a^1, \cdots, a^J$) to g are equivalent to a sequence of mappings $T_0, T_1, \cdots$, each T_t being from a sequence of J truth-values to a single truth-value (0, 1). If all T_t are identical, T is said to be a *truth-transformation.* The result that all transformations realized by w.b. stroke nets are truth-transformations is a justification of an earlier statement that the stroke element performs only a logical function; a w.b. stroke net has no memory, its state at a given time never depends on its state at a prior time and never influences its state at a later time.

WELL-FORMED NETS

Earlier reference was made to physical components which perform a logical rather than memory function and we have represented these in our system by stroke nets. In actual fact, these components function much the same as the components realizing delay elements in that signals on their input wires cause signals to appear, after a certain delay, on output wires. The differences between the temporal lag inherent in a logical component and that in a memory component are that the former is generally smaller than the latter and generally serves no useful purpose. On this account, and in the interest of logical simplicity, our theory includes a temporal delay only in the delay element. As a consequence, however, we should not expect the requirement of determinism to eliminate all nets in which there is a backward passage of causal influence through stroke elements. Thus in the w.b.n.:



, information flows from the output to the inputs of the stroke element *bc*, yet this net is deterministic, with $a_t \equiv \sim c_t \equiv b_t$. Since no component can mirror the logical behavior of the stroke element *bc*, though the transformation it realizes is easily realized physically, not all stroke elements in deterministic nets perform functions which can be duplicated by physical components.

In the present section we will define a class of nets, called well-formed nets (w.f.n.), which excludes the example just discussed. For reasons given in the next section, this is the most useful class of nets for the study of the behavior of digital computing circuits. There are w.f.n. representing, with various degrees of utility and directness, systems of neurons (in which the time intervals are of the order of one millisecond), some systems of electromechanical relays (in which the time intervals are of the order of milliseconds), and many electronic computing machines composed of vacuum tubes, crystal rectifiers, acoustic delay lines, and electrostatic storage tubes. In particular, w.f.n. characterize very closely the behavior of that type of electronic digital computer whose action is governed by a *clock* which is the source of equally-wide equally-spaced standard pulses (with the time interval between pulses being of the order of one microsecond).[12] In fact, our theory is especially directed towards such computers. In this case, a 1 represents the occurrence of a pulse and a 0 the absence of a pulse, or vice versa.

The class of *well-formed* nets is defined recursively as follows, with the understanding that no net is w.f. unless its being so follows from these rules.

(1) (a) Stroke rule: A stroke element is w.f.
    (b) Delay rule: A delay element is w.f.
(2) Assume N_1 and N_2 are disjoint w.f.n. with junctions $f^1, \cdots, f^J$ and $g^1, \cdots, g^K$ respectively.
    (a) Juxtaposition rule: The juxtaposition of N_1 and N_2 is w.f.
    (b) Cascade rule: The result of joining junctions $f^{q_1}, \cdots, f^{q_I}$ of N_1 to distinct input junctions $g^{p_1}, \cdots, g^{p_I}$ of N_2 respectively is w.f.
    (c) Input connection rule: The result of joining input junctions f^p and f^q of N_1 is w.f.
    (d) Cycle rule: If all the wires connected to f^p of N_1 are delay element input wires, then the result of joining any f^q of N_1 to f^p is w.f.

A w.f.n. N may conveniently be studied by means of $E(N)$. $E(N)$ is *unitary* if and only if no variable has more than one left-hand occurrence (to the left of the equivalence sign in a stroke or delay equation) in $E(N)$. $E(N)$ is *regular* if and only if there is an ordering (called a *regular ordering*) of $E(N)$ such that for all f if f has a right-hand stroke equation occurrence in $E(N)$ then there is no left-hand occurrence of f in that or any later equation. The regular ordering of a regular set of equations can be obtained by using the concept of rank. *Ranks* may be assigned to certain of the junctions and corresponding equations of any net as follows. First, assign the rank 0 to all input junctions and all delay output junctions to which no stroke element output wires are connected. Then iterate as long as possible the general step: Assign the rank r to all junctions f such that some junction directly driving f has rank $r-1$ and every junction directly driving f has a rank $\leq r-1$. Finally, to every equation $f \equiv$— which is such that the junction f has a rank, assign the rank of f.

Theorem VII: *N possesses no multiple junctions if and only if $E(N)$ is unitary; and N contains no stroke cycles if and only if $E(N)$ is regular.*

Proof: The first half is obvious. The *only if* part of the second half follows from the fact that the set of equations for a stroke cycle is not regular and hence any set of equations containing them is not regular. That $E(N)$ is regular if N contains no stroke cycles may now be proved as follows. We prove first that since N contains no stroke cycles every junction of N is assigned a rank. Assume some junction f of N has no rank. Then there must be a junction g^1 which directly drives it which has no rank. In turn, there must be a g^2 directly driving g^1 and without rank, ad infinitum. But there are only a finite number of junctions in N, so some variable g^i in the sequence $g^1, g^2, \cdots$ must occur twice in this sequence. Hence N contains a stroke cycle, contrary to our assumption. Since every junction of N is assigned a rank, every equation of $E(N)$ is assigned a rank, and these equations may be arranged in order of ascending rank. We prove finally that this ordering is regular. Consider any equation of the form $f \equiv Sgh$, where g is of rank

---

[12] Douglas R. Hartree, "Calculating Instruments and Machines," University of Illinois Press, pp. 97–111; 1949.

r. Then f is of rank $\geq r+1$; any equation of the form $g\equiv$— is of rank r and hence must precede $f\equiv Sgh$.

Theorem VIII: *N is w.f. if and only if $E(N)$ is both unitary and regular.*

Proof: We prove first that if N is w.f. it contains no multiple junctions and no stroke cycles. A stroke element or delay element by itself (cf. stroke and delay rules) contains no multiple junctions or stroke cycles. Moreover, if N_1 and N_2 contain no multiple junctions or stroke cycles, the result of combining them by any of the four rules of combination will not contain any multiple junctions or stroke cycles. It follows by *Theorem* VII that if N is w.f., $E(N)$ is both unitary and regular. We will prove the converse by giving a stepwise process for constructing N on the basis of S, a regular ordering of $E(N)$. Let S_i be that subsequence of S which consists of the first i equations of S. The net associated with S_1 is w.f. (by rules 1, 2c, and 2d) since $E(N)$ is regular. Assume now that $N_1{}^i$ is formed from S_{i-1} and is w.f. and consider the i'th equation of S. The element associated with it may have two input wires which are paired or not; in the former case use the input connection rule to get $N_2{}^i$; in the latter case take the element itself to be $N_2{}^i$. $N_2{}^i$ may have no input wire connected to a junction of $N_1{}^i$ in N or one or more such; in the former case juxtapose $N_2{}^i$ and $N_1{}^i$; in the latter case cascade $N_1{}^i$ onto $N_2{}^i$. Finally, consider the output f of $N_2{}^i$. Since S_i is regularly ordered and unitary, the only occurrences of f other than the left-hand occurrence in the last equation of S_i are right-hand delay equation occurrences in the equations of S_i. Hence the output of $N_2{}^i$ can be connected into the net, if necessary, by the cycle rule.

Theorem IX: *$E(N)$ is regular if and only if every junction of N has a rank.*

Proof: In *Theorem* VII it was shown that if every junction of N has a rank, then $E(N)$ is regular; and also that if $E(N)$ is regular, then N contains no stroke cycles and that if N contains no stroke cycles then every junction of N has a rank.

Thus the following four properties of N are equivalent: (1) N is w.f., (2) N has no multiple junctions and no stroke cycles, (3) N has no multiple junctions and every junction of N has a rank, and (4) $E(N)$ is both unitary and regular, and any one may be employed as a criterion of a w.f.n. The formation rules are naturally and simply applied when a net is being constructed. Given a complicated net, however, it may be difficult to determine whether or not it can be constructed by the rules. In this case a test procedure based on criterion (3) is useful. Label all junctions of rank 0, stopping if any are multiple junctions (since then N is not w.f.). Then iterate the following step as long as possible: label all junctions of rank r, stopping if any are multiple junctions. If this procedure terminates without a multiple junction being discovered, the N is w.f. if and only if all junctions have been assigned ranks (by *Theorem* IX).

Theorem X: *Every w.f.n. is deterministic, hence well-behaved.*[13]

Proof: The determinism of a w.f.n. follows from the fact that, in the presence of unitariness, regularity is stronger than determinism, allowing not only sequential computation with respect to time but also sequential computation at a given time. For each t the state of a w.f. N may be computed by proceeding through a regular ordering S of $E(N)$ as follows. If the equation at hand is a delay equation $f\equiv Dg$, then for $t=0$, $f_0\equiv 0$ and for $t>0$, $f_t\equiv g_{t-1}$, where g_{t-1} is known from the state of the net at $t-1$. If the equation at hand is a stroke equation $f\equiv Sgh$, then, since S is in regular order, g and h have no left-hand occurrences in that or any later equations of S. Hence g (h) either has a left-hand occurrence in an earlier equation of S, in which case g_t (h_t) is already known from the preceding computation; or g (h) has no left-hand occurrence in any equation, in which case it is an input variable and g_t (h_t) is given. Since $E(N)$ is unitary, this procedure gives a unique value for each f_t. Hence N is deterministic and by *Theorem* IV it is also w.b. An alternative way of looking at the computation is in terms of rank: the states of all junctions of rank 0 may be determined, then those for rank 1, etc.

By a procedure similar to that just used, we will now prove the first half of *Theorem* V, namely, that every nondeterministic w.b.n. contains a stroke cycle. This may be stated alternatively as: Every w.b.n. containing no stroke cycles is deterministic. The proof is as follows. Let N be a w.b.n. with no stroke cycles. By *Theorem* VII $E(N)$ is regular. Hence the behavior of N can be computed in the manner indicated in the last paragraph, and since N is w.b. the result will be unique.

N_1 is a *subnet* of N if and only if N_1 may be formed from N by a succession, perhaps null, of the following operations: (1) separating a wire from a junction; (2) deleting an element.

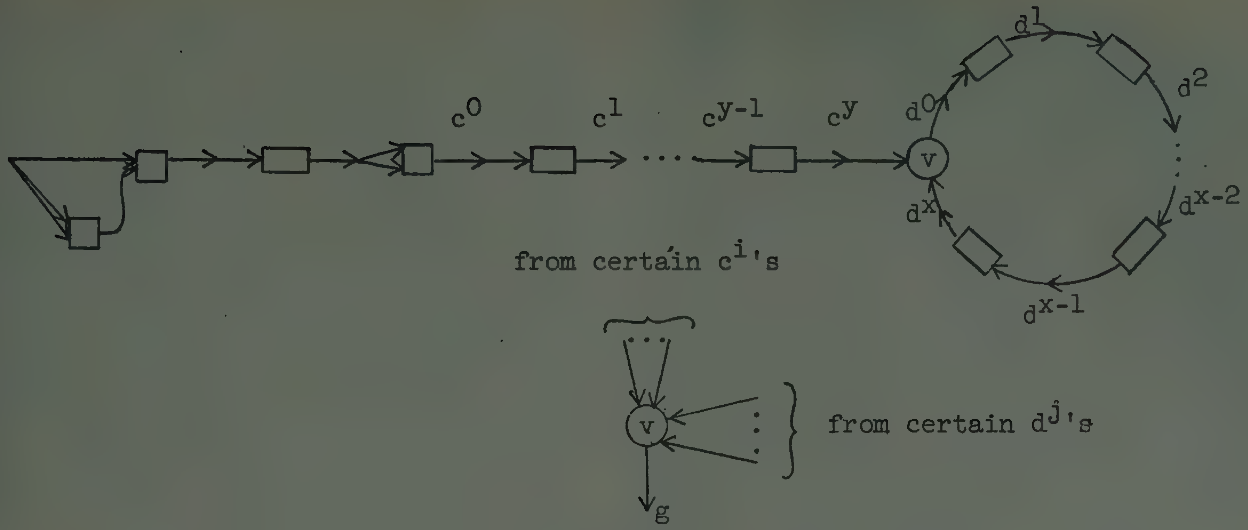
Theorem XI: *N is w.f. if and only if all the subnets of N are w.b.*[14]

Proof: If N is w.f., it contains no multiple junctions or stroke cycles, hence neither do any of its subnets. Therefore each of its subnets is w.f. and hence w.b. Next we show that if N is not w.f. it contains a subnet which is not w.b. There are two cases to consider, according to whether N contains a multiple junction or not. (1) Suppose N contains a multiple junction f such that $f\equiv$— and $f\equiv$... are in $E(N)$. Separate the input wires of the elements associated with each of the equations from their junctions. The result is not w.b. (2) Suppose N contains no multiple junctions but does contain a stroke cycle $f^0, \cdots, f^{I-1}$. We may assume without loss of generality that the associated sequence of equations is $f^{I-1}\equiv Sf^{I-2}g^{I-2}, \cdots, f^0\equiv Sf^{I-1}g^{I-1}$. If any of

---

[13] The example given at the beginning of this section shows that the converse does not hold.

[14] This theorem was suggested by Paul Henle.

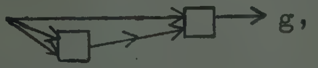


these equations is of the form $p \equiv Sqq$, separate one of the input wires of the corresponding stroke element from its junction, making it a net input. Then if any g^i input wire of an element corresponding to one of these equations is connected to an output junction, separate it from that junction so that it is a net input. The result is not w.b., shown by applying 1's to all input junctions.

Theorem XII: *A transformation is realizable by a w.f. stroke net if and only if it is a truth-transformation.*

Proof: We have already proved (*Theorem* VI) that all transformations realized by w.b. (hence by w.f.) stroke nets are truth-transformations, so it need only be proved that all truth-transformations can be realized by w.f. stroke nets. Since Sheffer's stroke function is a sufficient primitive for defining all truth-functions in the logical sense, it is a sufficient primitive for defining all truth-transformations. The process of definition involves substitution and the use of the same variable in more than one argument place; these are mirrored by the cascade rule and the input connection rule, respectively.

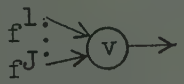
The last half of the theorem shows that in the presence of the formation rules a stroke element is a sufficient primitive for our purposes. It follows from the definition of truth-transformation that there are only two constant truth-transformations: $g_t \equiv 1$ and its negation $h_t \equiv 0$. The former is realized by the w.f.n.:



which is of interest because it is a realization in our system of a *clock*.[15]

Theorem XIII: *A constant transformation is realized by a w.f.n. if and only if it is periodic.*

Proof: The *only if* part of this theorem follows from *Theorems* I and X. The converse is proved by showing how to construct a net realizing any g such that $g_{t+nx+y} \equiv g_{t+y}$. The net which is shown above is a schematic construction of the desired net, where:



represents a J-input disjunction, readily constructed from stroke elements. Note that $c_0{}^0 \equiv 1$, $c_{t+1}{}^0 \equiv 0$, and in general $c_t{}^i \equiv 1$ if and only if $t = i$, while $d_t{}^j \equiv 1$ if and only if $t = j + nx + y$. For a particular constant transformation to g this schema may be converted into a net realizing this transformation as follows. If $g_t \equiv 1$ for any t less than y, connect c^t to one of the inputs of the disjunctive net whose output is g; if $g_t \equiv 1$ for any t as large as y and less than $x+y$, connect d^t to one of the inputs of the disjunctive net whose output is g. g is the desired junction.

Theorem XIV: *Every transformation realized by a w.f.n. is primitive recursive.*

Proof: Too long to be included here, but the essential idea is as follows. Let N be w.f. with input junctions $a^1, \cdots, a^J$ and output junctions $b^1, \cdots, b^K$ in regular order, and let the sequence $b_0{}^1, \cdots, b_0{}^K; b_1{}^1, \cdots, b_1{}^K; \ldots$ be relabeled $e_1, \cdots, e_K; e_{K+1}, \cdots, e_{2K}; \cdots$. Since the behavior of N can be computed in the manner indicated in the proof of *Theorem* X, it is possible to define a mathematical function F (from natural numbers to natural numbers) which is primitive recursive with respect to the a^i's and is such that:

$$F(n) = 2^{e_{n+1}} \cdot \cdots \cdot p_{2K}{}^{e_{n+2K}},$$

where p_k is the k-th prime, in order of magnitude. Each b^k can then be defined primitive recursively in terms of F as follows: $b_t{}^k$ equals the first exponent of $F(tK+k-1)$.

W.F.N. AND DIGITAL COMPUTING CIRCUITS

In this section we will discuss the realization of w.f.n. by digital computing circuits. Consider first the fact that both the delay element and the stroke element (or small nets of it) are realized by physical components in which the input wire states causally determine the output wire state. The output of the physical realization of a delay or stroke element in isolation has the property that its state can be causally determined by the states of its input wires and the formation rules for w.f.n. are such that every output wire of a circuit realizing a w.f.n. has this property. Thus the backward passage of causal influence through stroke elements (cf. the first net discussed in the preceding section) never occurs in a w.f.n. Hence, as far as these considerations are concerned every w.f.n. is physically realizable. There are, however, certain aspects of our idealization of a stroke element which require this conclusion to be restricted. In particular, though the delay of a component realizing a simple stroke net is generally small compared to the basic unit of time of the system, the same does not hold for circuits composed of such components. A practical way of dealing with this point is to construct circuits which perform fairly simple logical transformations and then feed the result into a delay line (as well as into power amplifying and retiming circuits), the temporal lag of the line being such that the total delay is one or a few units of time. This involves placing an upper limit on the allowable rank of a junction and on the number of junctions which drive a given junction. These restrictions could be removed from the net theory by taking as a primitive element a stroke element driving a delay element, but the additional complications would not be worth the gain. In any event, there is an over-all size limitation on the realizability of w.f.n.

---

[15] As mentioned earlier in this section, our theory is especially applicable to circuits synchronized by pulses from a standard clock.

The discussion of deterministic nets showed that if a circuit is represented by a well-behaved net that net is deterministic. Consider now the question: Are there any circuits represented by deterministic nets which could not be adequately represented by w.f. nets? To keep the range of application of the logic of nets as broad as possible, we have left the concept of representation (and its converse, realization) somewhat indefinite. It is sufficiently broad that some so-called *static* circuits and some mixed static and pulse circuits, as well as some pulse (*dynamic*) circuits can under suitable limitations be represented by w.f.n. The answer to the above question depends on the particular interpretation made and hence we will not attempt to give a general answer here; we will, however, make a few relevant comments. Engineers sometimes connect the outputs of two or more physical components together; this is a way of realizing logical disjunction and is better represented in our system by stroke nets realizing logical disjunction than by nets containing multiple junctions. Also, feedback loops are sometimes employed for memory purposes, as in the flip-flop, but these are better represented in our system by means of delay elements rather than by stroke cycles.[16]

On the other hand, consider the following example of a deterministic net not w.f. which may be physically realized in one sense of physical realization. Start with a single physical component realizing $f \equiv (g \cdot \sim h)$ and connects its inputs together so that $f \equiv (g \cdot \sim g) \equiv 0$. Its physical behavior would probably be unaffected by connecting its output back to its input. However, this connection, which introduces a stroke cycle in the corresponding net, is pointless, since it neither increases the number of transformations realized nor decreases the number of elements in the net. Thus this example gives rise to the following two theoretical questions which are worth investigating: (1) Can deterministic nets not w.f. realize transformations not realized by w.f.n.? and (2) Can they realize some transformations more efficiently? The answer with regard to (1) is given by:

Theorem XV: *Every transformation realized by a deterministic net is realized by a w.f.n.*

Proof: Let N be deterministic with input junctions $a^1, \cdots, a^I$, delay output junctions $b^1, \cdots, b^J$, and stroke output junctions $c^1, \cdots, c^K$; and let $\overline{N}$ be the desired w.f.n. whose junctions include the corresponding junctions $\bar{a}^1, \cdots, \bar{a}^I$; $\bar{b}^1, \cdots, \bar{b}^J$; and $\bar{c}^1, \cdots, \bar{c}^K$. We define a sequence of truth-values (0, 1) $x_1, \cdots, x_J$ to be *admissible*, relative to $E(N)$, if and only if it satisfies either of the following two conditions (cf. the second definition of determinism): (1) it consists of all 0's, and (2) there is some $t>0$ and some sequence $a_0^1, \cdots, a_0^I$; $b_0^1, \cdots$; b_0^J; $c_0^1, \cdots$; $c_0^K, \cdots$; $a_t^1, \cdots$; a_t^I; $b_t^1, \cdots$; b_t^J; $c_t^1, \cdots$; c_t^K satisfying the union of $E_0(N), \cdots, E_t(N)$ and such that for each j, $b_t^j = x_j$. Let $E_t^c(N)$ consist of all equations of $E_t(N)$ of the form $c_t^k \equiv$— (i.e., of the form $c_t^k \equiv S \cdots$). Since N is deterministic it then follows that for each $a_t^1, \cdots, a_t^I$ and each admissible $b_t^1, \cdots, b_t^J$ there is a unique $c_t^1, \cdots, c_t^K$ such that $a_t^1, \cdots, a_t^I$; $b_t^1, \cdots, b_t^J$; $c_t^1, \cdots, c_t^K$ satisfies $E_t^c(N)$. Now define for each c_t^k a mapping T_t^k as follows: for each $a_t^1, \cdots, a_t^I$ and each admissible $b_t^1, \cdots, b_t^J$, $T_t^k(a_t^1, \cdots, a_t^I; b_t^1, \cdots, b_t^J)$ is that value of c_t^j which satisfies $\mathrm{E}_t^c(N)$; for each $a_t^1, \cdots, a_t^I$ and each nonadmissible $b_t^1, \cdots, b_t^J$ $T_t^k(a_t^1, \cdots, a_t^I; b_t^1, \cdots, b_t^J) = 0$. Since each $E_t^c(N)$ is of the same form (i.e., a difference in t involves only a difference in the arguments), we may define for every c^k a truth-transformation T^k equivalent to the sequence of mappings $T_0^k, T_1^k, \cdots$. The net $\overline{N}$ may now be constructed as follows. For each b^j pick an equation of $E(N)$ of the form $b^j \equiv Df$ and connect a delay element from $\bar{f}$ to $\bar{b}^j$ in $\overline{N}$. For each $\bar{c}^k$ of $\overline{N}$ construct a w.f. stroke net (*Theorem* XII) from the $\bar{a}^i$'s and $\bar{b}^j$'s realizing T^k. The transformations realized by the $\bar{b}^j$'s and $\bar{c}^k$'s in $\overline{N}$ are the transformations realized by the b^j's and c^k's of N respectively, and since no stroke cycles and no multiple junctions were created in the formation of $\overline{N}$, $\overline{N}$ is w.f.

Consider now question (2). This involves the concept of simplicity. For nets composed of stroke and delay elements a rough measure of simplicity is given by the number of each. Some results concerning this rough measure will now be stated. Let us arbitrarily define N_1

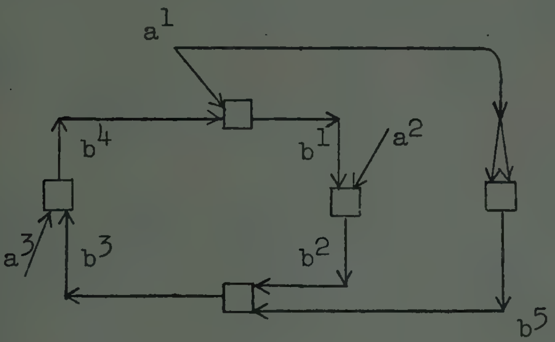
---

[16] By altering the defining equations of a stroke-element we can obtain a "stroke net" which performs a memory function. For example, a net with inputs s (set) and r (reset) and junctions f and g such that $f \equiv (\sim s \cdot \sim g)$ and $g \equiv [\sim f \cdot (\sim r \vee s)]$ is a representation of a flip-flop under the stipulation that if $s_t \equiv r_t \equiv 0$ then (1) if $t = 0$, then $f_t \equiv 0$ and (2) if $t>0$, then $f_t \equiv f_{t-1}$.

to be *as simple as* N_2 whenever N_1 has no more stroke elements and no more delay elements than does N_2. It should be remembered that logically equivalent primitives are not necessarily equivalent where simplicity is involved, so our subsequent theorems on simplicity do not necessarily hold for alternative sets of primitive elements logically equivalent to the set consisting of the stroke and delay elements (Primitive Elements). Question (2) can now be more precisely stated: Given a deterministic net N not w.f., is there a w.f.n. as simple as N which realizes the same transformations as N? The answer is in the negative.

Theorem XVI: *There is a deterministic net N such that no w.f.n. realizing all the transformations realized by N is as simple as N.*

Proof: Let N be:



N contains the stroke cycle b^1, b^2, b^3, b^4 and hence is not w.f., but by *Theorem* IV it is deterministic. It is easily verified that N realizes the distinct transformations:

$$b^1 \equiv (\sim a^1 \vee a^3)$$

$$b^2 \equiv (\sim a^2 \vee a^1 \sim a^3)$$

$$b^3 \equiv a^1 \vee a^2$$

$$b^4 \equiv \sim a^3 \vee \sim a^1 \sim a^2$$

$$b^5 \equiv \sim a^1$$

Consider now a w.f.n. N_1 with at least junctions b^1, b^2, b^3, b^4, and b^5, realizing the corresponding transformations. For each b^k, $1 \leq k \leq 5$ there must be exactly one equation in $E(N_1)$ of the form $b^k \equiv S$—. Replace $b^5 \equiv S$— by $b^5 \equiv Sa^1a^1$; this modification of N_1 does not change the total number of stroke elements in N_1 nor the number of transformations realized by N_1. Let the minimal rank of b^1, b^2, b^3, b^4 of N_1 be R and let b^x be one of the junctions b^1, b^2, b^3, b^4 of N_1 of this minimal rank. None of the transformations b^1, b^2, b^3, b^4 is equivalent to Sfg where f and g are a^1, a^2, a^3, or b^5, and hence b^x cannot be realized from a^1, a^2, a^3, b^5 by less than two stroke elements. Consequently, there is a junction b^6 directly driving b^x which is different from a^1, a^2, a^3, and b^5. b^6 is of rank less than R and hence realizes a transformation different from those realized by b^1, b^2, b^3, and b^4. But N_1 contains five other junctions realizing b^1, b^2, b^3, b^4 and b^5, and so N_1 contains at least six stroke elements. The set got from $E(N)$ by replacing $b^1 \equiv Sa^1b^4$ by $b^1 \equiv Sa^1b^6$ and $b^6 \equiv Sa^3a^3$ is associated with a six-stroke-element w.f.n. that realizes all the transformations realized by N.

Because *Theorem* XVI holds it is of interest to find necessary and sufficient conditions for a deterministic net to have the property that there exists as simple a w.f.n. realizing the same transformations. We have obtained a sufficient condition for this property involving the concept of a properly driven net.

Any junction of a net N is defined to be a *properly driven junction* of N if and only if it belongs to the smallest class satisfying the following rules:

(1) each input junction and each delay output junction is properly driven, and
(2) if g and h are properly driven and $f \equiv Sgh$, then f is properly driven.

A *properly driven net* (p.d.n) is then defined to be a w.b.n. in which every junction is properly driven. The following key theorem concerning p.d.n. is formulated in terms of the following concept. A set of equations $E'(N)$ is a *complete subset* of $E(N)$ if and only if for each output junction f of N $E'(N)$ contains at least one equation of $E(N)$ of the form $f \equiv$—.

Theorem XVII: *If N is p.d. E(N) contains a complete subset E′(N) which is unitary and regular.*

Proof: $E'(N)$ may be constructed as follows. For each delay output junction f of N select one equation of the form $f \equiv D$—. Then iterate this step: Add to $E'(N)$ any equation $f \equiv Sgh$ of $E(N)$ satisfying the conditions: (1) there is no equation of the form $f \equiv$— already in $E'(N)$; (2) both g and h satisfy the condition of having a left-hand occurrence in an equation of $E'(N)$ or being an input variable. It is obvious from its mode of construction that $E'(N)$ is unitary and regular, and it follows from the definition of a properly driven junction (since the above procedure will catch every properly driven junction, hence every junction of the net that) $E'(N)$ is a complete subset of $E(N)$.

Theorem XVIII: *If N is p.d., there is a w.f.n. as simple as N realizing all the transformations realized by N.*

Proof: The required w.f.n. is any subnet of N to which is associated a complete subset of $E(N)$ which is both unitary and regular.

Theorem XIX: *Every p.d.n. is deterministic.*

Theorem XX: *Every stroke cycle of a p.d.n. contains at least one multiple junction* (a characteristic distinguishing p.d.n. from other deterministic nets).

Proof: For if N is p.d. and contains a stroke cycle which has no multiple junctions, any complete subset of $E(N)$ must contain the equations of this stroke cycle and hence cannot be regular.

ACKNOWLEDGMENT

The writing of this paper and the research which it reports were done under the sponsorship of the Burroughs Adding Machine Corporation (completed December 23, 1952).

The authors wish to thank Carl H. Pollmar for many helpful suggestions.

Elements of Boolean Algebra for the Study of Information-Handling Systems*

ROBERT SERRELL†, SENIOR MEMBER, IRE

Summary—Boolean algebra is the algebra of classes or sets of objects. It consists essentially of systematic rules for the use of the fundamental connectives "or," "and," "not." The relevance of Boolean algebra to the information-handling field stems from the fact that, in digital systems, information can be represented only by means of sets of discrete physical states of the machinery involved.

This paper has been prepared principally to present an adequate mathematical basis for the application of Boolean algebra to the study of information-handling systems. An important purpose of this application is the minimization of the physical elements required in information-handling (or computing) circuits. Consequently, some fundamental methods of simplifying Boolean functions are explained in detail. These methods make possible the unconditional minimization of what are called here "elementary" functions, but of these functions only.

Because much of the symbolism and many of the methods in use at the present time are far from uniform, another purpose of this paper has been to put into use an adequate and consistent symbolism, to provide needed fundamental definitions and to derive all theorems and propositions required from the basic postulates.

The treatment is essentially an algebraic one. The methods are those of abstract algebra rather than of mathematical logic. The dualization laws have been systematically used to derive fundamental principles which cannot conveniently be obtained in any other way.

The application of Boolean algebra to the design of computer circuits is illustrated by actual examples.

INTRODUCTION

Boolean Algebra[1]

Almost one hundred years after the publication of "The Laws of Thought" by George Boole, Boolean algebra has become an important tool for the development of information-handling systems of all kinds. By "information-handling system" is meant a collection of methods and devices to perceive, operate upon and transfer information. Most often, the information is handled in digital form—meaning that a language of some sort is used.[2] But an information-handling system usually involves a good deal more than just a digital computer.

Boolean algebra is the algebra of classes or sets of objects. It consists essentially of systematic rules for the use of the three fundamental connectives "or," "and," "not." It may not be immediately evident to the average observer that, for example, the simple statement: "*A* or *B* and *C*" is quite ambiguous. It may mean: "Either *A* or *B* and, with one or both of them, *C*." Or else it may mean: "Either *A*, or *B* and *C* together."[3] A little thought easily shows that the two meanings are not the same. It was to resolve difficulties of this sort that George Boole wrote his "Laws of Thought" in 1854. Since then, the algebraic methods which he originated have been systematized and considerably extended. Boolean algebra is now an indispensable tool for the study of mathematical structure.[4]

The relevance of Boolean algebra to the Information-Handling field stems from the fact that information, in a digital system, is represented by the physical states of various components and circuits. These physical states necessarily form finite, discrete sets. The system can operate upon information only by means of operations on these sets. And because such operations necessarily involve the connectives "or," "and," "not" in some form, the mathematical techniques required (regardless of name or symbolism) are necessarily based on Boolean algebra.

Purpose of This Paper

The main purpose of this paper is to present an adequate mathematical basis for the application of Boolean algebra to the study of information-handling systems involving all internal operations other than pure storage.[5] An important purpose of this application is the minimization of the physical elements required in information-handling (or computing) circuits. Consequently, some fundamental methods of simplifying Boolean functions are explained in detail. These methods make possible the unconditional minimization of what are called the "elementary" functions, but of these functions only.[6] It is not difficult to show that a completely general solution to the minimization problem exists.[7] But, as pointed out in other writings, (12)[8] a completely general minimization technique, that is, one which is applicable to non-"elementary" as well as to "elementary" functions, necessarily involves finite groups of transformation and extends therefore beyond Boolean algebra into Lattice theory. It follows that the

---

* Decimal classification: 621.375.2×510. Original manuscript received by the Institute, June 8, 1953; revised manuscript received July 2, 1953.

† RCA Laboratories Div., David Sarnoff Research Center, Princeton, N. J.

[1] Named in honor of George Boole (1815–1864), English mathematician.

[2] A digital computer is "one which makes explicit use of a language." A language is "a set of symbols, with rules for the combination of these symbols, which may be used to express information, such that the sum of the number of symbols and the number of rules is much smaller than the number of distinct expressible meanings." (IRE definitions; see PROC. I.R.E., "Standards on electronic computers: definitions of terms, 1950," vol. 39, pp. 273; 274; March, 1951.

[3] See A, p. 1368 for a detailed explanation of the ambiguity.

[4] As Boole showed, it also provides the basis of such disciplines as Probability Theory.

[5] These internal operations are all assumed to take place at the same instant.

[6] An elementary Boolean function is one which does not require the use of parentheses within parentheses. See B, p. 1368.

[7] See Theorem XIII, p. 1376.

[8] Numbers in parentheses refer to bibliographical references listed in the Appendix.

development of a completely general minimization technique is not within the scope of the present paper.

Even a casual acquaintance with the literature concerning applications of Boolean algebra will reveal that no uniform symbolism exists at present in this field. Moreover, few texts are available giving a sufficiently complete treatment of the subject to permit direct and effective application of the algebra to all such engineering problems as can be improved by this application.[9] Thus, it is a secondary (but nevertheless important) purpose of this paper to put into use an adequate and consistent symbolism;[10] to give such fundamental definitions as are needed for; an orderly development of the subject; and finally, to derive all theorems required from a clear and complete statement of basic postulates.

It should be noted, however, that the material presented is in no sense complete. The aim has been to provide a solid foundation—one upon which applications work may safely be based—rather than to given an extensive treatment.

A Note on Method

It is useful to note that the treatment given here is essentially an algebraic one. The methods are those of abstract algebra rather than of mathematical logic. Because of the dualization laws,[11] all theorems of Boolean algebra come in pairs. That is to say that with every valid proof a theorem and its "dual" are established. This property (which has long remained inadequately exploited) is systematically put into use in the present paper. As a result, the presentation is clearer and more complete. Further, and this is much more important, fundamental principles are obtained which cannot easily be derived in any other way.

Examples concerning various binary adder circuits are given to illustrate the application of the algebra to the design of the circuits, the verification of their operation and their physical simplification.

DEFINITIONS AND POSTULATES

Boolean algebra concerns relations between classes, or "sets," of objects—any objects. A given set of objects may be designated by a letter A, B, etc. The objects in a set A are called the "elements" of A. These elements may themselves be sets, etc. Sets which contain a finite number of elements are called "finite sets." We shall be concerned with finite sets only. There are two important sets that serve as bounds: The empty set, often designated by 0, and the universal set, often designated by I. The set I is the set of all sets involved in a particular problem. In other words, I is the *class* of all sets under discussion. The number of these sets being finite in our case, I is finite. Two finite sets A and B are equal if, and only if, each distinct element of A is identical to one distinct element of B and vice versa.

Fundamental postulates of Boolean algebra will be given here in a redundant form.[12] It is useful to note that there is no unique set of necessary and sufficient postulates for Boolean algebra. A moderate amount of redundancy will help to clarify the exposition.

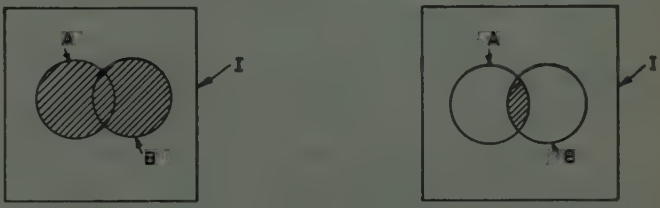
There are three important operations that may be performed on sets: The first is the operation of union, generally designated by $\cup$, as in $(A\cup B)$. The set $(A\cup B)$ is the set of elements that are either in A *or* in B *or* in both. The second is the operation of intersection, generally designated by $\cap$, as in $(A\cap B)$. This is the set of elements that are in both A *and* B. See Fig. 1 below.[13] The third is the operation of complementation, commonly and conveniently designated by a bar over the complemented set as in $\overline{A}$ (read: "not A"). Both operations of union and intersection are

commutative: $(A\cup B=B\cup A;\ A\cap B=B\cap A)$,

associative: $(A\cup[B\cup C]=[A\cup B]\cup C;$
$A\cap[B\cap C]=[A\cap B]\cap C)$, and

distributive: $(A\cup[B\cap C]=[A\cup B]\cap[A\cup C];$
$A\cap[B\cup C]=[A\cap B]\cup[A\cap C])$.

(Note that this complete distributivity does not exist in common algebra. In general, $f+(gh)\neq(f+g)(f+h)$ so that addition is not distributive over multiplication. Multiplication, however, is distributive over addition since $f(g+h)=fg+fh$. Addition and multiplication are both commutative and associative.)



(A U B) (A ∩ B)

Fig. 1—$(A\cup B)$ Definition of union.
$(A\cap B)$ Definition of intersection.

There is an "inclusion relation," as in $(A\supset B)$ which means "A contains B." The set A is then called a "superset" of B while B is a "subset" of A. If $A=B$, then superset and subset are called "improper." To cover both the proper and the improper cases the inclusion relation is written: $A\supseteq B$. This relation is reflexive (for all A, $A\supseteq A$), antisymmetric (if $A\supseteq B$ and $B\supseteq A$, then $A=B$), and transitive (if $A\supseteq B$ and $B\supseteq C$, then $A\supseteq C$).

---

[9] Among the most useful, references (3), (8) and (9) should be mentioned.

[10] For reasons that are explained in detail, this symbolism includes symbols that are well known to mathematicians but not consistently used by engineers.

[11] See p. 1368, footnote.[14]

[12] Essentially as presented in bibliography reference (3).

[13] The diagrams of this and the next two figures are often called "Venn diagrams." They are also called "Euler diagrams."

The following relations obtain:

$$\left.\begin{array}{l} A\cup A=A, \text{ and } A\cap A=A \text{ (Idempotent law)} \\ I\supseteq A\supseteq 0 \text{ (Universal bounds)} \\ 0\cap A=0, \text{ and } I\cap A=A \text{ (Intersection)} \\ 0\cup A=A, \text{ and } I\cup A=I \text{ (Union)} \\ A\cap\overline{A}=0, \text{ and } A\cup\overline{A}=I \text{ (Complementarity)} \\ \overline{(\overline{A})}=A \text{ (Involution)} \end{array}\right\} \text{For all } A.$$

Further:

$$\left.\begin{array}{l} \overline{(A\cup B)}=\overline{A}\cap\overline{B} \\ \overline{(A\cap B)}=\overline{A}\cup\overline{B} \end{array}\right\} \begin{array}{l} \text{For any } A \text{ and } B. \\ \text{(Dualization)}^{14} \end{array}$$

The three conditions: $A\subseteq B$, $A\cup B=B$, and $A\cap B=A$ are mutually equivalent. (Consistency principle)

Any two sets which possess an empty intersection are said to be disjunct.

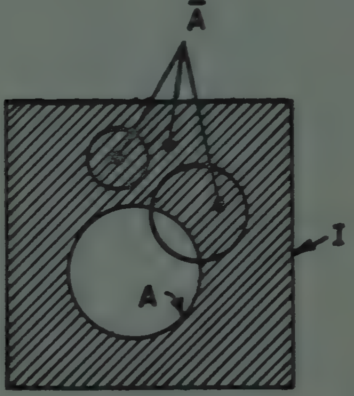


Fig. 2—Complementation. (All the shaded areas in the diagram together constitute $\overline{A}$.)

Note on Symbols

The symbols + and × or · are often used instead of ∪ ("cup") and ∩ ("cap"). There are several good reasons why the special symbols ∪ and ∩ are preferable:

1. There is a great deal of variation in the meaning attached to + and ·. Generally + is taken to mean ∪ ("or") but in some recent writings $+=\cap$. For example in "Synthesis of Electronic Computing and Control Circuits" (8), the symbol + is equivalent to ∪. But in "The Design of Switching Circuits" (9) this same symbol has the meaning "and."
2. The symbols ∪ and ∩ are in general use all over the world and they always have the same meaning.
3. We shall later use both the common symbols +, −, etc. and the logical symbols ∪ and ∩ in related expressions. (We shall perform operations in common arithmetic and operations in Boolean algebra simultaneously.) Distinctions of meaning will necessarily require distinct symbols.[15]

Some Additional Definitions

Any expression involving independent variables $A, B, C, \cdots$ etc., dependent variables $W, X, Y, \cdots$ etc., the symbols ∪, ∩,—and parentheses is called a "Boolean function." An "elementary function" is either a union of intersections or an intersection of unions with only one kind of symbol, ∪ or ∩, within parentheses.

A. An elementary function which is a union of intersections may conveniently be called a "subset function," while an intersection of unions may be called a "superset function."

Examples:

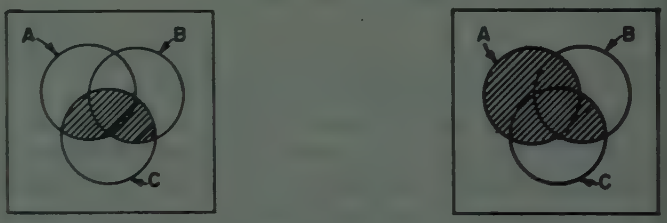
Elementary function: $W=(\overline{A}\cap B)\cup(A\cap\overline{B})$

Non elementary function: $Y=[A\cap(\overline{B}\cup C)]\cup D$

$$\text{Elementary functions}\left\{\begin{array}{l} \left.\begin{array}{l} A\cup(B\cap\overline{C})=X \\ (A\cap B)\cup(C\cap D) \end{array}\right\} \text{Subset functions} \\ \left.\begin{array}{l} A\cap(B\cup C)\cap D=Z \\ A\cap(B\cup C\cup\overline{D}) \end{array}\right\} \text{Superset functions} \end{array}\right.$$

Any expression within any single pair of parentheses is called a *term*.

B. It should be carefully noted that, within any Boolean expression, changes of sign from ∩ to ∪ or vice versa always require the use of parentheses to avoid ambiguity. For example, the expression $A\cup B\cap C$, without parentheses, is ambiguous. We should write instead $(A\cup B)\cap C$, or $A\cup(B\cap C)$, depending upon which is meant. The ambiguity which is due to the lack of parentheses arises from the fact that these two last expressions are not identical, as the diagrams of Fig. 3 clearly show.



$(A\cup B)\cap C$ $A\cup(B\cap C)$

Fig. 3—Ambiguity resulting from lack of parentheses.

---

[14] This pair of equations is often called "De Morgan's Theorem."

[15] The use of ∪ and ∩ instead of + and · does not preclude the possibility of contracting the symbolism as is commonly done with + and · in such expressions as, for example, $DE+G$. We can simply write $DE\cup G$. Further, by adopting the convention that the implied connective is that which does not appear in an expression (and also, that the connective which does appear is accompanied by implied parentheses) we can contract both kinds of expressions. Thus we can write:

$$DE\cup G \quad \text{for} \quad (D\cap E)\cup G$$

or:

$$DE\cap G \quad \text{for} \quad (D\cup E)\cap G, \quad \text{etc.}$$

The parentheses serve to define the range over which each symbol $\cap$ or $\cup$ is effective within a Boolean expression. It is interesting to note that much of the confusion which is sometimes found in purely verbal statements is due to the fact that the range of effectiveness of the words "and," "or" is not clearly apparent.

We shall designate the number of independent variables in any particular problem by n.

A $\begin{smallmatrix}\textit{minterm } m\\ \textit{maxterm } M\end{smallmatrix}$ is any one of the 2^n distinct $\begin{smallmatrix}\text{intersections}\\ \text{unions}\end{smallmatrix}$ of all n variables in which these variables are complemented or not in any one of the 2^n possible ways.[16]

Examples:

The $2^n = 2^2 = 4$ minterms of $n = 2$ are:

$$m_0 = (A \cap \overline{B}) \qquad m_2 = (A \cap \overline{B})$$
$$m_1 = (\overline{A} \cap B) \qquad m_3 = (A \cap B)$$

while the 4 maxterms are:

$$M_0 = (\overline{A} \cup \overline{B}) \qquad M_2 = (A \cup \overline{B})$$
$$M_1 = (\overline{A} \cup B) \qquad M_3 = (A \cup B)$$

The suffix of m or M is the decimal equivalent of the binary number formed by writing "0" for each complemented variable, "1" for each uncomplemented variable, in the order of appearance of these variables. If, for instance, $n = 4$, then $M_9 = (A \cup \overline{B} \cup \overline{C} \cup D)$ since 1001 (binary numeration) is equal to 9 (decimal numeration).

EXPANSION, COMPLEMENTATION AND CANONICAL REPRESENTATIONS OF BOOLEAN FUNCTIONS

Expansion of Elementary Functions

By application of the distribution laws, any subset function of α terms, each containing β appearances of a variable, can be expanded into a superset function of at most β^α terms, each containing at most α appearances of a variable.

Example: $(A \cap B \cap C) \cup (A \cap \overline{B} \cap C)$ can be expanded into $3^2 = 9$ terms:

$$\begin{aligned}(A \cap B \cap C) \cup (A \cap \overline{B} \cap C) \\ = (A \cup A) \cap (B \cup A) \cap (C \cup A) \cap \cdots \\ \cdots \cap (A \cup \overline{B}) \cap (B \cup \overline{B}) \cap (C \cup \overline{B}) \cap \cdots \\ \cdots \cap (A \cup C) \cap (B \cup C) \cap (C \cup C).\end{aligned}$$

Of course the expansion can generally be simplified, after it has been obtained, in many different ways, by application of the postulates listed above. The converse holds. Any superset function of α terms, each containing β appearances of a variable, can be expanded into a subset function of at most β^α terms, each containing at most α appearances of a variable.

Example: $(A \cup \overline{B}) \cap (\overline{C} \cup D)$ expands into a subset function of $2^2 = 4$ terms:

$$\begin{aligned}(A \cup \overline{B}) \cap (\overline{C} \cup D) \\ = (A \cap \overline{C}) \cup (A \cap D) \cup (\overline{B} \cap \overline{C}) \cup (\overline{B} \cap D)\end{aligned}$$

As before, the expansion can generally be simplified. It is evident that this expansion procedure can be generalized to functions the terms of which do not all contain the same number of appearances of a variable.

Undistribution

The undistribution of a Boolean function consists simply in the reversed application of the distributive laws to this function. That is to say that various appearances of a variable (in identically the same form in all appearances) are collected into a single appearance of the variable. This procedure is the converse of that which is described above. Note that in a subset elementary function (union of intersections) the undistributed variable is *intersected* with the remaining terms, and that in a superset function the undistributed variable is *united* with these terms. For example:

$$(A \cap B) \cup (A \cap C) \text{ becomes } A \cap (B \cup C)$$

and:

$$(A \cup B) \cap (A \cup C) \text{ becomes } A \cup (B \cap C), \text{ etc.}$$

Complementation of Functions

From de Morgan's theorem, it is evident that the complement of a function *which does not contain complemented parentheses* can be obtained simply by interchanging $\cup$ and $\cap$ throughout and by reversing all complementations. For example, if:

$$X = (A \cup \overline{B}) \cap (C \cup D \cup E) \cap \overline{F}, \text{ then:}$$
$$\overline{X} = (\overline{A} \cap B) \cup (\overline{C} \cap \overline{D} \cap \overline{E}) \cup F.$$

From this it is evident that if $A = B$, then $\overline{A} = \overline{B}$. But, in view of the consistency principle, note that if we have: $A \supseteq B$. then $\overline{A} \subseteq \overline{B}$.

Canonical Representations of Boolean Functions

Many Boolean functions that are at first glance distinct are actually identical. For example:

$$\begin{aligned}A \cap (\overline{A} \cup B) = (A \cap A) \cup (A \cap B) \\ = 0 \cup (A \cap B) = (A \cap B), \text{ etc., etc.}\end{aligned}$$

It is important to know that two formally distinct canonical (or standard) representations of every Boolean function exist which are practically indispensable for the study of such questions as identity, inclusion, reduction to minimal form, etc. To begin with, we shall show that:

---

[16] The name "minterm" is a contraction of "minimum term." It is justified by the fact that a minterm is a smallest subset of I greater than O. Likewise, a maxterm is a largest subset of I smaller than I. See Theorems VIII and VIIId. Any sentence containing such expressions as $\begin{smallmatrix}\text{“minterm”}\\ \text{“maxterm,”}\end{smallmatrix}$ with words one above the other, is to be read twice; the first time, words in the upper position should be used; the second time, words in the lower position should be read. This saves space and illustrates the dual character of the statements involved.

Theorem I. The union of all 2^n minterms is identically equal to I.

Proof: We can separate the union of 2^n minterms into the union of two unions, each containing $2^{(n-1)}$ minterms. The first of these unions will consist of all $2^{(n-1)}$ minterms containing, say, A, while the second will consist of all $2^{(n-1)}$ minterms containing $\overline{A}$:

$$\{(A\cap\cdot\cdot)\cup(A\cap\cdot\cdot)\cup\cdots\cup(A\cap\cdot\cdot)\}$$
$$\cup\{(A\cap\cdot\cdot)\cup(\overline{A}\cap\cdot\cdot)\cup\cdots\cup(\overline{A}\cap\cdot\cdot\}$$

But, by application of the distribution laws, this may be written:

$$\{A\cap[(\cdot\cdot)\cup(\cdot\cdot)\cup\cdots\cup(\cdot\cdot)]\}$$
$$\cup\{A\cap[(\cdot\cdot)\cup(\cdot\cdot)\cup\cdots\cup(\cdot\cdot)]\}$$

or, since the two sets in square brackets are evidently identical and can be designated by, say Q:

$$(A\cap Q)\cup(\overline{A}\cap Q)=(A\cup A)\cap Q=I\cap Q=Q.$$

We can proceed in this manner to eliminate B by separating Q into two sets, that of the $2^{(n-2)}$ terms containing B and that of the $2^{(n-2)}$ terms containing $\overline{B}$. This yields a set R. This set R can be separated into two sets to eliminate a third variable, etc. Finally, we have only two terms left containing only one variable (the nth) united with its complement. This is identically equal to I. Example, $n=3$:

$$\{(A\cap\overline{B}\cap\overline{C})\cup(A\cap\overline{B}\cap C)\cup(A\cap B\cap\overline{C})\cup\cdot\cdot$$
$$\cdot\cdot\cup(A\cap B\cap C)\}\cup\cdot\cdot$$
$$\cdot\cdot\cup\{(\overline{A}\cap\overline{B}\cap\overline{C})\cup(\overline{A}\cap B\cap C)\cup\cdot\cdot$$
$$\cdot\cdot\cup(A\cap B\cap\overline{C})\cup(A\cap B\cap C)\}$$
$$=\{A\cap[(\overline{B}\cap\overline{C})\cup(\overline{B}\cap C)\cup\cdot\cdot$$
$$\cdot\cdot\cup(B\cap\overline{C})\cup(B\cap C)]\}\cup\cdot\cdot$$
$$\cdot\cdot\cup\{A\cap[(\overline{B}\cap\overline{C})\cup(\overline{B}\cap C)\cup\cdot\cdot$$
$$\cdot\cdot\cup(B\cap\overline{C})\cup(B\cap C)]\}$$
$$=\{(\overline{B}\cap\overline{C})\cup(\overline{B}\cap C)\cup(B\cap\overline{C})\cup(B\cap C)\}\qquad(=\text{“}Q\text{”})$$

. . . .

$$=\{B\cap[(\overline{C})\cup(C)]\}\cup\{\overline{B}\cap[(\overline{C})\cup(C)]\}$$
$$=\{(\overline{C})\cup(C)\}\qquad(=\text{“}R\text{”})$$

. . . .

$$=I.$$

This completes the proof. Since this is an identity, Theorem I is obviously independent of the symbols used to represent the n variables. The theorem holds for the union of the 2^n (minterm) intersections of any n variables, complemented and uncomplemented in every possible way.

By complementing both sides of the equation expressed by Theorem I we obtain immediately:

Theorem Id (dual of Theorem I). The intersection of all 2^n maxterms is identically equal to zero.

Theorem II. The intersection of any two minterms of the same n is equal to zero.

Proof: By definition each minterm involves a complementation (or uncomplementation), for at least one of the n variables $A, B, C\cdots$ which is different from that in every other minterm. It follows that the intersection of any two distinct minterms involves the intersection of some variable with its complement and since this is by definition empty, the intersection of any two minterms is empty.

By complementing both sides of an equation expressing Theorem II such as: $m_\xi\cap m_\eta=0$, where m_ξ and m_η are any two minterms, we obtain:

Theorem IId. The union of any two maxterms of the same n is equal to I.

We shall also need:

Theorem III. The union of the 2^γ intersections obtained by intersecting any given function F with each of the 2^γ minterms that can be formed with γ arbitrary variables, is identically equal to F. (Exponential composition theorem).[17]

Proof: If, for example $\gamma=2$, we need to show that:

$$\{[F\cap(A\cap\overline{B})]\cup[F\cap(A\cap\overline{B})]$$
$$\cup[F\cap(A\cap\overline{B})]\cup[F\cap(A\cap B)]\}=F.$$

By application of the distribution laws, this can be written:

$$F\cap[(A\cap\overline{B})\cup(\overline{A}\cap B)\cup(A\cap\overline{B})\cup(A\cap B)]=F$$

But, by Theorem I, the expression within square brackets is identically equal to I, so that we have: $F\cap I\equiv F$, completing the proof.

The dual of theorem III is:

Theorem IIId. The intersection of the 2^γ unions obtained by uniting any given function F with each of the 2^γ maxterms that can be formed with γ arbitrary variables, is identically equal to F.

The proof is obtained as for Theorem III but by means of Theorem Id (instead of Theorem I), yielding $(F)\cup(0)\equiv F$.

We are now able to prove a basic theorem:

Theorem IV. Every Boolean function can be represented as one and only one union of minterms.

Proof[18] Consider for example the function $F=[\overline{(A\cap\overline{B})}\cup\overline{C}]\cap(\overline{\overline{A}\cup C})$. The complementing bar can always be moved inside the parentheses by de Morgan's theorem. In our example, this brings:

---

[17] The composition is called exponential because the number of terms resulting from it is a power of 2, namely 2^γ.

[18] The proof of this Theorem (and of its dual) is based on one given in bibliographical reference (3).

$F=(\overline{A}\cup B\cup\overline{C})\cap(A\cap\overline{C})$. Secondly, if a "cap," $\cap$, stands outside a parenthesis containing a "cup," $\cup$, the cap can be moved inside the parentheses by applying the distribution law. There results an expression written as a union of terms each of which is an intersection of complemented and uncomplemented variables. We have then:

$$F = (\overline{A} \cap A \cap \overline{C}) \cup (A \cap B \cap \overline{C}) \cup (A \cap \overline{C} \cap \overline{C}).$$

Thirdly, the expression can be shortened by eliminating all but one appearances of each letter within parentheses and by substituting 0 for, say $\overline{A}\cap A$, etc. This yields: $F=(A\cap B\cap\overline{C})\cup(A\cap\overline{C})$. Finally, by exponential composition (See Theorem III above) every term which does not contain all n letters can be replaced by the union of 2^γ terms, where $\gamma<n$ the number of missing letters, each of which contains all n letters. Each of these 2^γ terms contains the letters of the original term as they appear in this term; the other γ letters are complemented and uncomplemented in all possible ways. In our example, the term $(A\cap\overline{C})$ yields $\gamma=1$ and $2^\gamma=2$. We get:

$$(A \cap \overline{C}) = (A \cap B \cap \overline{C}) \cup (A \cap \overline{B} \cap \overline{C})$$

which finally gives:

$$F = (A \cap B \cap \overline{C}) \cup (A \cap \overline{B} \cap \overline{C}) = (m_6) \cup (m_4).$$

We must now show there is only one representation of a given function as a union of minterms. But since, (Theorem II) the minterms are all disjunct, distinct sets (distinct unions) of minterms represent distinct Boolean functions. This completes proof.

Since both union and intersection are distributive, we only need to interchange "$\cup$" and "$\cap$," and the words "union" and "intersection," wherever they appear in the proof of Theorem IV, to prove:

Theorem IVd. Every Boolean function can be represented as one and only one intersection of maxterms.

Using again the example given above (in the proof of Theorem IV maxterms we find successively:

$$F=(\overline{A}\cup B\cup\overline{C})\cap(A\cap\overline{C})=(\overline{A}\cup B\cup\overline{C})\cap(A)\cap(\overline{C})$$

The first term is a maxterm as it stands. By exponential composition, the other two terms, (A) and $(\overline{C})$, become:

$$A = (A \cup \overline{B} \cup \overline{C}) \cap (A \cup B \cup \overline{C}) \cap (A \cup \overline{B} \cup C) \cap \cdot\cdot$$
$$\cdot\cdot \cap (A \cup B \cup C)$$

$$\overline{C} = (\overline{A} \cup \overline{B} \cup \overline{C}) \cap (A \cup \overline{B} \cup \overline{C}) \cap (\overline{A} \cup B \cup \overline{C}) \cap \cdot\cdot$$
$$\cdot\cdot \cap (\overline{A} \cup B \cup \overline{C}).$$

So that, after eliminating repetitions of maxterms, the complete maxterm canonical representation is found to be:

$$F = (\overline{A} \cup B \cup \overline{C}) \cap (A \cup \overline{B} \cup \overline{C}) \cap (A \cup B \cup \overline{C})$$
$$\cap (A \cup \overline{B} \cup C) \cap (A \cup B \cup C) \cap (\overline{A} \cup \overline{B} \cup \overline{C})$$

or after arranging:

$$F = (M_0 \cap M_2 \cap M_4 \cap M_5 \cap M_6 \cap M_7).$$

As we have seen, there are 2^n distinct minterms and every distinct set (union) of them corresponds to a distinct Boolean function. Now since the number of distinct sets that can be formed with 2^n distinct elements if 2^{2^n}[19] it follows that:

Theorem V. There are precisely 2^{2^n} distinct Boolean functions of n variables.

Note that this includes one function identically equal to zero (no minterm) and one function identically equal to I (all 2^n minterms). See Theorem I.[20]

The two (dual) representations of every Boolean function provided by Theorems IV and IVd constitute the unique canonical representations of such a function.

Derivation of One Canonical Representation from the Other

Since, by Theorem I, the union of all 2^n minterms is equal to I, the complement of a given union of minterms, say $F_m=(m_0\cup m_1\cup\cdots\cup m_\epsilon)$ is equal to the union of all other minterms. Thus: $\overline{F}_m=[m_{(\epsilon+1)}\cup m_{(\epsilon+2)}\cup\cdots\cup m_{(2^n-1)}]$. But by applying the dualization law to the expression in square brackets we obtain an intersection of maxterms that is equal to the complement of the complement of F_m, that is, equal to F_m itself. Hence:

Theorem VI. To obtain F_M from F_m:

1. *Write down the union of all minterms not in F_m,* and:
2. *Interchange $\cup$ and $\cap$ throughout and reverse all complementations.*

Example: Let

$$F_m = \{(\overline{A} \cap B \cap \overline{C}) \cup (A \cap \overline{B} \cap C) \cup (A \cap B \cap \overline{C})\}$$
$$= (m_2 \cup m_5 \cup m_6).$$

Then:

$$\overline{F}_m = \{(\overline{A} \cap \overline{B} \cap \overline{C}) \cup (\overline{A} \cap \overline{B} \cap C) \cup \cdot\cdot$$
$$\cdot\cdot \cup (\overline{A} \cap B \cap C) \cup (A \cap \overline{B} \cap \overline{C}) \cup (A \cap B \cap C)\}$$
$$= (m_0 \cup m_1 \cup m_3 \cup m_4 \cup m_7).$$

And:

$$F_M = \{(\overline{A} \cup \overline{B} \cup \overline{C}) \cap (\overline{A} \cup B \cup C) \cap (A \cup \overline{B} \cup \overline{C}) \cup \cdot\cdot$$
$$\cdot\cdot \cap (A \cup B \cup \overline{C}) \cap (A \cup B \cup C)\}$$
$$= (M_0 \cap M_3 \cap M_4 \cap M_6 \cap M_7).$$

Note that, in view of Theorem Id, the order of two steps listed in Theorem VI is immaterial. We may:

1. Interchange $\cup$ and $\cap$ throughout and reverse all complementations. (This gives us $\overline{F}_M$ from F_m.)

---

[19] If δ is any positive integer,

$$\sum_{i=0}^{i=\delta} \frac{\delta!}{(\delta-i)!\,i!} = 2^\delta.$$

[20] It is interesting to note also that: $2^{2^{n+1}}=(2^{2^n})^2$. Even with n comparatively small, 2^{2^n} can be a very large number. As evaluated by A. S. Eddington, the total number N of "protons and electrons in the Universe" is given by: $N=(\frac{3}{2})\times(2^{256})\times 136$. (Fundamental Theory, Cambridge University Press, 1946, p. 283.) Since $(\frac{3}{2})\times 136<2^8$, the number N is smaller than 2^{264}. But with $N=9$, we find $2^{2^9}=2^{512}$. Thus, as pointed out by Dr. John R. Bowman, the number of (formally distinct) functions of 9 variables is larger than the estimated number of "protons and electrons in the universe."

2. Write down the intersection of all maxterms not produced by Step 1). (This gives us $\overline{(\overline{F}_M)} = F_M$.)

The dual of Theorem VI is obvious:

Theorem VId. To obtain F_m from F_M:

1. *Write down the intersection of all maxterms not in F_M, and:*
2. *Interchange $\cup$ and $\cap$ throughout and reverse all complementations.*

It is useful to note that, since the derivation of one canonical form from the other involves the selection of the terms that are *not* in the given form, we have:

Theorem VII. The number of terms in F_m plus the number of terms in the corresponding F_M (or vice versa) add up to a constant equal to 2^n.

Further, since the binary number attached as an identification tag to each $\frac{\text{minterm}}{\text{maxterm}}$ is determined by the complementations of the variables in the term, we may derive either canonical form from the other simply by:

1. Selecting all term numbers other than those appearing in the given function. (This gives us the complement of the function but leaves it in the original form.)
2. Subtracting each number so obtained from (2^n-1). (This gives us the binary tags of the terms constituting the derived form.) As before, the order of these two steps is evidently immaterial.

Procedures of this sort, involving operations on minterm and maxterm binary tags only, constitute a binary arithmetic operational method which, for many problems, greatly simplifies the algebra.[21]

From Theorems VI and VId we obtain the following corollaries:

1. Every maxterm is equal to the union of 2^n-1 minterms.
2. Every minterm is equal to the intersection of 2^n-1 maxterms.

Some Important Theorems on Minterms and Maxterms

From theorems given above we can derive:

Theorem VIII. A minterm is a smallest subset of I other than 0.[22]

Proof: We shall show that no minterm has any non-empty proper subset. Suppose that some minterm, say m_ξ, had a non-empty proper subset. Then, by Theorem IV, this subset should be expressible as a union of minterms. Since this union is not identically empty it should contain at least one minterm, say m_η. In any case, this m_η would be a proper subset of m_ξ and, by the consistency principle, we should have:

$$m_\xi \cap m_\eta = m_\eta.$$

But by Theorem II minterms are all disjunct and every such intersection is empty. It follows that no minterm has any non-empty proper subset.

Theorem VIIId. A maxterm is a largest superset of zero other than I.[23]

Proof: This is the exact dual of Theorem VIII. We shall show that no maxterm has any non-*I* proper superset. Suppose that some maxterm, say M_ξ, had a non-*I* proper superset. Then, by Theorem IVd this superset should be expressible as an intersection of maxterms. Since this intersection is not identically equal to *I* it should contain at least one maxterm, say M_η. In any case, this M_η would be a proper superset of M_ξ and by the consistency principle we should have:

$$M_\xi \cup M_\eta = M_\eta.$$

But by Theorem IId, the union of any two maxterms is equal to *I*. It follows that no maxterm has any proper superset other than *I*.

From the complementation rules it is evident that:

Theorem IX. Every minterm is the complement of some maxterm and vice versa.

Example: With $n=4$, the maxterm: $M_{11}=(A\cup\overline{B}\cup\cdots\cup C\cup D)$ becomes, when complemented, equal to the minterm: $m_4=(\overline{A}\cap B\cap\overline{C}\cap\overline{D})$.

Let F_{Rm} and F_{Sm} be two distinct Boolean functions of the same class (i.e., possessing the same n). Let Rm designate the set of minterms the union of which is equal to F_{Rm} while Sn designates the set of minterms the union of which is equal to F_{Sm}. Then by writing down F_{Rm} and F_{Sm} side by side and removing repetitions of minterms it becomes evident that:

Theorem X: $(F_{Rm})\cup(F_{Sm})=F_{(Rm)\cup(Sm)}$.

Further, in the expansion of $(F_{Rm})\cap(F_{Sm})$ by the distribution laws, all intersections of one minterm of F_{Rm} with a different minterm from F_{Sm} are empty, since, by Theorem II, all distinct minterms are disjunct. So in this expansion, only idempotent intersections (of a minterm with itself) remains non-empty. From this follows:

Theorem XI. $(F_{Rm})\cap(F_{Sm})=F_{(Rm)\cup(Sm)}$.

For example, let $F_{Rm}=m_1\cup m_2\cup m_3$ and $F_{Sm}=m_2\cup m_3\cup m_4$. Then:

$$\begin{aligned} F(_{Rm}) \cap (F_{Sm}) &= (m_1 \cup m_2 \cup m_3) \cap (m_2 \cup m_3 \cup m_4) \\ &= (m_1 \cap m_2) \cup (m_1 \cap m_3) \cup (m_1 \cap m_4) \cup \cdots \\ &\quad \cdots \cup (m_2 \cap m_2) \cup (m_2 \cap m_3) \cup (m_2 \cap m_4) \cup \cdots \\ &\quad \cdots \cup (m_3 \cap m_2) \cup (m_3 \cap m_3) \cup (m_3 \cap m_4) \\ &= m_2 \cup m_3 = F_{(Rm)\cap(Sm)} \end{aligned}$$

The duals of these last two theorems are fairly obvious. Let F_{RM} and F_{SM} be the maxterm representations of the two functions. Then by writing down F_{RM} and F_{SM} side by side and removing repetitions of maxterms we obtain:

---

[21] It is particularly useful in the determination of Boolean functions that are invariant under certain transformations, etc.

[22] Hence the name "minterm."

[23] Hence the name "maxterm."

Theorem Xd. $(F_{RM})\cap(F_{SM})=F_{(RM)\cup(SM)}$.

Finally, in the expansion of $(F_{RM})\cup(F_{SM})$ by the distribution laws, all unions of one maxterm of F_{RM} with a different maxterm from F_{SM} are equal to I, since, by Theorem IId, the union of any two distinct maxterms is equal to I. In this expansion, therefore, only idempotent unions (of a maxterm with itself) remain not equal to I. There follows:

Theorem XId. $(F_{RM})\cup(F_{SM})=F_{(RM)\cap(SM)}$.

If, for example, $F_{RM}=M_5\cap M_6$ and $F_{SM}=M_6\cap M_7$, then:

$$\begin{aligned}(F_{RM})\cup(F_{SM}) &= (M_5\cap M_6)\cup(M_6\cap M_7)\\ &= (M_5\cup M_6)\cap(M_5\cup M_7)\\ &\quad\cap(M_6\cup M_6)\cap(M_6\cup M_7)\\ &= M_6 = F_{(RM)\cap(SM)}\end{aligned}$$

Note that in the statement of each of the two theorems X and XI, only one symbol $\cup$ or $\cap$ is used. This not the case for the dual theorems Xd and XId.

ELEMENTARY COMPONENTS

It is useful to note that, with any fixed n, only a definite number of distinct terms may be formed. With only one appearance of a variable in each term, it is evident that $2n$ distinct terms may be formed. (Each of the n variables may be either complemented or uncomplemented.) With two or more appearances of a variable, terms may be divided into two general kinds. Those that contain cups (unions) and those that contain caps (intersections). Aside from this, the number of distinct terms containing, say, i appearances of a variable is equal to the number of distinct combinations that can be formed with i objects out of a total of n objects, multiplied by 2^i (since each of the i variables in a term may be complemented or not).

It follows that the total number of distinct terms, including both unions and intersections, is:

$$2n+2\sum_{i=2}^{i=n}\binom{n}{i}2^i=2\left[n+\sum_{i=2}^{i=n}\binom{n}{i}2^i\right].$$

Values of this quantity for $n=1, 2, \cdots 6$ are given below:

n	$2\left[n+\sum_{i=2}^{i=n}\binom{n}{i}2^i\right]$
1	2
2	12
3	46
4	152
5	474
6	1444

The distinct terms of both kinds that may be formed with n independent variables, may conveniently be called "elementary components." The following is a table of elementary components for $n=1, 2, 3$:

$n=1$
$\overline{A}, A$
$n=2$
$\overline{A}, A, \overline{B}, B$
$(\overline{A}\cup\overline{B}), (\overline{A}\cup B), (A\cup\overline{B}), (A\cup B)$
$(\overline{A}\cap\overline{B}), (\overline{A}\cap B), (A\cap\overline{B}), (A\cap B)$

$n=3$
$\overline{A}, A, \overline{B}, B, \overline{C}, C$
$(\overline{A}\cup\overline{B}), (\overline{A}\cup B), (A\cup\overline{B}), (A\cup B)$
$(\overline{A}\cup\overline{C}), (\overline{A}\cup C), (A\cup\overline{C}), (A\cup C)$
$(\overline{B}\cup\overline{C}), (\overline{B}\cup C), (B\cup\overline{C}), (B\cup C)$
$(\overline{A}\cap\overline{B}), (\overline{A}\cap B), (A\cap\overline{B}), (A\cap B)$
$(\overline{A}\cap\overline{C}), (\overline{A}\cap C), (A\cap\overline{C}), (A\cap C)$
$(\overline{B}\cap\overline{C}), (\overline{B}\cap C), (B\cap\overline{C}), (B\cap C)$
$(\overline{A}\cup\overline{B}\cup\overline{C}), (\overline{A}\cup\overline{B}\cup C), (\overline{A}\cup B\cup\overline{C}), (\overline{A}\cup B\cup C)$
$(A\cup\overline{B}\cup\overline{C}), (A\cup\overline{B}\cup C), (A\cup B\cup\overline{C}), (A\cup B\cup C)$
$(\overline{A}\cap\overline{B}\cap\overline{C}), (\overline{A}\cap\overline{B}\cap C), (\overline{A}\cap B\cap\overline{C}), (\overline{A}\cap B\cap C)$
$(A\cap\overline{B}\cap\overline{C}), (A\cap\overline{B}\cap C), (A\cap B\cap\overline{C}), (A\cap B\cap C)$

EXPONENTIAL DECOMPOSITION

From the proof of the exponential composition theorems (Theorems III and IIId) it is evident that the converse of these theorems also holds. A $\begin{array}{c}\text{union}\\ \text{intersection}\end{array}$ of 2^γ $\begin{array}{c}\text{intersections}\\ \text{unions}\end{array}$ is equal to a given function F if:

1. F appears (in exactly the same form) in each and every one of the 2^γ terms, and if:
2. The γ arbitrary variables are complemented in all possible ways among the 2^γ terms.

For example, the union of $2^2=4$ intersections:

$$(\overline{A}\cap B\cap\overline{C})\cup(\overline{A}\cap B\cap C)\cup(A\cap B\cap\overline{C})\cup(A\cap B\cap C)$$

is equal to $F=B$, since B appears (in the same form) in every term and since the two arbitrary variables, A and C, appear with all possible complementations. Similarly, the intersection: $(C\cup D\cup\overline{X})\cap(C\cup D\cup X)$ is equal to $F=(C\cup D)$.

Note that if the exponential decomposition theorems are applied either to a union of minterms or to an intersection of maxterms, the two conditions listed above may be combined into one. F is then an elementary component containing $(n-\gamma)$ variables. If F appears (in the same form) in 2^γ distinct $\begin{array}{c}\text{minterms}\\ \text{maxterms}\end{array}$ then the γ arbitrary variables must necessarily be complemented in all possible ways. Otherwise the 2^γ

$\begin{matrix}\text{minterms}\\ \text{maxterms}\end{matrix}$ could not be distinct. In such a case, it is sufficient therefore that 2^γ $\begin{matrix}\text{minterms}\\ \text{maxterms}\end{matrix}$ be found each containing F to insure that the $\begin{matrix}\text{union}\\ \text{intersection}\end{matrix}$ of these 2^γ $\begin{matrix}\text{minterms}\\ \text{maxterms}\end{matrix}$ be equal to F.

DECOMPOSITION OF CANONICAL FORMS INTO ELEMENTARY COMPONENTS

Every canonical form can, in general, be reduced by means of the exponential decomposition process into a simpler elementary function involving only elementary components of the same kind. (By "same kind" is meant that if the canonical form is a $\begin{matrix}\text{union}\\ \text{intersection}\end{matrix}$ of $\begin{matrix}\text{minterms}\\ \text{maxterms}\end{matrix}$ the elementary components are $\begin{matrix}\text{intersections}\\ \text{unions}\end{matrix}$).

A $\begin{matrix}\text{union}\\ \text{intersection}\end{matrix}$ of $\begin{matrix}\text{minterms}\\ \text{maxterms}\end{matrix}$ becomes a $\begin{matrix}\text{subset}\\ \text{superset}\end{matrix}$ function containing at most as many terms as the original and in which each term (an elementary component) contains at most n appearances of a variable. The decomposition process is facilitated by reference to a table of elementary components of the proper value of n. Consider for example the minterm function :

$$F = (\overline{A} \cap B \cap C) \cup (A \cap B \cap \overline{C}) \cup (A \cap B \cap C)$$
$$= m_3 \cup m_6 \cup m_7 \text{ in which } n = 3.$$

By referring to the table on p. 1373, we see that, since F is a union of only three minterms, none of A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$ is contained in (or is a subset of) F. But proceeding further, we find that:

$$m_3 \cup m_7 = (B \cap C)$$
$$m_6 \cup m_7 = (A \cap B)$$

so that:

$$(B \cap C) \cup (A \cap B) = (m_3 \cup m_7) \cup (m_6 \cup m_7)$$
$$= m_3 \cup m_6 \cup m_7 = F.$$

Here, a union of three minterms, each containing three appearances of a variable, has become a union of two elementary components each containing only two appearances of a variable. Note that, in the union of the two elementary components, one minterm, m_7, is represented twice.[24] m^7 is a subset of both $(B \cap C)$ and of $(A \cap B)$.

For a second example, consider the maxterm function:

$$F = (A \cup \overline{B}) \cap (A \cup \overline{B}) \cap (A \cup B) = M_0 \cap M_2 \cap M_3,$$

in which $n=2$. We find immediately that:

$$M_0 \cap M_2 = \overline{B}$$

while:

$$M_2 \cap M_3 \cup A$$

so that · ·

$$(\overline{B}) \cap (A) = (M_0 \cap M_2) \cap (M_2 \cap M_3)$$
$$= M_0 \cap M_2 \cap M_3 = F.$$

As in the first example, one minterm is represented twice.

SIMPLEST ELEMENTARY FUNCTION REPRESENTATION

It has been shown in the preceding pages how canonical forms can be decomposed into elementary components of the same kind. In general, as a consequence, in part, of Theorem VII,[25] one of the two canonical forms leads to a simpler representation than the other. To find the simplest elementary function representation of a given function F it is therefore necessary to express F both as a union of minterms and as an intersection of maxterms. Each of the two expressions should then be decomposed into all of its elementary components. After this is done, the given function can be built up by means of either subset elementary components or superset elementary components in such a way as to minimize whatever criterion of complexity is used. Since the number of elementary components of either kind is finite, the number of different ways in which the given function can be synthesized is finite, so that at least one simplest (elementary function) representation surely exists. (There may be more than one.) Of course this procedure may be used to synthesize the representation of several dependent variables simultaneously, leading to a multiple representation which is a simplest (elementary function) representation for all of them together.

Examples:

$$n = 3.$$

I. The minterm function:

$$(\overline{A} \cap \overline{B} \cap \overline{C}) \cup (A \cap B \cap \overline{C}) \cup (A \cap \overline{B} \cap \overline{C}) \cup \cdot\cdot$$
$$\cdot\cdot \cup (A \cap \overline{B} \cap C) \cup (A \cap B \cap C)$$
$$= m_0 \cup m_2 \cup m_4 \cup m_5 \cup m_7$$

can be reduced by exponential decomposition to a simpler elementary function:

$$(m_0 \cup m_2) \cup (m_4 \cup m_5) \cup (m_5 \cup m_7)$$
$$= (\overline{A} \cap \overline{C}) \cup (A \cap \overline{B}) \cup (A \cap C)$$

or

$$(m_0 \cup m_2) \cup (m_0 \cup m_4) \cup (m_5 \cup m_7)$$
$$= (\overline{A} \cap \overline{C}) \cup (\overline{B} \cap \overline{C}) \cup (A \cap C).$$

---

[24] Of course, by the idempotent law, $m_7 \cup m_7 = m_7$.

[25] Stating, in effect, that if the minterm representation of some given function is complicated, the corresponding maxterm representation is simple, and vice versa.

A union of five minterms, each containing three appearances of a variable, has been reduced to a union of three elementary components (subset function) each containing only two appearances of a variable.

The corresponding maxterm function:

$$(A \cup B \cup \overline{C}) \cap (A \cup \overline{B} \cup \overline{C}) \cap (\overline{A} \cup \overline{B} \cup C) = M_6 \cap M_4 \cap M_1$$

can be reduced to a simpler elementary function by exponential decomposition into elementary components:

$$M_1 \cap (M_4 \cap M_6) = (\overline{A} \cup \overline{B} \cup C) \cap (A \cup \overline{C})$$

An intersection of three maxterms, each having three appearances of a variable has been reduced to an intersection of two elementary components (superset function), one containing three appearances of a variable, and the other only two appearances of a variable.

Let us now define the number of logical elements required for the mechanization of some given elementary function. It is assumed that no logical elements are required for the complementation of independent variables taken singly. That is to say that no logical elements are required for functions of a single variable. For all others, the number of logical elements needed is given as the sum of:

1. The total number of appearances of a letter within every term containing more than one letter, plus:
2. The number of terms.[26]

Then by examining both reduced representations, we find that the reduced maxterm function is simpler than the reduced minterm function in that the superset function requires only seven logical elements, while the subset function requires nine logical elements.

II. The minterm function:

$$(\overline{A} \cap \overline{B} \cap \overline{C}) \cup (\overline{A} \cap B \cap C) \cup (A \cap \overline{B} \cap C) = m_0 \cup m_3 \cup m_5$$

cannot be reduced by means of elementary components to a simpler elementary function.

The corresponding maxterm function:

$$(A \cup B \cup \overline{C}) \cap (A \cup \overline{B} \cup C) \cap (\overline{A} \cup B \cup C) \cap \cdots$$
$$\cdots \cap (\overline{A} \cup \overline{B} \cup C) \cap (\overline{A} \cup \overline{B} \cup \overline{C}) = M_6 \cap M_5 \cap M_3 \cap M_1 \cap M_0$$

can be reduced by means of elementary components to a simpler form:

$$(\overline{A} \cup C) \cap (\overline{B} \cup C) \cap (A \cup \overline{B}) \cap (A \cup B \cup \overline{C}) \cap \cdots = (M_1 \cap M_3) \cap (M_1 \cap M_5) \cap (M_0 \cap M_1) \cap (M_6).$$

An intersection of five maxterms, each containing three appearances of a variable has been reduced to an intersection of four elementary components (superset function), three containing only two appearances of a variable, and one, three appearances of a variable.

We now find by examination that the minterm function requires only 12 logical elements, while the reduced maxterm function requires 13.

If, in this simplifying process, the simpler elementary components are considered first (for extraction from the canonical representations of the given function), it is sufficient to consider each component only once. It should be evident that the simpler the elementary component that can be extracted, the smaller the number of $\genfrac{}{}{0pt}{}{\text{minterms}}{\text{maxterms}}$ that remain after extraction. Thus, by proceeding from simpler elementary components to more complex, direct simplification results.

For example if:

$$F = (A \cap B \cap C) \cup (A \cap \overline{B} \cap \overline{C}) \cup (A \cap \overline{B} \cap C) \cup (A \cap B \cap \overline{C})$$

we may first extract the elementary components $(A \cap B)$ and $(A \cap \overline{B})$ from F to find:

$$F = (A \cap B) \cup (A \cap \overline{B})$$

which can of course be simplified further to $F = (A)$. This result, however, can be obtained directly by extracting the simpler elementary component (A) from the given function, yielding $F = (A)$ in one step.

An example concerning the simultaneous reduction of more than one function is given on p. 1376.

APPLICATION

Correspondence tables and fundamental minterm representation. A simple heuristic proof will be given here of the fact that:

Theorem XII: Every table specifying the "output" corresponding to each of the 2^n "input" conditions determined by n independent variables may be completely described by a union of at most 2^n minterms in the n independent variables.

Proof: Let the correspondence table be one such as that shown below:

Input Conditions			Output Conditions
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

---

[26] This does not take into account the possible complementation of some terms. However, insofar as elementary functions are concerned, it is easy to see that the number of logical elements required (as defined here) is smaller if the complementations of terms are removed by the complementation rule.

It should be noted that the definition is not a necessary one. It is only convenient to use. A physical realization of any given elementary function involving one non-linear element (relay contact, rectifier, etc.) for each logical element indicated by this definition is always possible. It is important to know, however, that the converse does not hold in general. For some cases, "bridge circuits" exist in which the number of physical non-linear elements required is smaller than that of logical elements given by the definition. See reference (9).

Further, let A be the set of instances in which input A is "1" (energized) and similarly for B and C. Then $\overline{A}$ is the set of instances in which input A is "0," etc. Likewise, X is the set of instances in which the output is "1" (energized) and $\overline{X}$ is the set of instances in which it is "0."

We can always describe each single element of X as one intersection of the sets A, B, C, etc., or of the complements of some of these sets. Consider the table above: Corresponding to the first instance in which the input X is "1" the input A is "0," the input B is "0" and the input C is "1." That is to say that the first element of X corresponds to input conditions $\overline{A}$ and, at the same time, $\overline{B}$, and, at the same time, C. In the usual symbols therefore:

$$\text{1st element of } X = \overline{A} \cap \overline{B} \cap C$$

Similarly, the other two elements of X are given by:

2d element of $X = A \cap B \cap \overline{C}$. (Input A is "1," input B is "1," input C is "0").

3d element of $X = A \cap B \cap C$. (Input A is "1," input B is "1," input C is "1").

Since this takes all elements of X (as given by the table) into account, we have:

$$X = (A \cap \overline{B} \cap C) \cup (A \cap B \cap \overline{C}) \cup (A \cap B \cap C)$$

This expression is simply a union of minterms, each of which represents one distinct element of X.

It is now necessary to show that:

$$\overline{X} = \overline{\{(\overline{A} \cap \overline{B} \cap C) \cup (A \cap B \cap \overline{C}) \cup (A \cap B \cap C)\}}$$

But from Theorem I we find immediately:

$$\overline{\{(\overline{A} \cap \overline{B} \cap C) \cup (A \cap B \cap \overline{C}) \cup (A \cap B \cap C)\}}$$
$$= \{(\overline{A} \cap \overline{B} \cap \overline{C}) \cup (\overline{A} \cap B \cap \overline{C}) \cup (\overline{A} \cap B \cap C) \cup \cdots$$
$$\cdots \cup (A \cap \overline{B} \cap \overline{C}) \cup (A \cap \overline{B} \cap C)\}$$

while the expression:

$$\overline{X} = \{(\overline{A} \cap \overline{B} \cap \overline{C}) \cup (\overline{A} \cap B \cap \overline{C}) \cup \cdots$$
$$\cdots \cup (A \cap B \cap C) \cup (A \cap \overline{B} \cap \overline{C}) \cup (A \cap \overline{B} \cap C)\}$$

may be drived directly from the correspondence table given above, thus completing the proof.[27]

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	0	0

Of course more than one dependent variable may be defined simultaneously from one and the same correspondence table. If, for example, the dependent variables Y and Z are added to the table given above, we find immediately:

$$Y = (\overline{A} \cap B \cap \overline{C})$$
$$Z = (\overline{A} \cap \overline{B} \cap C) \cup (\overline{A} \cap B \cap C), \quad \text{etc.}$$

It is evident that the functions X, Y, Z, etc. may be operated upon as if they were any Boolean functions given a priori. In particular, the maxterm canonical representations may be derived from the minterm representations as explained earlier.

Upper limit of the number of logical elements required. It is easy to show that:

Theorem XIII: The number of logical elements required for mechanization of a function expressing a dependent variable X in terms of n independent variables A, B, C, etc. is never larger than $2^{(n-1)}(n+1)$.

Proof: Theorem XII above shows that not more than 2^n minterms need to be used. But Theorem VII states that if this number is greater than 2^{n-1}, then conversion to the equivalent maxterm representation will result in a function possessing less than 2^{n-1} maxterms. It follows that the total number of minterms or maxterms required need never be larger than 2^{n-1}. To complete the proof it is sufficient to note that each term contains all n variables and that there are not more than 2^{n-1} pairs of parentheses. This yields:

$$(2^{n-1})(n) + 2^{n-1} = (2^{n-1})(n+1).$$

It is evident that the number of logical elements actually required is often very much less than $2^{(n-1)}(n+1)$. This value represents an upper limit which is sometimes reached but never exceeded. The existence of this limit proves that a solution to the general minimization problem exists.

Examples—The Binary Adder. Examples involving various forms of the binary adder will now be given to provide a brief illustration of the application of Boolean algebra to the study of computing circuits. The binary adder has been chosen because it is a well-known device which is widely used in many forms and because its features are reasonably typical. The first example concerns the design of an adder circuit starting from a bare statement of the problem in correspondence-table form. The second example concerns the verification of the performance and suitability of a given adder circuit. Finally, the third example concerns the simplifications of adder circuits that are possible with logical elements of a given type.

---

[27] It is interesting to note that the form in which Boolean functions are most readily derivable from a correspondence table is a minterm rather than a maxterm representation. This is apparently due to the fact that functions in minterm form can be directly combined: The terms of the union of two functions are given by the union of their terms; the terms of the intersection of two functions are given by the intersection of their terms. Functions in maxterm form do not follow such simple rules. See Theorems X and XI and their duals. The psychophysiological implications of these facts appear to be worth noting.

I. The one-column binary adder is a device possessing three inputs, an augend A_1, an addend A_2, and a carry C_i (from the preceding column). The device also possesses two outputs, the sum S and a carry C_0 (to the succeeding column) as illustrated in Fig. 4.

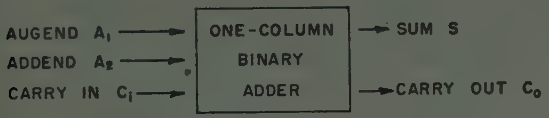


Fig. 4—Inputs and outputs of binary adder.

The operation of the adder may be described by means of the correspondence table given below:

A_1	A_2	C_i	S	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The functions S and C_0 may be represented as shown in the diagrams of Fig. 5:

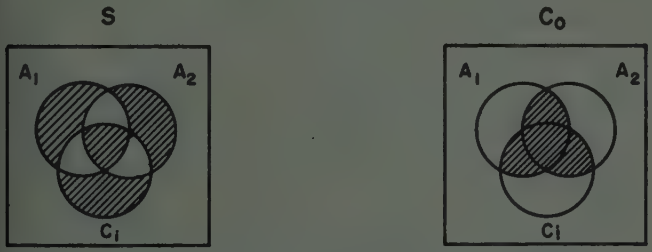


Fig. 5—Diagrammatic representations of S and of C_0.

By examination of the table, we obtain directly:

$$S = \{(\overline{A}_1 \cap \overline{A}_2 \cap C_i) \cup (\overline{A}_1 \cap A_2 \cap \overline{C}_i) \cup \cdots$$
$$\cdots \cup (A_1 \cap \overline{A}_2 \cap \overline{C}_i) \cup (A_1 \cap A_2 \cap C_i)\}$$
$$C_0 = \{(\overline{A}_1 \cap A_2 \cap C_i) \cup (A_1 \cap \overline{A}_2 \cap C_i) \cup \cdots$$
$$\cdots \cup (A_1 \cap A_2 \cap \overline{C}_i) \cup (A_1 \cap A_2 \cap C_i)\}$$

The elementary components of S are precisely those given in the canonical subset function above. However, the application of the exponential decomposition process to the canonical subset expression for C_0 yields:

$$C_0 = \{(A_1 \cap A_2) \cup (A_1 \cap C_i) \cup (A_2 \cap C_i)\}$$

This leads directly to a two-stage (elementary function) physical realization of the one-digit binary adder as shown in Fig. 6.

It can easily be seen from the figure that this realization requires:

$$[(4 \times 3) + 4] + [(3 \times 2) + 3] = 25$$

logical elements. This is the total number of inputs to "intersectors" $\boxed{\cap}$ and to "unitors" $\boxed{\cup}$.

The third kind of logical device (not needed in the circuit of Fig. 6) can be called a "complementor" and can be represented schematically by $-\boxed{-}-$. Physically, an intersector is any device possessing two or more distinct inputs and one output such that the output is energized when and only when all inputs are energized.

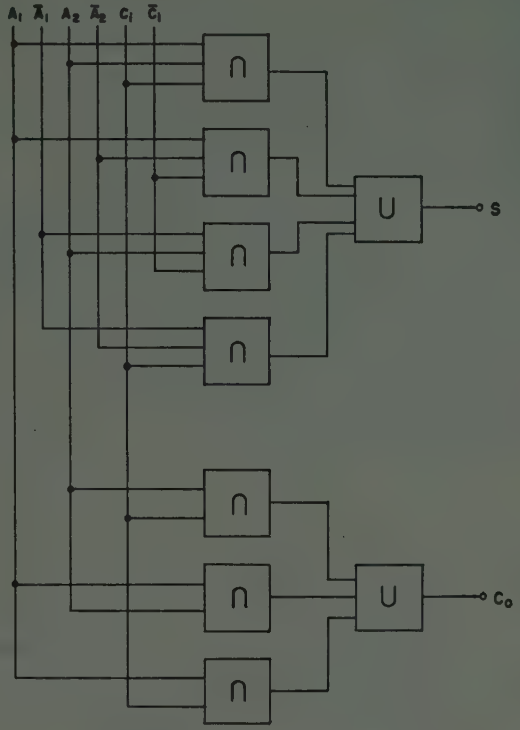


Fig. 6—Elementary function synthesis of the one-column binary adder.

It may be made of a number of "make" relay contacts in series, etc. Similarly, a unitor is any device possessing two or more distinct inputs and one output such that the output is energized when and only when one or more of the inputs are energized. It may be made of a number of "make" relay contacts in parallel, etc. Finally, a complementor is any device possessing one input and one output such that the output is energized when and only when the input is not energized. It may be made of a "break" relay contact, etc.[28]

Now we may write:

$$S = m_1 \cup m_2 \cup m_4 \cup m_7.$$

From which we find:

$$S = M_1 \cap M_2 \cap M_4 \cap M_7.$$

Similarly:

$$C_0 = m_3 \cup m_5 \cup m_6 \cup m_7$$

---

[28] See Proc. I.R.E., "Standards on electronic computers: definitions of terms, 1950," vol. 39, p. 271; March, 1951, for similar definitions. Insofar as relay circuits are concerned, we are considering *transmission* characteristics rather than the "hindrance" of references (2) and (9). Transmission properties are more directly ascertainable and they more closely resemble the attributes of other than relay circuits.

which yields:

$$C_0 = M_3 \cap M_5 \cap M_6 \cap M_7$$[29]

or, by decomposition into simplest elementary components:

$$C_0 = \{(A_1 \cup A_2) \cap (A_1 \cup C_i) \cap (A_2 \cup C_i)\}.$$

It follows that a physical realization of the one-column binary adder which is the dual of that shown on Fig. 6 may be obtained simply by interchanging $\cap$ and $\cup$ throughout. The functions performed and the circuits involved are exactly the same as in the case of Fig. 6 but intersectors and unitors are interchanged.

II. It is well known that many other physical realizations of the binary adder are possible. An interesting and useful one is that which utilizes two half adders in cascade. A half adder is a device which performs the addition of only two binary digits (instead of three) supplying a sum S and a carry C_0. No provision is made for a carry C_i from the preceding stage.[30] The correspondence table of a half adder is:

A_1	A_2	S	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A convenient physical realization of the half adder is one using seven logical elements connected as shown in Fig. 7.

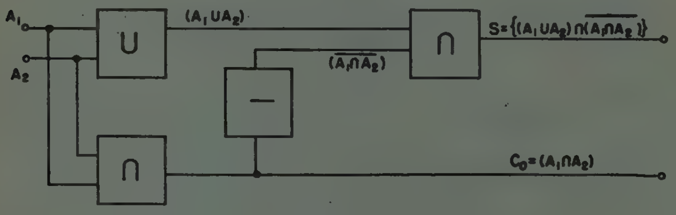


Fig. 7—Block diagram of half adder.

The complete adder is shown on Fig. 8, together with detailed indications of the functions performed by each component. To show that the S and C_0 obtained are actually identical to the functions desired, we transform the outputs S and C_0 as given in Fig. 8 to one of the canonical forms. We have from the figure:

$$S = \{[(A_1 \cup A_2) \cap \overline{(A_1 \cap A_2)}] \cup C_i\}$$
$$\cap \{(\overline{A}_1 \cap \overline{A}_2) \cup (A_1 \cap A_2) \cup \overline{C}_i\}$$

From which we find successively:

$$S = \{[(A_1 \cup A_2) \cap (\overline{A}_1 \cup \overline{A}_2)] \cup C_i\} \cap \cdots$$
$$\cdots \cap \{(\overline{A}_1 \cup A_1 \cup \overline{C}_i) \cap (\overline{A}_1 \cup A_2 \cup \overline{C}_i) \cap \cdots$$
$$\cdots \cap (\overline{A}_2 \cup A_1 \cup \overline{C}_i) \cap (\overline{A}_2 \cup A_2 \cup \overline{C}_i)\}$$
$$S = \{(A_1 \cup A_2 \cup C_i) \cap (\overline{A}_1 \cup \overline{A}_2 \cup C_i) \cap \cdots$$
$$\cdots \overline{C}_i \cap (\overline{A}_1 \cup A_2 \cup C_i) \cap (A_1 \cup \overline{A}_2 \cup \overline{C}_i)\}$$
$$S = M_1 \cap M_2 \cap M_4 \cap M_7.$$

Likewise:

$$C_0 = (A_1 \cap A_2) \cup \{(A_1 \cup A_2) \cap \overline{(A_1 \cap A_2)} \cap C_i\}$$
$$C_0 = (A_1 \cap A_2) \cup \{(A_1 \cup A_2) \cap (\overline{A}_1 \cup \overline{A}_2) \cap C_i\}$$
$$C_0 = \{(A_1 \cup A_2 \cup A_1) \cap (\overline{A}_1 \cup \overline{A}_2 \cup A_1)$$
$$\cap (C_i \cup A_1) \cap (A_1 \cup A_2 \cup A_2) \cap \cdots$$
$$\cdots \cap (\overline{A}_1 \cup \overline{A}_2 \cup A_2) \cap (C_i \cup A_2)\}$$
$$C_0 = \{(A_1 \cup A_2) \cap (A_1 \cup C_i) \cap (A_2 \cup C_i)\}.$$

Since these last expressions for S and C_0 are the same as obtained earlier, it is clear that the device under discussion here does perform correctly as a one-column binary adder.

III. It is well known that through a judicious use of the properties of different sorts of vacuum tubes a one-column binary adder may be built which possesses fewer (physical) logical elements those of examples I and II.

Consider the classical case of two or more triodes the cathodes of which are connected in parallel and to a common output resistor. (The anodes are also connected in parallel and to the $+B$ supply). The cathode side of the output resistor is at a high positive potential (energized) when and only when one or more of the triodes are conducting. That is to say that if energization of each of the separate grids is defined as a swing

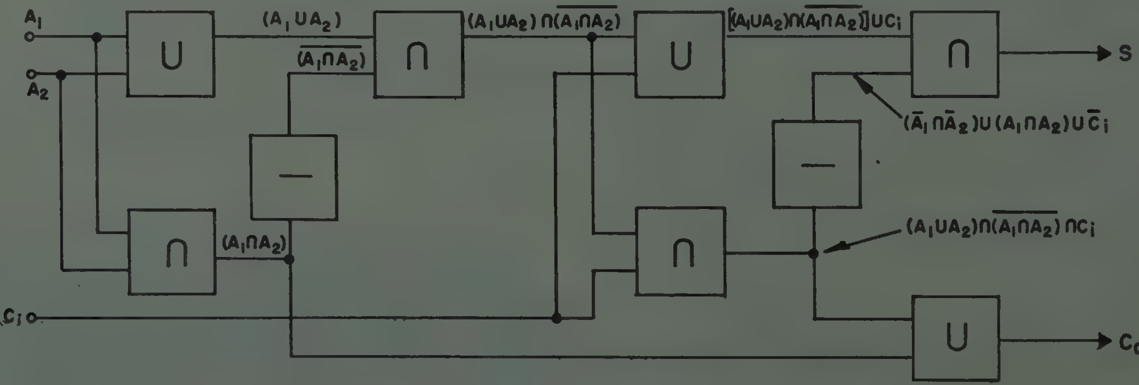


Fig. 8—Block diagram of one-column binary adder using two half adders.

---

[29] As in the present cases of S and C_0, some (but not all) $\genfrac{}{}{0pt}{}{\text{subset}}{\text{superset}}$ canonical representations involving $2^{(n-1)}$ $\genfrac{}{}{0pt}{}{\text{minterms}}{\text{maxterms}}$ possess the same minterm and maxterm numbers in both subset and superset canonical representations.

[30] See Proc. I.R.E., "Standards on electronic computers: definitions of terms, 1950," vol. 39, p. 274; March, 1951.

in the positive direction (from a cut-off state) to a point where conduction is established, and if the sets of instances of energization of the grids are designated by A, B, C, etc., respectively, then the set of instances of energization of the output is $A \cup B \cup C \cup \cdots$ etc. In other words, this circuit, involving say, n triodes, performs the union of n variables corresponding to the n inputs. Note that, in the present case, the output electrical polarity is the same as that of the inputs.

Another classical case is that of a number of triodes the anodes of which are connected in parallel and fed through a common output resistor. (The cathodes are also connected in parallel and grounded.) The anode side of the output resistor is at a high positive potential (energized) when and only when all the triodes are cut-off. This is to say that if energization of each of the separate grids is defined as a swing in the negative direction (from a conduction state) to a point at (or beyond) cut-off, then the set of instances of energization of the output is $A \cap B \cap C \cap \cdots$ etc. In other words, this circuit performs the intersection of as many variables as it contains triodes. Here, the polarity of the output is the same as in the previous case, but the polarity of the inputs is reversed.

It is evident that a single triode with anode output may be used as a complementor. The output is at a high positive potential (energized) when and only when the input grid is not energized in the positive direction (from a cut-off state). The electrical polarities of output and input are the same as those of the triode unitor.

These and many other circuits of the same general class have been fully described in bibliography reference (8). Through the ingenious combination of a number of these circuits, a vacuum tube binary adder requiring only 12 control grids can be built.

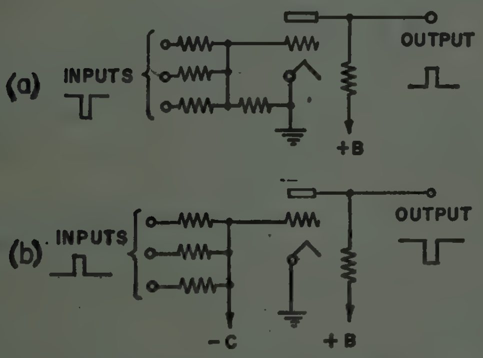


Fig. 9—(a) One-triode unitor. (b) One-triode intersector.

Under certain conditions, the union or the intersection of a small number of variables may be obtained by means of a single triode. Consider the circuit of Fig. 9(a). When no signals are applied to the inputs, the triode is conducting. However, the application of a sufficiently high negative potential to any one or more of the inputs will cause the triode to be cut-off. With say, n inputs, it is sufficient that this negative potential be not less than n times as large as the normal cut-off grid voltage to insure that the triode be cut-off when one or more of the inputs are energized (in the negative direction). It is clear, then, that the set of instances in which the anode output is at a high positive potential (energized) is the union of the sets of instances in which the respective grids are energized (in the negative direction). Note that the cut-off characteristic of the triode provides a reference level insuring that, as long as the conditions specified above are satisfied, the output level is independent of input amplitudes and circumstances. Electrical polarities are the same as those of the triode intersector described above.

To obtain an intersection by means of a similar one-triode scheme, we need only reverse the definition of the energization of both the output and the inputs. The anode output is at a low positive potential (energized state) when and only when all the inputs are energized at (say) cathode potential (Fig. 9(b)). This circuit can easily be derived from that of the one-triode unitor by noting that:

$$A \cap B \cap C \cap \cdots = \overline{(\overline{A} \cup \overline{B} \cup \overline{C} \cup \cdots}.$$

As before, the triode characteristics may be used to insure that the output level be independent of input circumstances.

Using the maxterm representations of S and Co previously obtained (in which these functions are each given as an intersection of four and three unions, respectively) a one-column binary adder has been built which requires only 7 control grids in 7 triodes. The seven unions are performed by means of seven sets of resistors appropriately connected to the seven control grids. The intersection required for S is performed by connecting the first four anodes in parallel and feeding them through one output resistor. Co results from the intersection which is performed by connecting together the other three anodes at a second output resistor.

Acknowledgment

Mrs. K. J. Rupprecht has collected the bibliographical references, prepared and checked examples and given much help in organizing the material for presentation. The author owes much to Dr. V. K. Zworykin for his kind encouragement of this work.

Bibliography

(1) G. Boole, "Investigation of the Laws of Thought," 1854. Dover, New York; 1951 (Reprint).
(2) C. E. Shannon, "A symbolic analysis of relay and switching circuits," Elec. Eng., Transactions Suppl., vol. 57, pp. 713–723; 1938.
(3) G. Birkhoff and S. MacLane, "A survey of modern algebra," New York, Macmillan, 1948; Chap. XI, *Algebra of Classes*, pp. 311–325.
(4) D. R. Hartree, "Calculating instruments and machines," The University of Illinois Press, pp. 99–105; 1949.
(5) C. E. Shannon, "The synthesis of two-terminal switching circuits," *Bell Sys. Tech. Jour.*, vol. 28, pp. 59–98; January, 1949. (Bibliography of 11 Entries).

Bibliography Continued

(6) D. R. Brown and N. Rochester, "Rectifier networks for multiposition switching," Proc. I.R.E., vol. 37, pp. 139–147; February, 1949.
(7) G. W. Patterson, "Logical syntax and transformation rules," Moore School of Elec. Eng., University of Pennsylvania, Research Div. Report 50-8; October 10, 1949.
(8) "Synthesis of electronic computing and control circuits"; Harvard University, Staff of the Computation Laboratory; Harvard University Press; 1951. (Annals of the Computation Lab., No. 27).
(9) Wm. Keister, A. E. Ritchie and S. H. Washburn, "The Design of Switching Circuits," New York, D. Van Nostrand Company, 1951.
(10) I. A. D. Lewis, "A symbolic method for the solution of some switching and relay circuit problems," *Proc. IEE*, vol. 98, pp. 181–191; May, 1951. (Bibliography of 4 Entries).
(11) E. C. Berkeley, "A Summary of Symbolic Logic and its Practical Applications," E. C. Berkeley; 1951.
(12) R. Serrell, (Book review) "Synthesis of electronic computing and control circuits," *Electronics*, vol. 25, pp. 400–406; March, 1952
(13) R. Staehler, "An application of Boolean algebra to switching circuit design," *Bell. Sys. Tech. Jour.*, vol. XXXI, pp. 280–305; March, 1952.
(14) W. V. Quine, "The problem of simplifying truth-functions," *The American Mathematical Monthly*, vol. 59, pp. 521–531; October, 1952.

Dynamic Circuit Techniques Used in SEAC and DYSEAC[*]

ROBERT D. ELBOURN[†] AND RICHARD P. WITT[†], MEMBERS, IRE

***Summary*—As a result of decisions to perform all logical operations in germanium diode circuits, all storage in delay lines and only amplification in tubes, there has been developed a digital computer circuitry whose high degree of standardization offers several advantages. Manufacturing, stocking replacements, and troubleshooting are simplified by having only two types of plug-in packages; moreover very thorough engineering study of these circuits was feasible. The possibilities for constructing logical functions are completely general and each tube can drive gate circuits associated with 14 others.**

INTRODUCTION

DEVELOPMENT OF THE digital computer pulse circuitry to be described began in 1948 with the decision of the National Bureau of Standards to build the Standards Eastern Automatic Computer, SEAC.[1] The functional plan of SEAC was derived from that of the EDVAC built by the Moore School of the University of Pennsylvania. It operates in the serial mode at a one-megacycle pulse repetition rate. Since the completion of SEAC this circuitry has been improved in reliability and efficiency and has been packaged into just two types of etched-circuit plug-in packages which are used in the NBS computer, the DYSEAC.

The first of the decisions which fixed the characteristics of this circuitry was to minimize the number of tubes by performing all the logical operations of "and," "or," and "not" between pulses in circuits comprised of germanium diodes and resistors. Such diode circuits were suggested in a preliminary report on the UNIVAC by the Eckert-Mauchly Computer Corporation and were described with variations by T. C. Chen[2] in early reports on EDVAC.

To extend the life of the diodes, back voltages were kept low by restricting the amplitude of pulses to 10–20 volts. On the other hand complex cascades of diode logic circuits required considerably more driving current than do vacuum tube circuits. Thus there were presented loads of much lower impedance level than vacuum tubes can drive efficiently. An obvious solution was to use small, step-down, pulse transformers such as had been extensively studied at the Massachusetts Institute of Technology;[3] however, there remained the problem of achieving uniform shape and timing of pulses at the high but variable duty cycle that occurs in a serial-type machine.

In addition to supplying large pulse currents at low voltages, the use of pulse transformers has these advantages:

1. Eliminating dc coupling permits all tubes to operate from the same supply voltages.
2. All tubes can operate with positive pulses on the grid, i.e., no inverter stages are required, because with two secondaries each transformer can supply both positive pulses for normal signals and negative pulses for inhibiting.
3. Performance of ac coupled pulse amplifier stages is less critical of tubes, because it depends on only their incremental characteristics.

The disadvantages of transformer coupling stem chiefly from the fact that during a pulse the magnetic flux in the transformer core must increase in direct proportion to the voltage-time area of the pulse and a corresponding magnetizing current is required in addition to the load current. Then after the pulse, to bring the flux and the magnetizing current down again to their original values requires an equal but negative voltage-time area. In other words a negative-going back-swing transient must follow each pulse. This limits the maxi-

---

[*] Decimal classification: 621.375.2. Original manuscript received by the Institute, July 9, 1953. Revision of article from *Transactions of the I.R.E. Professional Group on Electronic Computers*, vol. EC-2, pp. 2–9; March, 1953.

[†] National Bureau of Standards, Washington 25, D. C.

[1] S. Greenwald, R. C. Haueter, and S. N. Alexander," SEAC," Proc. I.R.E., pp. 1300–1313; this issue.

[2] T. C. Chen, "Diode coincidence and mixing circuits in digital computers," Proc. I.R.E., vol. 38, pp. 511–514; May, 1950.

[3] T. F. Wimett, "Low Power Pulse Transformers," Massachusetts Institute of Technology Project Whirlwind Report R-122; December, 1947.

mum duty cycle of pulses to about one-half, so the speed of the computer is only one-half of what it would be with the same rise time and tolerances if the pulse envelope or non-return-to-zero system could be used. However, this inefficiency is more than compensated by the greater power which a tube can deliver with a transformer. There do remain, however, some variations in pulse shape and timing due to variations in magnetizing current between the first and later pulses of a train.

In EDVAC the one-word registers needed in the arithmetic and control units are dynamically circulating loops comprising electrical delay lines, repeater amplifiers, and clocking gates. This scheme is also used in SEAC because it requires fewer tubes than do static flip-flop registers. The logical reduction of this idea to storing an individual pulse in a one-pulse-time circulating loop called a dynamic flip-flop was suggested in the preliminary report on the UNIVAC. In SEAC the dynamic flip-flop completely replaced the Eccles-Jordan type, because it uses only one tube and can drive a number of external gates without additional amplification. These decisions resulted in a one-megacycle repetition rate digital computer circuitry which has basic uniformity in design and clean separation in function:

1. All logical operations are done by diode-resistor circuits.
2. All incidental storage is done by electrical delay lines, and
3. All amplification is done by transformer-coupled pulse amplifiers of a standardized design using only one type of tube.

Since construction of the SEAC circuitry has been improved, first, by increasing the positive grid drive, the plate supply voltage, and the turns ratio to obtain more power output; second, by changing the one-megacycle clock signal from 3-phase to 4-phase to improve timing tolerances; and third, by substituting a smaller, more efficient transformer using a ferrite core.[4] Many features of this circuitry were later adopted by the Moore School in the design of MSAC. Further improvement was achieved by studying the SEAC circuits to find an efficient way to divide them into a few standard plug-in packages. A group at the Air Force Missile Test Station, Patrick Air Force Base, Florida, and another at the Willow Run Research Center of the University of Michigan have each built computers using these packages. More recently, the circuitry has been incorporated into etched-circuit dip-soldered packages of just two types. One contains diode gates and buffers with a tube and transformer. The other contains lengths of electrical delay line and suitable terminating circuits.

Although this paper will describe only the vacuum tube version, it is of interest to note that J. H. Felker has adapted the principles of this circuitry for use with transistors.[5] He retained the configuration of the diode and delay circuits, the repetition rate, and even the impedance levels, but he was able to reduce the levels of voltage and current by nearly a factor of ten and to reduce the physical dimensions accordingly.

THE TUBE PACKAGE

A tube package contains a tube and transformer, five and-gates, an or-gate for feeding the output of the gates of the grid of the tube, an output or-gate to permit the transformer to drive the gates of subsequent packages, and six spare diodes which may be connected to provide additional inputs to the gates as required. The circuit is shown in Fig. 1. In the normal or quiescent condition of no pulses, the diodes of the gates are conducting because their input terminals are held at slightly below −8 volts by being connected to the positive output terminals of preceding packages. Each positive output terminal is held just below −8 volts by its −8-volt limiting diodes which are kept conducting by pull-down resistors to −65 volts. With the output terminals of the and-gates at about −8 volts, the diodes in the or-gate are non-conducting because a limiting diode prevents the 39K (39 kilohm) resistor from pulling the grid down much below −5 volts. The 3-volt back bias on the or-gate diodes protects the grid from noise such as cross-talk on long leads between packages or variations in forward drop across the −8-volt limiting diodes. To achieve the some protection by grid cut-off would require more bias and hence larger pulses, much of which would be wasted in charging the grid capacitance through a region of very low transconductance.

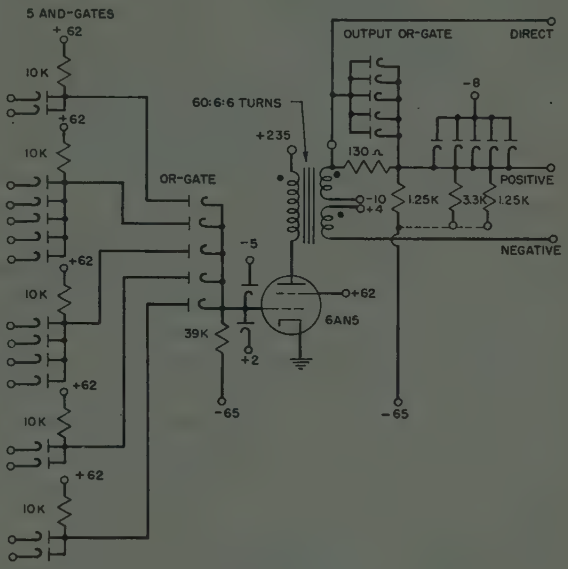


Fig. 1—Circuit diagram of the tube package.

---

[4] F. G. Brockman, "Magnetic ferrites for high frequency uses," *Electrical Eng.*, vol. 68, pp. 1077–1080; December, 1949.

[5] J. H. Felker, "The transistor as a digital computer component," *Review of Electronic Digital Computers*, A.I.E.E. Special Publication S-44, pp. 105–109; February, 1952.

If one compares the direction of low resistance of the diodes in and-gates and in or-gates, it will be apparent that the output voltage of an and-gate approximates its *lowest* input voltage; whereas, the output voltage of an or-gate approaches its *highest* input voltage. Therefore, an or-gate performs the logical "or" function because it will transmit a positive pulse applied to any of its input terminals. On the other hand an and-gate performs the logical "and" function because it can transmit a positive pulse only when all of its input terminals are pulsed positively.

The choice of resistance values depends upon the current requirements which are calculated by working back from the grid. At the end of a pulse, when the or-gate diodes have all cut off but the grid is still at +2 volts, the 39K resistor must pull the grid down by discharging all the parasitic capacitance of the grid circuit. This capacitance is 19 micromicrofarads, and a speed of at least 75 volts per microsecond is required under the most unfavorable combination of 5 per cent tolerances on both supply voltages and resistances. At the leading edge of a pulse the 10K resistor in a gate is able to overcome the 39K resistor and to pull the grid up at 75 volts per microsecond under the worst combination of 5 per cent tolerances and with 19 micromicrofarads capacitance on the and-gate junction. This includes the capacitance of connecting spare diodes as additional inputs to the gate. At the top of a pulse the 10K resistor supplies grid current required to obtain maximum output from the tube, but the limiting diode connected to +2 volts prevents excessive grid current which would occur when two or more and-gates operate simultaneously.

A diode and-gate imposes quite unusual requirements upon the sources which drive it. When a source pulses positively, its gate diode simply cuts off so that practically no current flows. But when a source is *not* pulsing, it must actively exert its veto power by drawing through its gate diode whatever current is necessary to hold the potential of the and-gate down to about −8 volts. Only when all the inputs to a gate go positive simultaneously should the 10K resistor be permitted to pull up the output voltage of the gate and, through conduction of its or-gate diode, to transmit a positive pulse to the grid. Whenever some but not all of the inputs to an and-gate are pulsed, the remaining unpulsed inputs must suddenly accept with little change in voltage a different proportion of the current supplied by the 10K resistor; therefore, a low dynamic impedance is required. By themselves a tube and transformer are not a suitable source, because when not pulsed they may present as much as 300 ohms impedance at one megacycle. The required low dynamic impedance is achieved by the forward conductance of the −8-volt limiting diodes in the output or-gate.

To keep them conducting, even when all other sources pulse, the pull-down resistors which return to −65 volts must draw more current than can be supplied by the 10K resistors in all the and-gates connected to the output or-gate. Because the positive pulse secondary of the transformer returns to −10 volts, the series diodes in the output or-gate are cut off so that none of this current is trapped in the high dynamic impedance of the transformer. When the tube is turned on, a 20-volt pulse appears at the secondary of the transformer, the series diodes conduct, and the transformer supplies the current taken by the resistors to −65 volts. Three resistors are provided to permit the load on the positive output to be adjusted to the number of and-gates actually to be driven. Each 1.25K resistor can hold down five gates and the 3.3K resistor can hold down two. The rest of the rated driving capacity of 14½ gates for the package can be used at the negative and direct outputs. One of the 1.25K resistors is permanently connected to insure there will be at least enough load to prevent excessive screen dissipation. The 130-ohm resistor which shunts the series diodes of the output or-gate adds no load during a pulse but is provides somewhat less than critical damping for the negative-going transient which follows a pulse. The combination of the 130-ohm damping resistor and the permanently connected 1.25K resistor is sufficient to prevent the underdamped transient from going above −8 volts.

The function of inhibiting an and-gate is accomplished by connecting the negative output of a transformer directly to an input diode of the gate. Because the negative winding returns to +4 volts, this diode is normally non-conducting and does not affect the operation of the gate. But whenever a negative pulse is applied to this diode it becomes the most negative input to the gate and by conducting prevents any positive output at that pulse time. An inhibiting connection does not require an and-gate ahead of it because it carries current only during a pulse at which time the tube and transformer present a very low impedance.

The direct output terminal of the transformer is used to drive electrical delay lines which present a linear resistive load and to drive or-gates other than the output or-gate.

If one is familiar with Boolean algebra[6] he will see that the configuration of diode logic circuits in these packages will allow one to realize any required logical operation. In Boolean algebra "and," "or," and "not" are a complete set of connectives; moreover, the pattern of a set of and-gates feeding one or-gate corresponds to one of the normal forms in which every Boolean proposition can be stated.

For the logical description of computing machines it is certainly desirable to have a more compact symbolism than the complete circuit diagrams. Fig. 2 shows the circuit of the tube package in a logical symbolism devised when SEAC was designed and also in a briefer symbol appropriate when these packages are used. With the addition of numbers for package location and pin designation, the latter symbol can be the basis of a single-drawing description which can replace logical diagrams, circuit diagrams, and layout charts. Lines carrying negative pulses are marked by a small circle at each end.

---

[6] G. Birkhoff and S. McLane, "A Survey of Modern Algebra," Macmillan Co., New York, N. Y., Chap. 11; 1944.

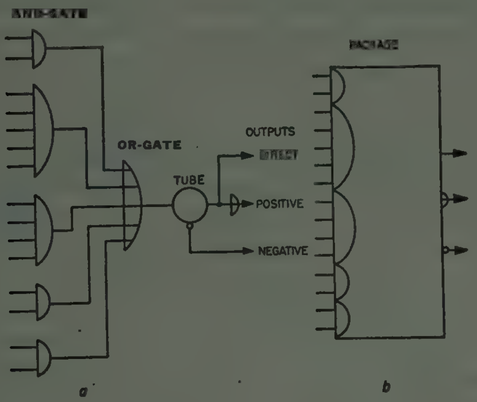


Fig. 2—Logical diagram symbols for the circuit of the tube package, (a) in SEAC notation, (b) in simplified notation.

Pulses are standardized in shape and timing, and the entire computer is kept in synchronism by making a clock pulse one input to every and-gate. Actually the clock pulses are distributed as one-megacycle sine waves at 30 to 45 volts peak-to-peak amplitude. However, the effective waveform is just the trapezoidal center slice which lies between the −5 and +2 volt grid clipping levels. The delay through a tube and transformer is much less than one microsecond; in fact, the best timing tolerances are obtained when the clock pulses in successive stages are separated by about one-quarter microsecond; therefore, four phases of one-megacycle sine waves are used for clock pulses. Fig. 3 shows the waveform of a typical pulse at the secondary of a transformer.

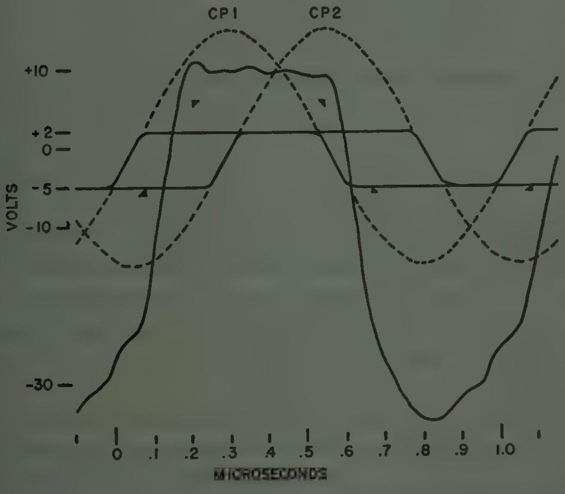


Fig. 3—Waveform of a typical pulse with the clock pulse from which it was derived and the clock pulse with which it will be reclocked. Black triangles mark the critical timing limits.

The signal on the grid of that stage was the −5 to +2 volt slice of clock phase CP1, while in the next stage the pulse will be gated with clock phase CP2. Notice that the signal pulse does not cover CP2; it cannot because it is too narrow. However, the overlap of the signal pulse with CP2 is sufficient to turn on the next stage; then, once it has been turned on, its own output can be fed back to keep it on until the end of CP2. This trick, called "generative broadening," is illustrated in Fig. 4 which shows the logical diagram of two dynamic flip-flops connected together to form part of a shifting register. Either stage may be turned on in one of two ways. The first is by the coincidence of a pulse from the memory and a Read pulse, the second by the coincidence of a pulse from the preceding stage and a Shift pulse. When coincidence does occur the active gate does not rise until such time as the clock pulse CP2 also starts to rise. After the output has risen, the input pulses may fall because the regenerative signal will keep the tube on via the upper gate until the end of CP2. The output signal delayed 0.75 microsecond arrives at the bottom gate with the next rise of CP2 and so permits the tube to be turned on again. The bottom gate can transmit a signal only during the overlap of CP1 and CP2 (see Fig. 3). This is wide enough to initiate regeneration but narrow enough to be covered by a negative pulse (−) Hold which can inhibit the bottom gate and so stop circulation in the flip-flop. Other computer circuits are built up in a very similar fashion.

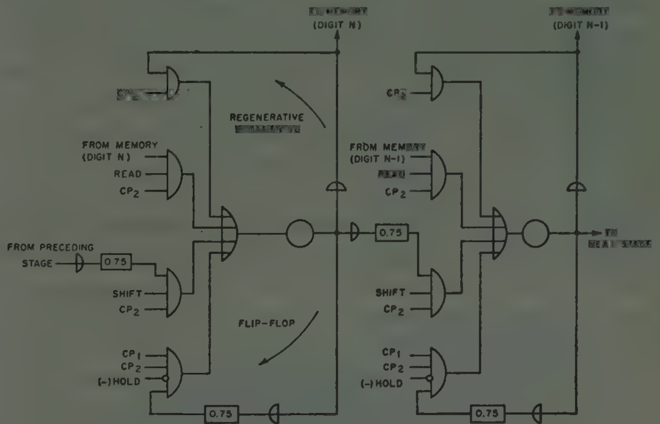


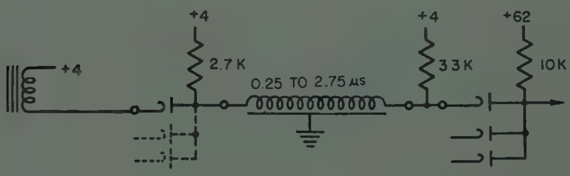
Fig. 4—Two stages of a typical shifting register.

The Delay Line Package

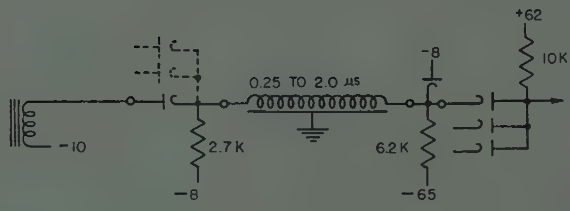
An electrical delay line is used to enable a transformer to drive a gate which is clocked by a later phase than the next; therefore, only integral multiples of 0.25 microsecond delay are required. The problem of reflections from the nonlinear gate loads could be avoided if the characteristic impedance were made so low that the terminating resistance would swamp the nonlinear load of the gate, but this would require a wastefully large driving current. Instead the characteristic impedance is made equal to the pulse voltage divided by the current drawn at the top of a pulse; thus, the line is matched for the main body of a pulse so that only narrow reflections occur during the rise and fall. These are reduced to negligible size by dispersion in transmission and by partial absorption in an input termination.

The type of delay line used was described by Blewett and Rubel.[7] It is built up from the inside out of: (1) a core of plastic tubing; (2) a close-wound helix of very fine wire; (3) a sprayed layer of aluminum paint; (4) two layers of Teflon tape; (5) a grounded braid of insulated wires; and (6) a protective cotton serving. Its characteristic impedance is 1350 ohms and a 0.25 microsecond section is about five inches long.

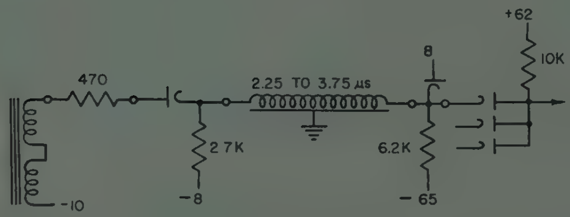
A delay line package contains one 0.75-microsecond section and twelve 0.25-microsecond sections along with terminating circuits for five positive pulse lines and for two negative pulse lines. Sections may be connected in series at the socket to obtain other lengths. Fig. 5 shows the termination circuits connected between a transformer and the line at the input end and between the line and a gate at the output.[7] Spare diodes from a tube package may be connected as shown by dotted lines to form an or-gate between several inputs to a line.



a. FOR NEGATIVE PULSES



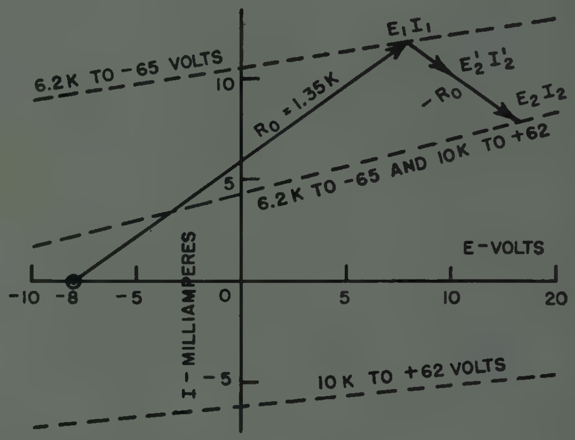
b. SHORT LINES FOR POSITIVE PULSES



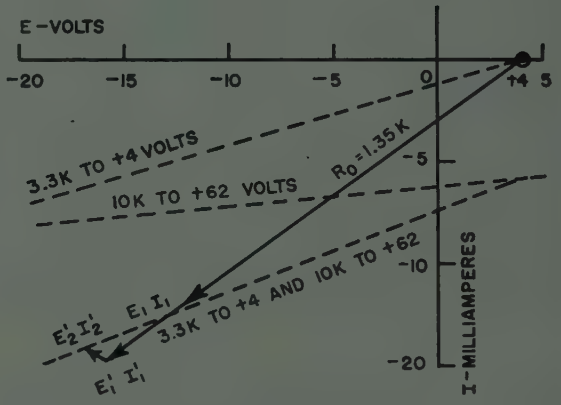
c. LONG LINES FOR POSITIVE PULSES

Fig. 5—Termination circuits for electrical delay lines.

Volt-ampere diagrams in Fig. 6 show how the load-end terminations match the characteristic impedance of the delay line for incident pulses of 16 volts amplitude. The terminal voltage and current is a superposition of an incident wave and a reflected wave which must exactly satisfy the terminal resistance conditions. For the incident wave the ratio of voltage to current is just the characteristic impedance, while for the reflected wave it is the negative of this because either the voltage or the current must be reversed by reflection. Dotted lines show the terminal resistance conditions; E_1I_1 denote the incident wave and E_2I_2 the reflected wave.



A) POSITIVE PULSE TERMINATION



B) NEGATIVE PULSE TERMINATION

Fig. 6—Volt-ampere diagrams for delay-line terminations.

For a positive pulse line (Fig. 6A) the 6.2K resistor returned to -65 volts exactly terminates a 16-volt incident pulse when the pulse renders the and-gate diode nonconducting. The more obvious termination of a 1.35 resistor to -8 volts cannot be used because it would not hold the and-gate down firmly to -8 volts whenever there is no pulse on the line.

If an incident pulse arrived when all the other inputs of the and-gate were so positive that the 10K resistor remained connected to the line at the top of the pulse, then a reflected wave E_2I_2 would be produced; however, positive pulses (other than clock pulses) do not rise above $+10$ volts so only the smaller reflection $E_2'I_2'$ will be produced. This is comparable in magnitude to the small reflections which are caused by an incident pulse having more or less than 16 volts amplitude because it has suffered more or less attenuation in a longer or shorter delay line than average, or else are caused by variations within the voltage and resistance tolerances.

---

[7] J. P. Blewett and J. H. Rubel, "Video delay lines," Proc. I.R.E., vol. 35, pp. 1580–1584; December, 1947.

For a negative pulse line (Fig. 6B) a 16-to-17-volt incident pulse is correctly terminated by the 3.3K and 10K resistors acting together. A 20-volt pulse $E_1'I_1'$ will suffer a small reflection $E_2'I_2'$. A somewhat larger reflection is produced if negative pulses from two delay lines arrive simultaneously at the same and-gate and thus have to share the 10K resistor. The 2.7K resistors in the input terminations absorb enough energy from the small returning reflections to prevent their accumulating seriously in the line, but they do not require as much initial pulse current as would terminations equal to the characteristic impedance of the line. The input diodes disconnect the line from the back-swing transient of the transformer. In long lines the attenuation due to the series resistance of the line (about 1 db per μsec) is so great that extra input voltage is required. Connecting both secondaries of the transformer in series gives more than enough voltage, so a 470-ohm series resistor is added to reduce the effective load and to drop the excess voltage which would produce undesirable reflections.

An output termination intended for a positive line, i.e., a -8 volt limiting diode and a 6.2K resistor to -65 volts, can be used alternatively as an or-gate between the direct output terminals of several packages and the input of an and-gate by connecting spare diodes as series input diodes for the or-gate. Two terminations in the delay line package are provided with buffer diodes already attached for this purpose.

Design of the Pulse Amplifier

The type 6AN5 tube was selected as possessing the best combination of high transconductance, low capacitances, reasonably high current and dissipation ratings, an an efficient heater-cathode structure. Its pertinent characteristics are:

Heater voltage	6.3	volts
Heater current	0.45	ampere
Input capacitance	9.0	micromicrofarads
Output capacitance	5.0	micromicrofarads
Maximum screen dissipation	1.4	watts
Maximum average cathode current	50.0	milliamperes
Minimum increment of plate current between $E_{c_1}=-5$ volts and $E_{c_1}=+2$ volts at $E_p=E_{c_2}=62$ volts	42.0	milliamperes.

The plate dissipation rating is 4.2 watts with 120 volts on plate and screen, and 1.7 watts with 300 volts on plate and screen. In this pulse amplifier the plate dissipation tends to be low because the instantaneous plate voltage is quite low during a pulse. Plate dissipation exceeds 2.0 watts in only those tubes which have an unusually large plate current at 5.0 volts bias. In service very few heater failures have occurred and no evidence of cathode interface resistance has developed. Some tubes whose heaters were operated at 6.5 volts lost emission at about 3,000 hours, but most tubes operated at 6.3 volts or below have survived well over 10,000 hours.

Fig. 7 shows (1) plate characteristic curves of 6AN5's at grid voltages of -5 and $+2$; (2) the spread in plate current between high limit and low limit tubes; and (3) the load line presented by the output buffer. The reasons for the remarkably low position of the load line and many other design considerations are best explained while following the operating point on the e_p, i_p diagram through a complete pulse cycle.

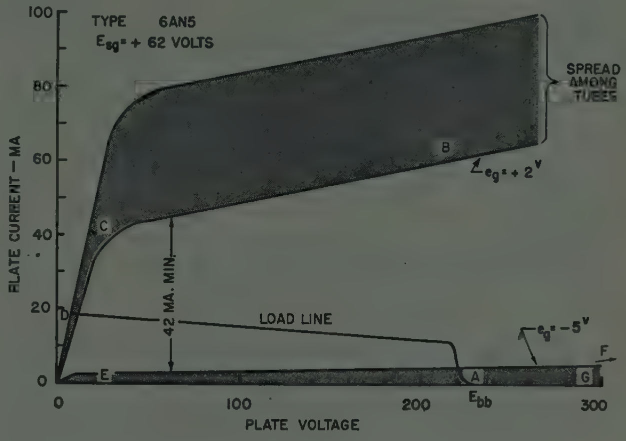


Fig. 7—Plate characteristic curves with load line.

Before the first pulse the plate is at the supply voltage; so the operating point is at A. If the grid is turned on suddenly, the plate current quickly rises to B and must both supply the load and charge all the parasitic capacitances to bring the plate voltage down to C and finally to D. Now a high ratio of primary to secondary turns on the transformer will give a high ratio of secondary to primary current, but it will also require a higher primary voltage to give the required secondary voltage; therefore, more of the plate current will go into the plate capacitance rather than into the primary of the transformer. So there is a problem of finding the turns ratio N which will give the most secondary current I_s for given plate current I_p, plate capacitance C_p, required secondary pulse amplitude E, and allowed rise time T. If the currents are taken as the average values during the rise, one may write

$$I_s = N(I_p - NEC_p/T).$$

By equating to zero the derivative of I_s with respect to N, one can find the optimum turns ratio

$$N_{\text{opt}} = \frac{I_pT}{2EC_p}.$$

This result is easy to remember because it says that just half the plate current should be used to charge the plate capacitance. The corresponding secondary current is

$$I_s = \frac{I_p^2 T}{4EC_p}.$$

Because the secondary current increases with the square of the plate current, it pays large dividends to drive the grid as positive as the dissipation ratings will allow. In this design the plate capacitance, including socket, wiring, and equivalent primary capacitance of the transformer, is 10 micromicrofarads; the required secondary pulse amplitude is 20 volts; and the allowed rise time is roughly 0.1 microsecond. For a plate current of 40 milliamperes obtained from a low limit tube with positive grid drive, the optimum turns ratio is 10 and the secondary current 200 milliamperes. This calculation is admittedly only approximate since it uses average currents during the rise, and the allowed rise time is determined very differently in practice; nevertheless, experiments confirmed the choice of a 10-to-1 turns ratio. In addition to the delay of charging the plate capacitance, the output pulse is further delayed about 0.02 microsecond by the leakage inductance and the load capacitance.

When the plate voltage reaches the knee C, the plate current quickly drops to the intersection with the load line at D. At this point a load of at least one 1.25K resistor in the output or-gate is required to prevent excessive screen dissipation. The steep slope of the plate characteristic in this region provides a very uniform pulse height between high limit and low limit tubes and between first and Nth pulses in a train. The high-frequency ringing seen on top of the pulse in Fig. 3 comes from resonance between the leakage inductance and the load capacitance. Inductance in the −10 volt supply lead adds directly to the leakage inductance; therefore, close by-passing is desirable.

As the pulse continues, the transformer requires a magnetizing current which increases as the voltage-time area of the pulse, so the operating point gradually drifts up toward C. To prevent its passing around the knee of a low-limit tube before the end of the pulse requires at least three millihenries open-circuit primary inductance.

At the end of the pulse, when the grid turns off, the plate current drops from C to E, and the magnetizing current and load current combine to discharge the parasitic capacitances rapidly to A. Beyond this point the output pulse swings negative as the operating point moves on toward F, because the magnetizing current continues to excite an oscillation of the open-circuit inductance of the transformer with plate capacitance. Load capacitance is disconnected by the output or-gate. If this oscillation is not damped, a spurious positive pulse will appear in the next half cycle. On the other hand, if it is over-damped, the magnetizing current will not be quenched before the next pulse time, and it will subtract from the charging current available at the leading edge. The best compromise is to make the transient slightly under-damped in an effort to bring the magnetizing current to zero at the leading edge of the next pulse. In this type of transient the current passes through zero appreciably before the voltage does, so at the start of the next pulse the operating point may be at G; however, the very large charging current available there charges the plate capacitance to B with very little time delay.

Because the open-circuit inductances of the transformers employed vary with a standard deviation of about six per cent, it is not possible always to make the magnetizing current exactly zero at the start of the next pulse. If the magnetizing current increases by an amount I during each pulse and is attenuated by a factor k in each interval between, then the magnetizing current at the start of an Nth pulse approaches (as N approaches infinity)

$$((Ik + I)k + I)k + \cdots = \frac{Ik}{1 - k}.$$

In the worst case, with the primary open-circuit inductance at its upper limit of 4.5 millihenries, solution of the RLC transient gives $k = 0.24$. This leads to an estimate of 5.6 milliamperes for the remaining magnetizing current. Experiments with a low-current tube confirm both the slower rise of an Nth pulse with a high inductance transformer and the earlier fall at the trailing edge when the inductance is too small.

The foregoing theory is not accurate enough to define a final design; instead it provided a reasonable point of departure and helped to interpret the timing tests which were the real criteria of the design. The central objects of the timing studies are four critical timing limits marked in Fig. 3 by black triangles. Two of these define an interval over which the pulse at the secondary of the transformer must be above +6 volts, and the other two define an interval through which it must be below −6 volts. The level of +6 volts allows for drop in the series diodes of the output buffer and for attenuation in delay lines. On one hand these limits are the results of a paper study of the logic circuits in a computer. All the various possibilities for gating or inhibiting between direct pulses or pulses whose waveforms have been distorted by transmission through delay lines were studied to find just what timing limits would insure correct operation. This requires that the pulse to be gated or inhibited is always properly overlapped and yet that no adjacent pulses are improperly affected.

On the other hand the timing limits are the result of scaling hundreds of photographs of output pulses obtained under the most unfavorable combinations of the following conditions: first versus Nth pulse, high current versus low current tube, maximum versus minimum resistive load, no load capacitance versus 300 micromicrofarads, 4.5 versus 3.0 millihenries primary open-circuit inductance, maximum pull-up current in the and-gates with minimum pull-down current in the or-gate versus the opposite, and 45 versus 30 volt peak-to-peak clock pulse amplitude. These two definitions of the critical timing limits allow some give and take through adjustable parameters, so the final design was reached by successive approximations.

At the same time a set of loading restrictions was obtained of which the most noteworthy follow. The maximum resistive load is the equivalent of $14\frac{1}{2}$ gates in addition to the regenerative broadening connection which is always present. With this load there may be up to 300 micromicrofarads of wiring capacitance. With smaller loads there may be more capacitance until a maximum of 1,000 micromicrofarads is reached with nine gate loads or less. A negative input to an and-gate counts as only 0.75 of a gate load, a short delay line as 1.75 gate loads, and a long delay line, which requires double amplitude drive, as six gate loads.

THE TRANSFORMER

The transformer is completely enclosed by its two-piece cup core in the form of a short cylinder 9/16-inch in diameter by 5/16-inch high. The core is a magnetic ceramic, specifically, sintered manganese-zinc ferrite with approximately the following properties:

Initial permeability	1000
Saturation induction	3400 gauss
Curie temperature	130°C
Resistivity	100 ohm-cm.

Its very low core loss and high effective permeability at one megacycle, as compared with silicon-iron laminations, are primarily due to its resistivity being over two million times higher. While the separate losses are quite difficult to measure or to estimate accurately, one can compute that the total loss in the transformer is probably less than 0.1 watt because the temperature rise under steady pulsing measures less than 15°C.

Instead of being wound in layers the three windings are arranged side-by-side in deep narrow slots turned in a circular nylon bobbin. The slots for the 6-turn secondaries are just wide enough for one wire, hence the turns pile up radially. The slot for the 60-turn primary is 5 to 6 turns wide, thus the primary automatically piles up in an approximately bank-wound arrangement which gives low distributed capacitance. The primary is placed at one side rather than between the secondaries, so that the inside ends of the primary and secondaries can be kept away from each other. Because the positive pulse output has the more critical timing, it is taken from the nearer secondary which has the smaller leakage inductance. The windings must be carefully insulated from the core because ferrit is very abrasive and is a good enough conductor to provide a break-down path between primary and secondary.

The core is assembled with no spacer in the butt joint between the ground surfaces of the halves. When one observes that the total reluctance of the magnetic circuit is equivalent to that of an air gap only 0.0006 inch long in the center leg, one can appreciate the importance of cleanliness and accurate contact of the ground surfaces. Completed transformers, though apparently held together securely by a screw, fibre washers, and lock washers, showed serious inductance changes with rough handling until dipping in a hard-setting epoxy resin was adopted.

For acceptance, the open-circuit primary inductance is measured at 250 kilocycles with a Q-meter. Acceptance limits are 3.4 to 4.2 millihenries, although the timing tests were run at 3.0 and 4.5. The small size and high effective permeability make the stray parameters of the transformer quite small. The capacitance between the primary and the nearer secondary is 3.1 micromicrofarads of which only about one-third is effectively across the primary if the assumption that the pulse voltage varies linearly along the windings is valid. The following table shows various short-circuit inductances measured on a transformer whose primary open-circuit inductance was 3.34 millihenries. Subscripts 1 and 2 denote terminals of the primary; 3 and 4, terminals of the nearer secondary; and 5 and 6 those of the farther secondary:

L_{12} (34 shorted) = 45.00 microhenries
L_{12} (56 shorted) = 80.00 microhenries
L_{33} (12 shorted) = 0.65 microhenry
L_{56} (12 shorted) = 0.97 microhenry.

ACKNOWLEDGMENT

The original SEAC version of this circuitry was developed through the closely integrated efforts of a group which included S. N. Alexander, R. D. Elbourn, S. Greenwald, R. C. Haueter, S. Lubkin, W. L. Martin and R. J. Slutz. The extension to the present version was carried out primarily by R. P. Witt with the cooperation of R. D. Elbourn, S. Greenwald, R. C. Haueter and the Communication Measurements Laboratory, Inc., which laid out and produced the etched circuitry.

The Design of Logical OR-AND-OR Pyramids for Digital Computers*

S. E. GLUCK†, ASSOCIATE, IRE, H. J. GRAY, JR.†, ASSOCIATE, IRE, C. T. LEONDES†, ASSOCIATE, IRE, AND M. RUBINOFF†, ASSOCIATE, IRE

Summary—This paper first considers design techniques of widespread use in the field today. As an example of these techniques, design values for the circuits of the Moore School Automatic Computer (MSAC) are presented. Some recently developed design techniques are then presented which offer marked improvements. These techniques are compared with those presented earlier by listing design values for comparable performance. The paper also considers some of the basic philosophies involved in the choice of elements for logical "OR-AND-OR" pyramids. It concludes with a description of reduced circuits which, when combined with the new techniques, make possible a 50-fold saving in power.

I. INTRODUCTION

IN EXISTING digital computers widespread use is made of cascaded coincidence and mixing circuits employing germanium diodes. The functions of the coincidence and mixing circuits in digital computers are those of the logical "AND" and the logical "OR" respectively. The form often assumed by the cascaded networks is that of a logical "OR-AND-OR" pyramid at the apex of which is a pulse power amplifier. Regeneration is also generally provided to maintain both the shape and the machine timing of the output pulse of the pyramid. The form of the circuits is as shown in Fig. 1. Additional "AND" inputs may be connected at the junction P_2 and additional "OR" inputs at P_1 or P_3. A logical drawing of the form assumed for a typical pyramid of simple nature with provisions for regeneration is shown in Fig. 2.

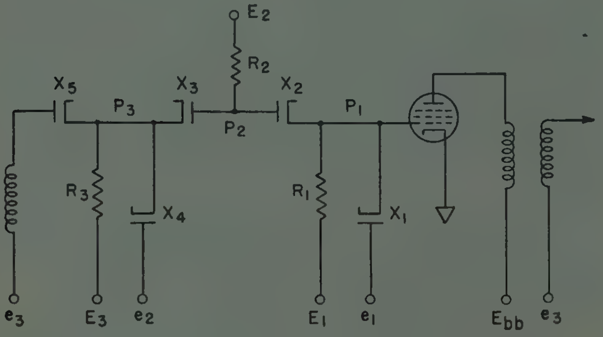


Fig. 1—Schematic diagram of basic pyramid.

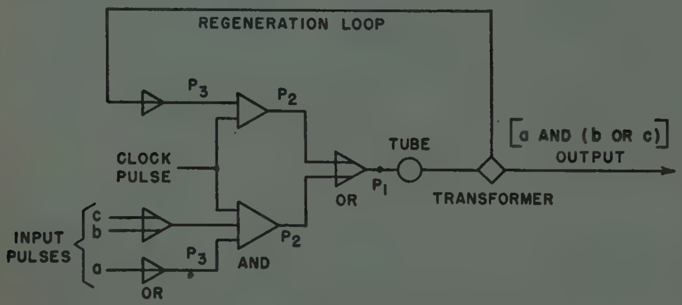


Fig. 2—Logical diagram showing three inputs and regeneration.

The values assumed by the resistors and voltages in Fig. 1 are a function of the rise and fall times desired, and are dependent upon existing stray capacitances, vacuum tube characteristics, and the characteristics of the diode employed.

II. PRESENT-DAY DESIGN TECHNIQUES

In present day designs[1,2] the technique usually employed in selecting the values for resistors and voltages involves initially the determination of parameters at the apex of the pyramid and then proceeding back until the input to the pyramid is reached.

An assumption usually made is that during fall time negligible current flows through X_2. The voltage e_1 is selected to maintain the tube in a state of relatively low conduction,[3] for nominal plate and screen grid voltages, during the condition of no signal. The resultant circuit is that shown in Fig. 3.

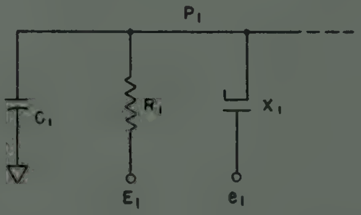


Fig. 3—Effective circuit for fall time.

The magnitude of R_1 is chosen on the basis of desired fall time, t_f, using the easily derived

$$\frac{t_f}{R_1C_1} = \ln \frac{V_p - E_1}{V_0 - E_1}, \tag{1}$$

where C_1 is the total capacitance at the point P_1, V_p is the voltage assumed by point P_1 during the pulsed state, and V_0 is equal to e_1 less the drop in X_1 due to the current flowing from e_1 to E_1.

The magnitude of E_1 is chosen large enough to prevent untoward current changes through R_1 when the voltage rises to V_p (i.e. $E_1 \gg V_p - V_0$) and small enough to assure "reasonable" power consumption. It may be noted that the back resistance of the crystal X_1 and the input resistance to the vacuum tube are shunted across R_1.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, May 20, 1953.

† Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa.

[1] R. D. Elbourn and R. P. Witt, "Dynamic circuit techniques used in Seac and Dyseac," TRANS. I.R.E. PGEC, vol. EC-2, pp. 2–9, March, 1953.

[2] "MSAC Diode Circuit Technical Memorandum," Moore School Research Div. Rep. 52–03; July 1, 1951.

[3] *Ibid.*, p. 33.

However, the effects of these two are small and may be ignored. In any event they actually speed up the fall time slightly so that ignoring them only results in a more conservative design.

The resistor R_2 is determined from the magnitude of the desired rise time, t_r. The circuit to be considered is shown in Fig. 4. Taking into account initial conditions the equation for rise time is

$$t_r = \frac{C_1+C_2}{G_1+G_2+(n-1)G_{B2}} \times \ln \frac{E_2G_2+E_1G_1+E_{p2}(n-1)G_{B2}-V_0(G_2+G_1+(n-1)G_{B2})}{E_2G_2+E_1G_1+E_{p2}(n-1)G_{B2}-V_{0p}(G_2+G_1+(n-1)G_{B2})} \quad (2)$$

where C_2 is the stray capacitance at P_2, n is the number of inputs X_2 at P_1, $G_2=1/R_2$, $G_1=1/R_1$, $G_{B2}=1/R_{b2}$, R_{b2} is the back resistance of the other X_2 crystals tied to P_1, and E_{p2} is the voltage at which P_2 resides during the no-pulse state. It may be seen from Fig. 1 that E_{p2} is roughly equal to e_2.

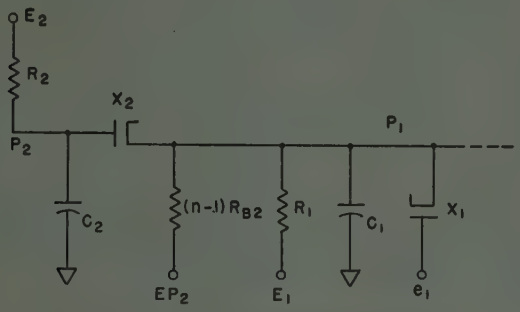


Fig. 4—Effective circuit for rise time.

Actually during the first part of the rise time of the circuit there is a delay until the crystal X_2 starts to conduct due to the time taken to charge C_2 through R_2 from the value E_{p2} to V_0. But, this delay is insignificantly small and may be ignored. As before, E_2 is chosen consistent with conditions of reasonable power consumption and small changes in current through R_2.

The voltage e_2 is selected sufficiently below e_1 to minimize the likelihood of transmission to the grid of small spurious input signals. Also it should be selected as positive as possible to reduce necessary driving signal amplitude and so reduce time delay through the system.

The voltage e_3 should be sufficiently negative to prevent static conduction of the X_5 diode. It should also be as positive as possible to reduce the necessary driving signal amplitude and thus reduce time delay.

In the determination of R_3 it is clearly advantageous and usually possible to set E_3 equal to E_1. R_3 is then selected on the basis of either of the following criteria, whichever is applicable in the particular case: (a) The clamping diode X_4 must never be quiescently in a nonconducting condition. This condition must hold even when current flows into P_2 through all other X_3 crystals in the multi-input AND gate. (b) The fall time of the point P_2 should not exceed the desired value. Reverse currents in the X_3 crystals are a factor here.

The equation for determining R_3 on the basis of the first criterion is

$$0 = I_{X4} = \frac{1}{R_3}(e_2-E_3) - \frac{1}{R_2}(E_2-e_2)-(n-1)I_b, \quad (3)$$

where I_{X4} is the current through the crystal X_4, n is the number of inputs to P_2, and I_b is the maximum value of back current which may flow through any X_3 crystal during the pulsed state. The circuit to be considered for the determination of R_3 on the basis of the second criterion is shown in Fig. 5, for which the time of fall, t_f, may be shown to be

$$t_f = \frac{C_2+C_3}{G_2+G_3+(n-1)G_{x3}} \times \ln \frac{E_2G_2+E_3G_3+e_p(n-1)G_{x3}-V_p(G_2+G_3+(n-1)G_{x3})}{E_2G+E_3G_3+e_p(n-1)G_{x3}-E_{p2}(G_2+G_3+(n-1)G_{x3})}, \quad (4)$$

where C_3 is the stray capacitance at P_3, G_{x3} is the back conductance of the X_3 crystals, n is the number of X_3 crystals at P_3, and e_p is the amplitude of the input pulse to the circuit. It may be noted that actually during the first part of the fall time of the pulse there is a slight delay until the crystal X_3 starts to conduct due to the fact that P_3 must fall from e_p to V_p. However this delay is insignificantly small and may be ignored.

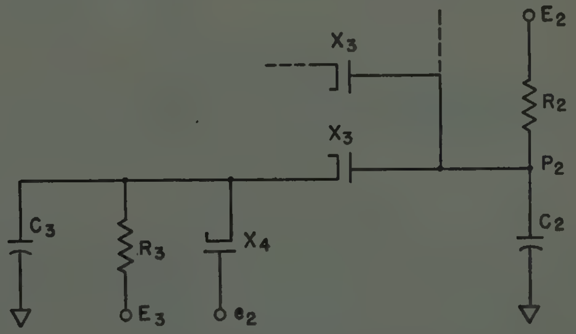


Fig. 5—Circuit to determine R_3.

As an example of these design techniques the values assumed by voltages and resistors for a one word input circuit are shown in the first column of Table I.

TABLE I

Typical Design for a Pyramid Using 30V Input Pulses

Design Technique	Old	New
Tube	6AG7	6AG7
E_{bb}	+250	+250
E_{sc}	+105	+105
e_1	−4.5	−4.5
E_1	−70	None
R_1 or R_1'	33 k	4.7 k
E_2	+70	+35
R_2	11 k	12 k
e_2	−7.5	−7.5
E_3	−70	−35
R_3	4.7 k	4.7 k
e_3	−10.5	−10.5
Diode Type	CK713 or IN38	CK713 or IN38
Rise Time	0.1 μs	0.1 μs
Fall Time	0.1 μs	0.1 μs
Voltage Tolerance	±5%	±5%
Resistance Tolerance	±10%	±10%
C_1	25 μμf	25 μμf

III. THE NEW DESIGN TECHNIQUES

The first step in the new design techniques involves the elimination of R_1 and E_1 in Fig. 1. In their stead a resistor, R_1', is shunted across the crystal X_2. The magnitude of this resistance is determined by the desired fall time of the circuit. In the new circuits the crystals X_5 and X_4 are eliminated in clock pulse inputs.

Therefore, the circuit for determining the magnitude of R_1' is shown in Fig. 6, where the voltage at P_1 is to go from the value during the pulsed state which will be designated by V_p to the value V_0 (where V_0 is as defined before) and C_1 is the distributed capacitance at the point P_1. The voltage at P_2 will be quite different due to the overshoot of the clock pulse. However, this acts in favor of the designer so that actually a conservative estimate of the fall time is obtained. In addition the presence of the back current of the crystals X_2 acts in favor of the designer and may be ignored.

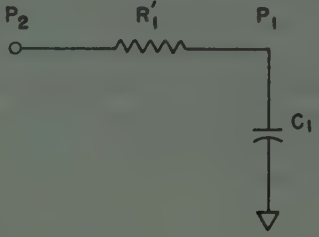


Fig. 6—Circuit to determine R_1'.

The resistance R_1' is then obtained from this expression for the fall time of the circuit of Fig. 6.

$$t_f = R_1'C_1 \ln \frac{V_p - e_3}{V_0 - e_3}. \qquad (5)$$

When there are n X_2 diodes, R_1' will consist of $(n-1)$ resistors, of equal resistance, $(n-1)R_1'$, shunting all the X_2 crystals except that employed in the regeneration loop. In this manner the rise time of the circuit is aided as will presently become evident.

Referring again to Fig. 1, the resistor R_2 and the voltage E_2 in the new circuits are determined from the circuit shown in Fig. 7, where R_b is the back resistance of the X_1 crystals and n is the number of "OR" inputs at the point P_1. It should be noted that in pyramids where regeneration is employed n is never less than 2. The magnitude of the voltage e_2 is determined by considerations similar to those in the earlier circuits. The values for R_2 and E_2 may be determined from this expression for the rise time of the circuit of Fig. 7:

$$t_r = \frac{C_1 + C_2}{G_1 + G_2} \ln \frac{E_2G_2 + e_2G_1 - V_0(G_1 + G_2)}{E_2G_2 + e_2G_1 - V_p(G_1 + G_2)}, \qquad (6)$$

where

$$G_2 = \frac{1}{R_2}, \quad G_1 = \frac{n-1}{R_b} + \frac{n-2}{n-1}\,\frac{1}{R_1'}.$$

It now remains to choose R_3 and E_3 since the voltage e_3 is determined by considerations similar to those presented in Section II. It is important to note that since for clock pulse inputs the crystals X_5 and X_4 and the resistor R_3 are now eliminated, for the word inputs the resistor R_3 and the voltage E_3 may be determined for a greater fall time, namely, the time between clock pulses.

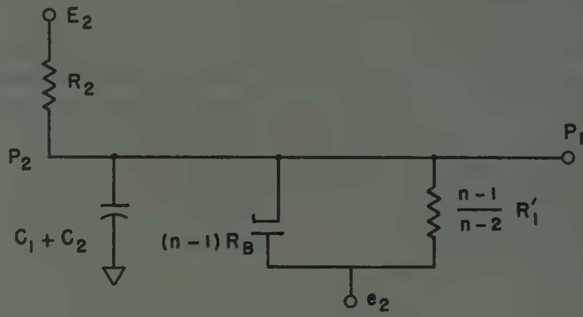


Fig. 7—Circuit to determine new R_2.

Consequently, R_3 and E_3 are determined only by the first criterion mentioned in Section II, namely, the clamping diode X_4 must never be quiescently in a nonconducting condition. It follows that

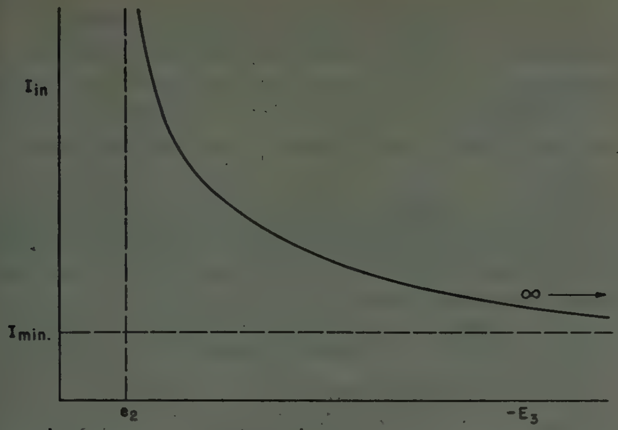
$$0 = \frac{1}{R_3}(E_3 - e_2) + \frac{1}{R_2}(E_2 - e) + (n-1)I_b + (e_1 - e_2)\frac{1}{R_1}, \qquad (7)$$

where n is the number of "AND" inputs at the point P_2 and I_b is the back current flowing through the X_3 crystals during the pulsing condition. If one establishes a value for E_3 then R_3 can be simply determined from (7).

The values for E_3 may be determined from this expression for the input current required during the time of the application of a word pulse

$$I_{\text{in}} = \frac{(e_p - e_f + e_3 - E_3)\left[\frac{1}{R_2}(E_2 - e_2) + (n-1)I_b + (e_1 - e_2)\frac{1}{R_1}\right]}{(e_2 - E_3)}, \qquad (8)$$

where e_p is the amplitude of the input pulse above the level of the voltage e_3 and e_f is the forward voltage drop in the X_5 crystal. The variation of I_{in} as a function of E_3 is shown in Fig. 8. From this figure, I_{in} may be selected to be the smallest value possible compatible with the problem of power supply design and power consumption.



$$I_{min.} = \frac{1}{R_2}(E_2-e_2)+(n-1)I_B+(e_1-e_2)\frac{1}{R_1}$$

Fig. 8—Input current vs. return voltage.

A comparison of the modified circuit with the original circuit is indicated in Fig. 9, and the alteration of MSAC resistance and voltage values is shown in the second column of Table I. Laboratory tests verified that both rise and fall times were at least maintained at 0.1 μsec or perhaps decreased about 10 per cent.

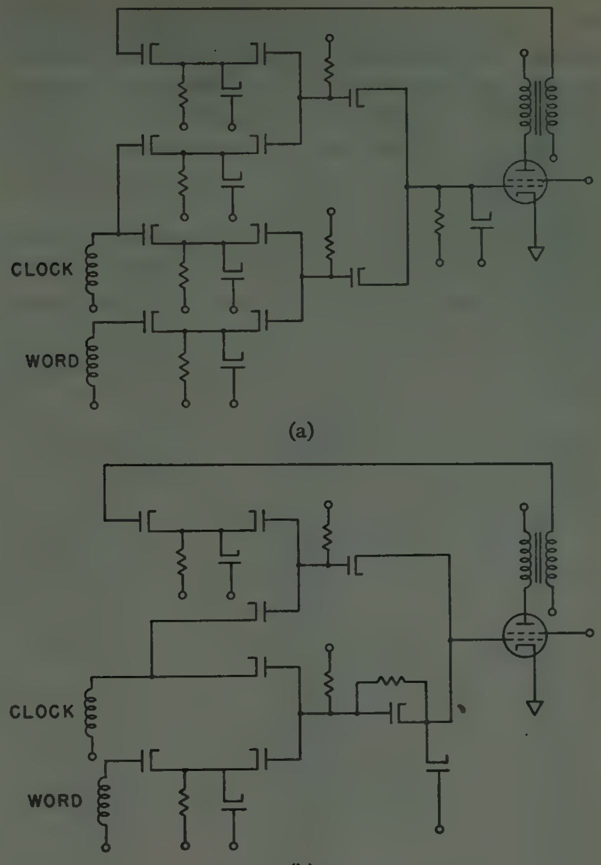
When logical "OR-AND-OR" pyramids are designed by these new techniques, six important advantages can in general be realized:

a. Fewer diodes are needed.
b. The largest voltages needed may be reduced by factors of as much as 2.
c. The power needed in the pyramid proper may be reduced by at least a factor of 2. As a direct result the physical sizes of the resistors may be reduced.
d. The resulting rise and fall times are speeded up by an appreciable factor, thus increasing circuit reliability.
e. Increased impedance levels at various pyramid inputs (in some cases by a factor of 2) may make it possible for a pulse power amplifier to drive more circuits.
f. The clock pulse power needed to drive any input may be reduced by at least a factor of 2.

IV. REDUCED CIRCUITS

Existing crystal diodes switch in approximately 1 v, from 100 k or higher at $-\frac{1}{2}$ v to 1 k or less at $+\frac{1}{2}$ v. It would be expected then that the pulse amplitudes used in diode switching circuits would be of the order of 3 to 5 v. Nevertheless most computer diode circuits use pulses of 20 v or more. For example, MSAC pulses are nominally 31 v.

Blame for these oversized pulses is usually placed on vacuum tube characteristics. Amplification is essential to diode gating since the latter is inherently degenerative of both power and waveform. It is of interest to inquire what characteristics are demanded of tubes.



(a)

(b)

Fig. 9—Comparison of original and new circuits. (a) Original circuit. (b) New circuit.

If low voltage pulses are to be effective, a primary requirement is that the grid cut-off bias, G, be as small as possible. This implies, in a pentode, low screen voltage. In order to develop large output power, either large plate supply voltage, E_{bb}, must be provided or the zero-bias plate current, I, must be high, or both. For rapid switching (short rise and fall times) tube capacitances, C, must be small; also, plate supply voltage must be low. The latter condition results from the three-fold consideration (a) that the pulse amplitude approximates E_{bb}, (b) the rate of pulse change is limited by the ratio I/C, and (c) the rise time is longer than the ratio of these two, namely, $E_{bb}C/I$.

Clearly, compromises must be made since small G results in small I, and E_{bb} must be both large and small. In the past it has been the practice to concede G in an effort to obtain large I, taking advantage of the three-halves power relationship of I vs screen and grid voltages. It is now to be demonstrated that this concession is unnecessary and, in fact, a disadvantage.

Let us examine the effect of a 5-fold reduction of all voltages in either the original MSAC diode circuit or preferably in its modification, as displayed in Table I. The most immediate result is a five-fold reduction in all currents, with consequent savings in power supply requirements and hence in components. Moreover the power dissipation decreases by a factor of 25; the largest

MSAC multiple input cascade (125 inputs) would then dissipate less than 1 watt. Clearly this allows the use of miniature resistors and subminiaturized packaging and consequently a substantial *decrease in wiring capacitance*. From the discussions in Sections II and III, it follows that R_1, R_2, and R_3 may be increased while maintaining the original rise times.

The decreased load on the pulse power amplifiers which results from increased R_3 is, of course, offset by the more than proportional loss in plate current, I. The latter would fall to about 40 per cent of its original (relative) value if the same tube type, the 6AG7, were employed. But the reduced power demands allow the use of smaller tubes, of which the subminiature 6AK5 (the CK5702WA) and the 6AH6 are examples. Both of the tubes may be biased (almost) to cut-off by setting $e_1 = -1$ v and by using appropriate screen voltage. The loss in current I for these tubes is in fact virtually negligible, particularly for the 6AH6. On the other hand there is a further substantial decrease in capacitance.

TABLE II

TYPICAL DESIGN FOR A PYRAMID USING 6V INPUT PULSES

Design Technique	Old	New
Tube	CK5702WA	CK5702WA
E_{bb}	+50	+50
E_{sc}	+35	+35
e_1	−1	−1
E_1	−14	None
E_1 or R_1'	39 k	6.2 k
E_2	+14	+7.5
R_2	13 k	15 k
e_2	−1.5	−1.5
E_3	−14	−7.5
R_3	5.6 k	5.6 k
e_3	−2	−2
Diode Type	IN96	IN96
Rise Time	0.1 μs	0.1 μs
Fall Time	0.1 μs	0.1 μs
Voltage Tolerance	±5%	±5%
Resistance Tolerance	±10%	±10%
C_1	15 μμf	15 μμf
C_2	10 μμf	10 μμf
C_3	10 μμf	10 μμf

Laboratory tests have been made using this 5-fold reduction in voltage. The various possible pyramid configurations have been studied experimentally under this mode of operation using both present day design techniques and the newly developed design techniques. A dynamic eight stage closed loop from a timer unit has also been studied under this mode of operation. In each case reliable operation with improvements in rise and fall time was achieved, thus bearing out the preceding analysis.

Typical parameter values are listed in Table II for pyramids employing these reduced design techniques. The values listed in this table are for the simple one word input pyramids.

V. CONCLUSIONS

This paper considered in detail present-day design techniques. Newly developed design techniques were then presented whose advantages were listed in Section III. The basis for choice of parameters for computer pyramids was briefly reviewed. Consideration of pulse voltage led to the suggestion of reduced pyramids, with substantial decrease in power dissipation, yet no deterioration in switching characteristics. For instance, using the new design techniques coupled with reduced pyramids, a 50-fold saving in power was achieved.

Since present-day trends in digital computers make it extremely desirable to reduce their size and power consumption it is suggested that more effort in the field should be devoted to the design and use of reduced pyramids using the new techniques. Incidentally, since all these circuits happen to provide current drive at the control grid, they are inherently adaptable to transistor pulse power application.

ACKNOWLEDGMENT

The work described here summarizes the efforts of the authors and numerous colleagues, especially Smil Ruhman, over an extended period of time. It was performed in connection with independent contracts placed by Signal Corps Engineering Laboratories, Fort Monmouth, N. J., and later by Special Devices Center, Office of Naval Research.

The authors are happy to acknowledge the advice of the group at the National Bureau of Standards who built the SEAC, to whom is owed the original philosophy of diode gating followed by pulse power amplifying tube, transformer coupling, and the "old" OR-AND-OR design technique.

* * *

A Survey of Digital Computer Memory Systems*

J. P. ECKERT, JR.†, ASSOCIATE, IRE

Summary—**Many types of storage and memory systems have been proposed for use in digital computing systems. This survey paper discusses only the various systems whose reaction time is faster than human reaction time, employing a historical approach to the subject. Criteria for evaluation are discussed, and comparisons given among the different systems as to general applicability, ease of construction and use, speed of operation, latency time, memory span, and economy.**

INTRODUCTION

THE HISTORY of the development of calculating devices includes in its scope the development of the many memory systems which have been considered, tested, used, held in abeyance, or discarded.

The concept of memory includes all forms of temporary and permanent storage of information for use in and by the computing device. A memory is a means for displacing in time various events which depend upon the same information. It is also a mediating device, a means for matching various speeds of operation to each other for the maximum efficiency of the computer components.

In the first instance the memory is much like the scratch pad used by a human being working a problem at a desk. It provides a place to put intermediate or auxiliary results, or to retain the original data of a problem. The center of concentration is focused on one calculation at a time. In the second instance storage facilities such as punched cards, magnetic tape, punched paper tape, and other media can be used for matching the high, internal operating speeds of the computer to the relatively slow speeds of an output printer, or of a a typist at some input device. The principal focus of this paper is the internal storage memory, the scratch pad of the computer data-processing circuits.

Upon looking into the systems which have been proposed for digital computers alone, one cannot help being struck by their wide variety and surprisingly large number. Many of these were, and may still be, impractical; yet there is no reason to believe that they must remain so, or that systems other than those already proposed may not be added to the list in the future.

Because there is such an abundance of examples, the better picture of the evolution of memories is probably given by a historical approach to the subject. Regardless of the approach, however, there are certain characteristics which inhere in any system of memory, and by means of which each may be evaluated.

One of the most important of these is the speed of operation, the rate at which reading-in and reading-out are accomplished. This is an especially important criterion in considering memories for high-speed computers.

The manner in which data are stored once inserted into the memory is another characteristic by means of which the various systems can be classified.

Additionally, speed of operation must be considered in terms of cost. The ratio is not a direct one: generally it is unwise to pay twice as much for doubling the speed. As a matter of fact, an increase of greater than twenty per cent in cost for doubling the speed of operation is usually considered unwise.

Furthermore, the balance of speed in all parts of a computer is important. It is foolish to have processing circuits—arithmetic circuits, and so forth—operating so fast that they must sit idle half the time waiting for other circuits to catch up. Thus the speed of a memory system will be strongly influenced by the cost of achieving that speed, and by the requirements of the other circuits.

To reduce the scope of this topic for the purposes of this paper, an arbitrary limit has been set on the speeds of the devices discussed so as to include only those systems whose access time or operation time is somewhat better than human reaction time. This lower limit ranges somewhere between one-tenth and one-thirtieth of a second; any slower device has been excluded.

EARLY DIGITAL MEMORIES

Predating the electronic computer are a number of familiar memory devices which should be considered before attacking more recent developments. The punched card, for example, is one of the most common memory devices for computing equipment. Before it, however, was the Jacquard loom system, wherein cards controlled the design being woven on the loom.

Co-existent with these was the mechanical assembly, usually called the accumulator, used in desk calculators and in tabulating equipment. The original design for mechanical accumulators dates back to Pascal and Leibnitz in the 17th century. Modern machines are refinements of those early ideas.

As far as electrical devices are concerned, relays and stepping switches have long held a prominent position as memory devices. A combination of electrical and mechanical components is used in the Lake Adder and Lake Storage units, which are a part of so much IBM equipment. In these units one finds a magnetic release followed by mechanical operation.

---

* Decimal classification: R621.385.2. Original manuscript received by the Institute, June 24, 1953; revised manuscript received August 4, 1953.

† Remington Rand, Inc., Philadelphia, Pa.

Among thermionic devices one of the earliest truly digital ones was the ring counter made with thyratrons by Wynne-Williams in England. The thyratrons were capable of firing rapidly, but tended to turn off slowly. This characteristic was tolerable in a ring circuit, since the slow die-out time was not a severe limitation as long as the next stage triggered rapidly. A development of Wynne-Williams' work was the cold cathode ring built out of OA4G's. The first such ring was built by Mauchly at Ursinus College some time in 1938.

The classical Eccles-Jordan trigger circuit, or flip-flop, another early device, was the first hard-tube counter. Its uses since its origin have been legion. At MIT, an efficient cascade of these trigger circuits was developed as a ring counter.

Since each stage of this type of circuit requires two tubes, a decimal-type counter involves twenty tubes—perhaps ten envelopes. With some improvements, this basic circuit was used in the ENIAC. The improvements included careful consideration of all the tolerances, and cathode-coupling the circuits so that no two stages could come on at one time.

Another counter called a Lewis ring was developed from the Eccles-Jordan circuits. In the Lewis ring a single tube was used for each stage, and each tube was connected through a resistor to every other tube in the circuit. Lewis also developed the bi-quinary counter, requiring only seven tubes (compared to the twenty of the Eccles-Jordan-MIT ring) for a count of ten. Although the bi-quinary Lewis counter was known at the the time of the construction of the ENIAC, it was not used because it required stable resistors, which were then much more expensive than they are now.

RCA, Remington Rand, and Bell Telephone Laboratories all have developed bi-quinary counters, the latter organization using relays. In the Lewis counter the quinary counter was stepped at each pulse, while the "bi" stage indicated whether the quinary was going through its first or second trip. The RCA bi-quinary system operated in the opposite way, with the "bi" stage stepped by each pulse. This is a better method since the binary counter, which has the simpler tolerance problems, is made the fast counter. In the Remington Rand 409-2 calculator, an ingenious method of pulsing both stages at the same time has been used.

A cascade of four binary counters or flip-flops provides another approach to the problem of a decimal counter. Potter at GE and Grossdoff at RCA both worked on this approach. The circuit is in wide use (in IBM 604 calculators, for example). There are probably more tube sockets now devoted to this type of circuit than to any developed thus far. This type of counter requires regenerative or jamming connections which force the sixteen possible states to become, in effect, only ten. An important step in the development of this system was regenerating or jamming at two different points in the ten-count, so that one counter stage would not be loaded with a regenerating connection to two other stages.

Probably the first example of what might generally be termed regenerative memory was developed earlier than 1942 by Atanasoff in Iowa. He used a drum with many capacitors mounted on it, and with a commutative method of connecting the capacitors with brushes for reading-in, reading-out and regenerating. The principal feature of the capacitor memory was the use of cheap, reusable elements. The capacitors could be charged, discharged and recharged as often as desired, and they were common and readily available components. The characteristics of small initial expense and almost unlimited reusability have guided the development of memory systems since, and remain two important criteria of the merit of any system at any time. There may have been similar systems prior to Atanasoff's but none was as inexpensive to construct. Unfortunately his development was interrupted by the war and never completed.

Another early reference to practical and relatively inexpensive large memory systems is given in a thesis written by Crawford at MIT in 1942. This thesis discussed certain fire-control computing apparatus in which the various functions representing firing table data were to be stored in the form of magnetic recording on discs. Out of this thesis grew the magnetic-drum and magnetic-disc memory system.

In 1944 the author submitted to the Moore School of Electrical Engineering at the University of Pennsylvania a memorandum which recommended the use of drums or discs for the general storage of all data required by a computer—not only the numbers being processed, but also instructions, functions required for the computation, timing channel signals, and so forth. This memorandum became the basis for the design of the EDVAC memory. The EDVAC design was subsequently switched from magnetic discs and drums to mercury tanks, principally for the reason that the mercury tank was a faster system at that time. Furthermore the engineers who worked on EDVAC were familiar with the use of mercury tanks, having previously developed a mercury-delay tank at the Moore School for some radar problems.

DELAY-LINE MEMORIES

The basic concept of a delay-line memory is simple: an information pattern is inserted into a path containing a delay element. From the end of the delay element the pattern may be fed back to the beginning through amplifying and timing circuits, thus forming a closed loop for recirculation. In simplest terms, a delay-line memory is equivalent to the short-range human device of repeating a phone number to oneself from the time it is located in the phone book until it has been dialed. The delay medium should slow the propagation rate of the information sufficiently that the physical size of the storage equipment for a large number of pulses will be within reason.

A large variety of media has been suggested for use in delay-line memories. Some of these transmit the information pattern acoustically, some electromagnetically. In the acoustic field mercury has probably received the widest use so far. The BINAC, built by the Eckert-Mauchly Computer Corporation for Northrop Aircraft, included a mercury tank memory of eighteen channels, each of which could hold thirty-two words of thirty-six bits each. Today the UNIVAC uses a similar mercury memory of a hundred channels, each of which holds ten 91-bit words. Both the BINAC and UNIVAC memories hold approximately 1,000 pulses per channel.

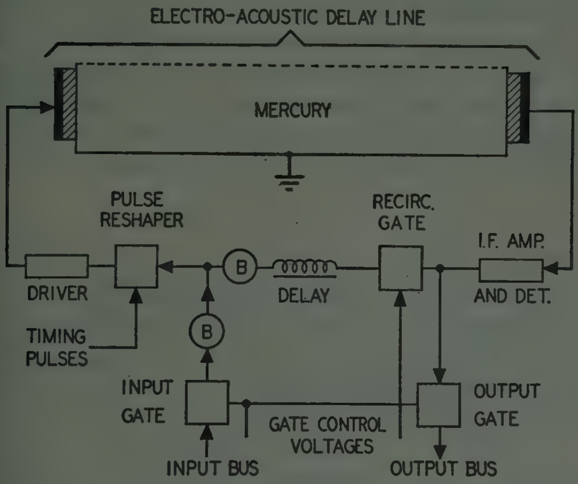


Fig. 1—Block diagram of UNIVAC acoustic memory.

The block diagram of the UNIVAC memory channel is given in Fig. 1. At each end of the mercury column is a transducing crystal, backed by a special metal alloy mounting piece is shaped and designed to absorb reflections. The loop is closed through the recirculation amplifier, which contains not only the amplifying, timing and reshaping circuits, but also the gates through which data are read out and in, and by means of which the tank is cleared entirely. Fig. 2 shows a complete tank with one of the eighteen recirculation chasses mounted on the shell.

The mercury tank requires rather precise temperature control since the velocity of an acoustic wave varies directly as the density of the propagating medium, which is a function of its temperature. The requirements are not so excessive as to have presented insurmountable problems, however.

One possible solution to the problem is to maintain no control of temperature, and to vary the master oscillator so that the delay through the tank is constant relative to frequency. On the other hand, an equally feasible solution is to use a crystal-controlled master-oscillator frequency as an absolute standard, and control the temperature to maintain a precise delay. The latter method has the advantage that electric delay lines can be used in the associated circuitry without additional compensation.

There are, in each of the seven mercury tanks in UNIVAC, a coarse and a fine temperature control. The coarse control operates from the expansion and contraction of the mercury. An expansion bellows at the end of the mercury column operates a microswitch, which applies power to a set of heating coils on a purely on-or-off basis. The signal for modulating the current through the heating coils of the fine temperature-control system comes from one of the eighteen memory channels specifically reserved for the purpose of controlling temperature. A standard signal circulates through this channel, and its time of arrival at the end of the delay line is compared with the timing of a control signal from the master oscillator. The results of this comparison adjust the heating-coil current.

Short mercury tanks are used in UNIVAC for the

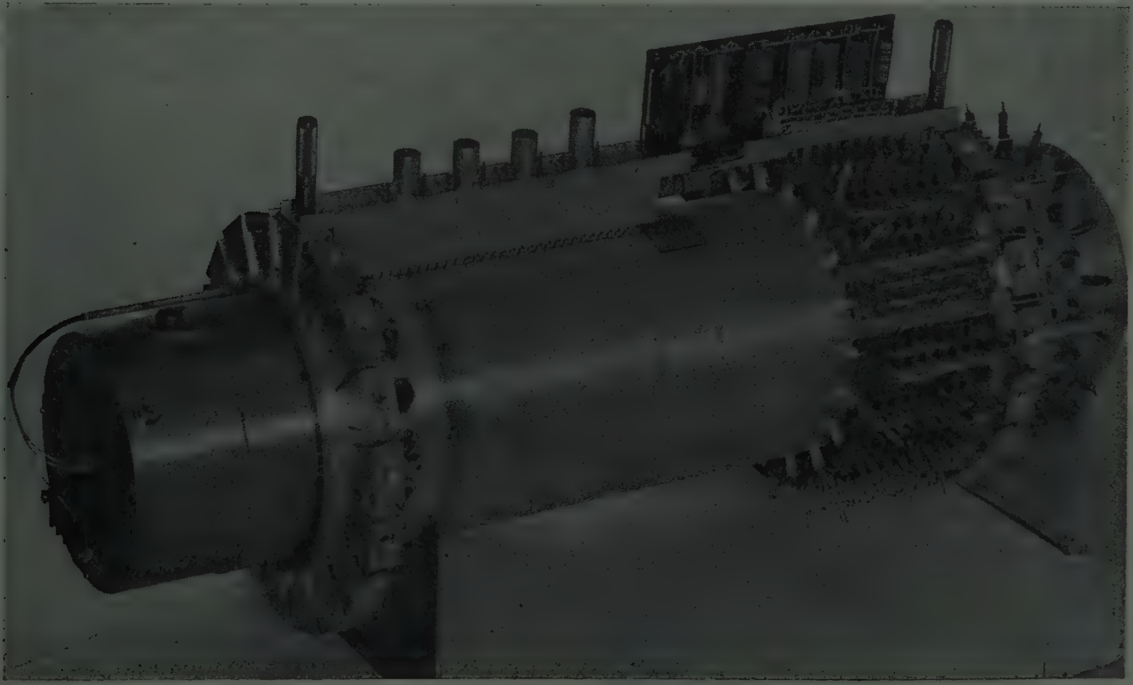


Fig. 2.—Photograph of mercury tank used in UNIVAC.

storage of 91 pulses (one word) in the small registers associated with the data-processing circuits. The same general design can also be used for the storage of two words, or half a word. In these small tanks the problem of temperature control is less severe, and a simple on-off control has been found adequate.

Other media have been proposed and tested for acoustic propagation systems. Quartz was tested at MIT and was used by the Japanese during World War II. The Japanese used a special powdered-glass coating on the outer surface of the quartz to suppress certain undesirable modes of wave transmission. Magnesium bell-metal was used by the Raytheon Corporation, while steel, lead and glass were tried at the Moore School. MIT also experimented with glass. The Naval Research Laboratories have worked with thin steel rods wound in a helix with transducing crystals at each end. The crystals are without backing, and the lines are only useful to a fraction of a megacycle.

The choice of media for the UNIVAC memory fell heavily in favor of mercury. It is a stable liquid which can readily be matched to transducers such as quartz crystals; being a liquid, it will not support any waves except longitudinal-compression and surface waves, and the latter are suppressed when the mercury is enclosed in a tank; it has uniform characteristics achieved through careful distillation, and it has no localized strains to cause spurious patterns. Solids generally support shear waves, and usually present problems in coupling to suitable transducers.

Another type of delay line is one in which essentially acoustic patterns are propagated through a medium as a result of either magnetostrictive or piezoelectric effects. The Hazeltine Electronics Corporation first developed a nickel-ribbon magnetostriction system, and later a method using nickel wire. Elliott Brothers in England have also worked on nickel wire. Fig. 3 shows a magnetostrictive memory using ferrite as a medium. The read-in coil, when pulsed, produces a longitudinal-compression wave in the ferrite. This wave travels down the line and induces a current in the read-out coil. This current can be detected and put through a regenerating circuit to make a continuous loop.

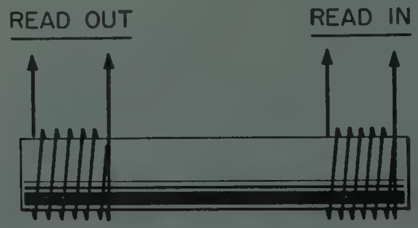


Fig. 3—Magnetostrictive delay line.

In the piezoelectric delay line illustrated in Fig. 4 a pair of conducting plates are supplied with a voltage pulse which produces a double-shear wave in the piezoelectric material. This wave travels along the line to the output plates where a voltage pulse is generated.

A third form of dynamic storage, which has seen wide acceptance, is the electric delay line. There are two types of these: distributed parameter and lumped-parameter lines. Fig. 5 is a photograph of a lumped-parameter line.

Both types of lines were thought of by Pupin sometime in the late 19th century. More recently, MIT and Bell Labs worked with distributed-parameter lines with lumped-parameter phase correction networks at the end. Kallman, at MIT, worked with distributed-parameter lines, placing semi-lumped phase correctors consisting of tinfoil at uniform intervals along the line. Experiments performed at the Moore School by the author produced some distributed-parameter lines with metal-ribbon phase correction windings. Maximum surface-to-surface apposition of the metal ribbon resulted in large interwinding capacitance. Double-layer wire windings were used, with the same aim.

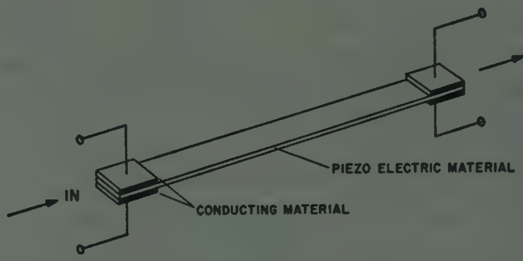


Fig. 4—Piezoelectric delay line.

The General Electric Company developed a system in which the line was sprayed with aluminum paint to provide continuous phase correction. A distributed-parameter delay line made by Millen is used by the Bureau of Standards in the SEAC. At frequencies under a megacycle such a line is economically useful with proper circuits up to about eight pulses. The continuous-parameter line tends to become comparatively less efficient than the lumped-parameter line for more than eight or so pulses. Neither type is as efficient spacewise as the acoustic line since each type requires greater space for a given amount of memory, and both electri types are expensive except for a small number of pulses Wherever lumped-parameter lines are used in UNIVAC the signal is regenerated after every seven-pulse dela

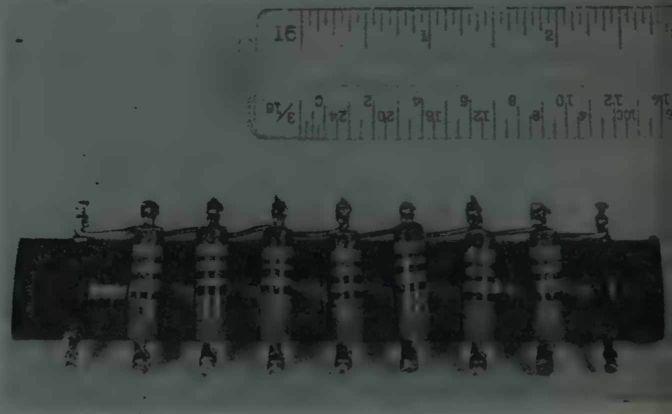


Fig. 5—Photograph of a lumped-parameter delay line.

(although thirty pulses were stored in an electric delay line with only one regeneration station in the BINAC). Electric lines cause comparatively large signal attenuation in any event, but lose almost nothing in the input or output coupling; signals passing through acoustic lines, on the other hand, suffer little attenuation in the medium, but are severely attenuated in the transducers at each end.

The use of any delay-line memory usually makes time-sharing of the recirculation circuits impractical. Other disadvantages of the delay line are the awkward amount of access time (the maximum access time being the length of the delay) and the amount of terminal equipment involved. Making longer channels amortizes the terminal equipment over more memory, but increases the access time and presents a greater problem in temperature control.

ELECTROSTATIC SYSTEMS

Under the general heading of electrostatic memory systems are many different examples, some of which differ only slightly from others. Basically there are four types, referred to as the surface-redistribution, holding-beam, barrier-grid and sticking-potential types. The surface-redistribution type is sometimes called the interfering-periphery type.

Although the basic phenomenon of electrostatic storage was illustrated in the earliest iconoscopes, such a recording was continuous in nature. Some of the first experiments with the electrostatic principles aimed directly at the digital problem were inducted at the Moore School by Sharpless and the author. Prior to this Connell at MIT did some work recording radar signals. Other early experiments with this type of system were performed by Forbes at MIT and Williams in England. The latter system has been quite widely and successfully used in various digital computers.

There are some characteristics of electrostatic systems, and criteria for their evaluation, which differ markedly from the characteristics of delay line. The retentivity ratio—the ratio of the retention time to the read-write time—is one of these. In a delay line the two are identical, and the ratio is one. A complete cycle of the delay line is required for reading in or out; this is also the retention span of the line. (Obviously a system with a ratio less than one is unfeasible, since the read-in or read-out time exceeds the memory span, and the second cycling would override part of the first.) The retention time is usually larger than necessary in an electrostatic storage tube.

Another important characteristic of electrostatic systems is the redistribution, or "read-around" time. This is the maximum time during which a spot may be read without destroying the spots in the vicinity. This characteristic determines when the adjacent spots must be regenerated in terms of the total time the reading beam has spent on a selected spot. The ratio of read-write time to redistribution time is an excellent indication of the requirements of the regeneration system. For example, with redistribution time measured in milliseconds and read-write time measured in microseconds, this ratio would be on the order of 10^3. If, in such a circumstance, there were 10^3 spots on a tube, then regardless of the absolute rate, regeneration should occupy half of the time, allowing reading and writing to occur during the other half. Improvements in the redistribution characteristic could improve this situation, by permitting either less frequent regeneration or increased spot densities.

Surface Redistribution System

An interfering-periphery, or surface-redistribution, storage system developed at the Eckert-Mauchly Laboratories is similar in concept to most of this type of store. It will be used as a model in this discussion.

Most such storage systems depend on the secondary-emission phenomenon. Fig. 6 shows the relationship of primary and secondary emission as voltage increases. The region wherein the secondary emission exceeds the primary is the important area of this graph. When this ratio exceeds one, the potential of the spot on the screen goes positive.

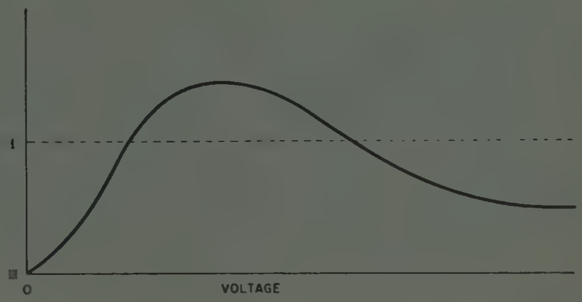


Fig. 6—Ratio of primary to secondary electrons versus voltage.

This alone, however, is not enough to allow storage of the binary digits or two-level signals required by the usual digital computers. In order to achieve two-level storage two different patterns must be stored on the face of the tube, one of which is used as a reading pattern. If the reading pattern is the same as the stored pattern, there will be little change in the charge on the face of the tube when reading occurs. If the reading pattern is different, the stored pattern will be destroyed and changed to the reading pattern. It is this change from one pattern to another which produces a total change of charge on the face of the tube. A fine wire mesh may be placed over the outside face of the tube to detect this change by capacitor action.

Numerous charge patterns have been devised and tested, some of which are illustrated in Fig. 7. It is desirable to choose two patterns whose peripheral interference is large. Our experiments have been concerned mostly with the dot-circle and focus-defocus patterns shown on lines *D* and *C* of the illustrations. More widely used, however, is the dot-line (or dot-dash) of line *A* and an adjacent-dot system similar to line *F*. The original dot-line system was developed by Williams in

England.[1] The signals at the right of Fig. 7 are suggestive in shape only of the typical output signals obtained when the smaller-periphery shapes are read by superimposing the larger patterns.

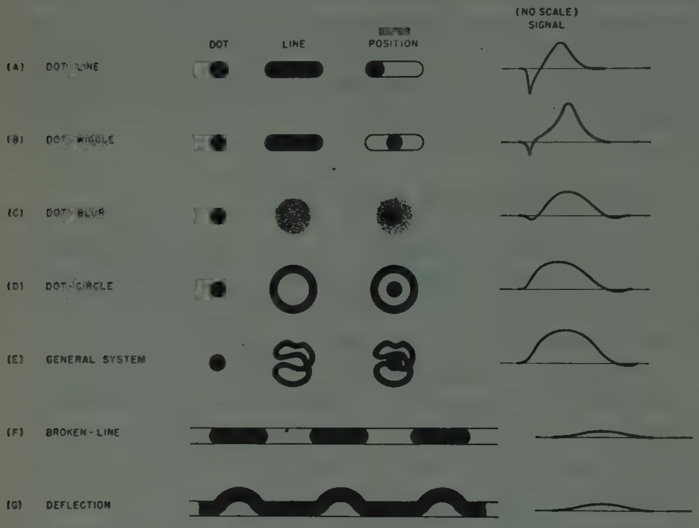


Fig. 7—Electrostatic storage patterns.

The block diagram of the surface-redistribution system is given in Fig. 8. The blanking circuit cuts off the beam while the deflection circuits are assuming the correct potentials for the chosen spot. The circle generator is gated in and out of the circuit, depending on the pattern desired. The wire mesh over the face of the tube is shown connected to an amplifier. The amplifier output is shaped and fed to a switching circuit, which is controlled from the computer's sequencing and control circuits.

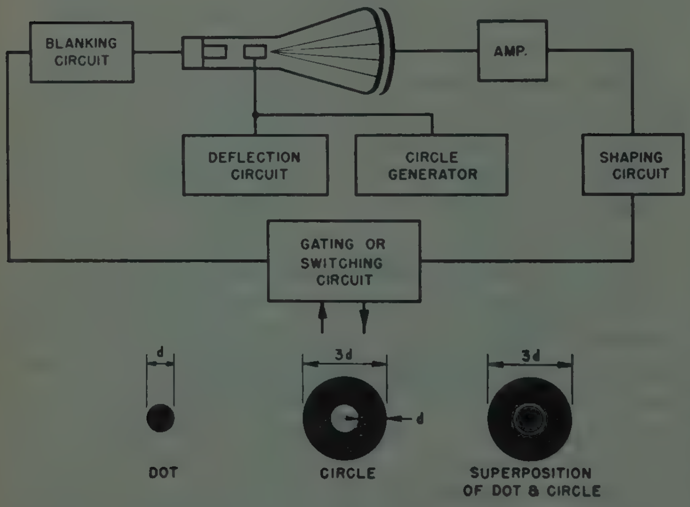


Fig. 8—Block diagram of electrostatic [circle-dot] storage.

In this system the circle is always used as the reading pattern. If a circle has been previously stored in a given area, and a circle superimposed on it for reading, there will be no appreciable output signal. If, however, a dot has been stored, the circle will destroy the dot and in so doing develop a significant output pulse. Typical dimensional relation of dot and circle, giving reasonable peripheral interference, is shown in the lower part of Fig. 8.

The operation of such a tube within a computer depends on the systematic interlacing of the regeneration operation and the reading and writing operations. During one part of each memory cycle, one spot is regenerated, first being read off the screen and then being replaced through the recirculation loop. The second part of the cycle can then be used as required by the computer for reading or writing. When a spot is read for transferal to the data-processing circuits, no significant information is left on the face of the tube. In the write operation the previous pattern is of no importance, since the new pattern will override and destroy the old in any event.

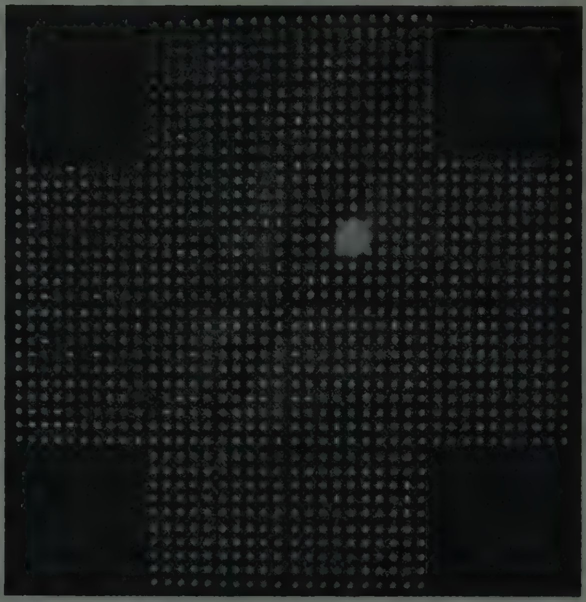


Fig. 9—Photograph of face of electrostatic storage tube.

Fig. 9 shows the face of an electrostatic storage tube with the pattern of dots and circles. At the time the photograph was made the same spot was being read each cycle, while every other spot was being regenerated in sequential order during successive cycles. Since there are 1,200 separate spots on the tube, the one selected spot in this worst of all possible conditions is being read 1,201 times to only once for each other spot; hence it appears as a much more intense image than the others.

Barrier-Grid System

Another electrostatic storage system, operating in a manner similar to the surface-redistribution type, is the barrier-grid type. An example of this is the Radicon tube produced by RCA and intended for use as a digital storage tube. A cross-section of this type of memory is shown in Fig. 10.

---

[1] Comparison and discussion of these systems, as well as Fig. 7, appear in Eckert, J. P., Jr., H. Lukoff, and G. Smoliar, "A dynamically regenerated electrostatic storage system," Proc. I.R.E., vol. 38, pp. 498–510; May, 1950.

The capacitance between the inside surface of the insulating plate and the conducting back plate reacts as many elementary capacitors. In operation each of these elementary capacitors is charged by the beam through the barrier-grid to a potential determined by the potential at which the input conducting plate is held. The deflection means may be any one of the familiar types. The purpose of the barrier grid is to reduce the number of secondary electrons which would otherwise fall back on the surrounding area of the tube face. Because of the grid mesh most of the secondaries are directed toward the output collector plate; what few do fall back land near the spot made by the beam.

A variation of this system is the Krawinkel tube, which is really a barrier-grid system without a barrier grid. In both systems the potential on the plate in front of the tube determines the potential stored during the writing process; this is the essential difference between these two and the redistribution system. In the reading operation the beam is directed at the proper spot while a standard reading potential is maintained on the plate behind the storing surface. If the stored potential differs from the reading potential, current will flow in the input or output resistor, and from there can be read to other circuits.

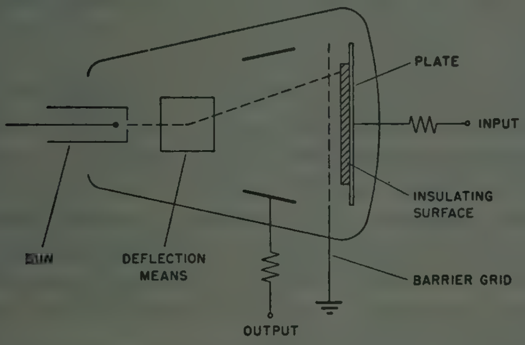


Fig. 10—Barrier-grid memory.

Holding-Beam Systems

A third type of electrostatic storage is commonly called the holding-beam system. In this type of memory, developed by Haeff and others, areas on the inside face of the tube are charged to one of two levels. Long-term memory of either of these levels is accomplished by spraying the entire target area with a defocused beam from a separate holding gun.

Fig. 11 illustrates the holding-beam method. The cathode potential of the holding gun is established at such a value that the equilibrium of all points on the target will be maintained, regardless of whether they are charged to the higher or lower potential. For example, if the collector is grounded, and the holding gun cathode potential is −75 volts, the writing gun could have a potential of −40 volts. Under these conditions, the entire face of the tube is set initially at the collector potential. The action of the writing beam combined with that of the holding beam would shift the potential of the selected area to that of the holding-beam cathode. (The choice of potentials depends on the target material.) The various areas of the target, therefore, would be at either collector or holding-gun potential.

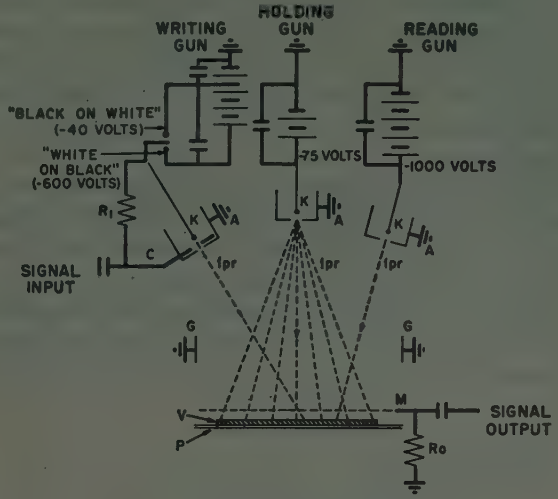


Fig. 11—Holding-beam memory tube.

To read the information it is necessary to scan the selected area with a reading beam whose cathode is so much more negative that the secondary emission ratio is greater than one. If an area is nearly at collector potential, the collector grid placed between the target and the guns will receive a capacitor discharge current of a given magnitude. If an area is at holding-gun potential, the action of the reading beam produces a capacitor discharge of greater magnitude.

A single gun can be used for both reading and writing provided that the potential of its cathode is shifted from one value to the other for the two operations. One advantage of using separate guns, however, is that writing and reading may take place simultaneously, provided that the output currents caused by the writing operation can be separated from those generated by the reading action. One method of achieving this is modulating the reading beam with a high-frequency alternating signal, and separating the signals in the output with IF and detector circuits.

Erasure of all information means bringing the entire target area to a common potential. This can be accomplished by raising the holding-gun cathode potential to −40 volts and then flooding the tube face with the holding beam.

The holding-beam system requires a specially constructed tube. An additional disadvantage is that adjacent areas charged to different potentials may bleed into each other if left under the influence of the holding beam alone for long periods of time. The spillover can be overcome by constructing the tube face in the form of a mosaic, in which the elementary areas are of nonconducting material and the mosaic itself is of conducting material. With such a construction the system is quite stable, and external regeneration is not required. Furthermore, the information is not destroyed on read out.

The holding-beam type of memory, like the interfering periphery and barrier-grid types, possesses an inherent parallelism in that a common deflecting circuit can position the reading or writing beams in several tubes at a time, each of which can deliver one binary component of an element of data. For a given output rate this reduces the response requirements of the deflecting system.

The selectron is a specialized tube operating on the principles of a holding-beam tube and built as a digital data store. The geometry of the electrodes is the most important factor in the construction of the tube, due to the fact that the lattice-like arrangement of selecting bars entirely controls the registering of the data and its subsequent readout.

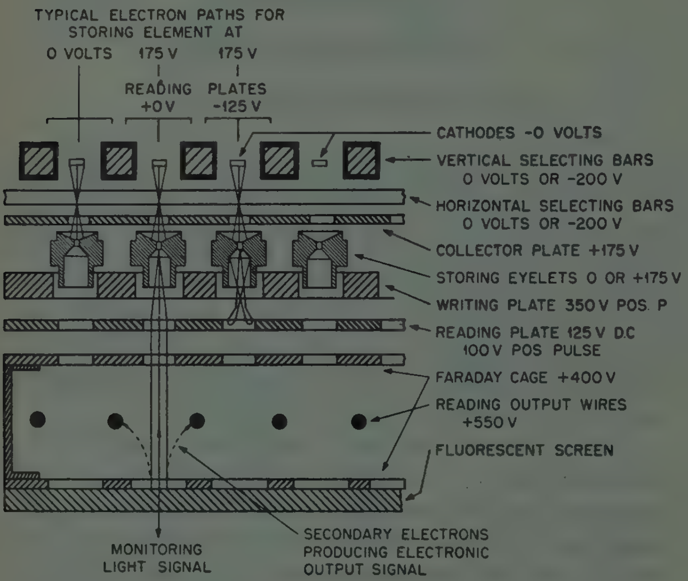

TYPICAL ELECTRON PATHS FOR STORING ELEMENT AT
0 VOLTS
175 V
175 V
READING +0 V
PLATES -125 V
CATHODES -0 VOLTS
VERTICAL SELECTING BARS 0 VOLTS OR -200 V
HORIZONTAL SELECTING BARS 0 VOLTS OR -200 V
COLLECTOR PLATE +175 V
STORING EYELETS 0 OR +175 V
WRITING PLATE 350 V POS. P
READING PLATE 125 V D.C 100 V POS PULSE
FARADAY CAGE +400 V
READING OUTPUT WIRES +550 V
FLUORESCENT SCREEN
MONITORING LIGHT SIGNAL
SECONDARY ELECTRONS PRODUCING ELECTRONIC OUTPUT SIGNAL

Fig. 12—Selectron.

The geometry of the elements is shown in Fig. 12. The actual storage elements are the metallic eyelets near the top of the drawing, which are insulated from all surrounding construction. The cathodes continuously emit electrons toward the storing eyelets, just as the holding gun does. There is a small hole in the center of each eyelet. The beam is focused on the eyelets by the horizontal and vertical selector bars and through the collector plate. The selector bars permit precise selection of any eyelet.

The eyelets can sit at either of two stable potentials, one slightly below cathode potential (which is near ground) and the other slightly below collector potential. The current-voltage characteristic of the storing element has an unstable cross-over point between these two extremes. If all the selector bars but one horizontal and one vertical are pulsed negatively at the same time, only one square or gate will remain at the bias cathode potential. All others will be driven to the more negative collector potential. In this fashion a selective gating arrangement is obtained for either reading or writing.

Reading and writing can be done only after the selection has been made. In the write operation the writing plate is pulsed positively as the selector bars reach their maximum negative potential. The writing plate is capacitively coupled to each of the storage elements. If the element is at collector potential, it will be raised to nearly twice this potential by the writing pulse. If it is originally at cathode potential, the pulse on the writing plate will bring it nearly to collector potential. Either positive or negative registry of the information may be made. If positive registry is desired, the writing pulse is made to decay slowly enough to keep the displacement current to the element small. For negative registry, the writing pulse is kept at its maximum value long enough for the primary electrons to bring back to the collector potential those elements whose potential was doubled. The writing pulse then drops sharply; the resulting negative displacement of current overrides the holding current, and brings the storage element to cathode potential, where it remains locked.

Erasure as a separate operation is not necessary. Regardless of the previous condition, the act of writing will bring the element to either of the possible levels. It is the pulse applied to the writing plate which determines which of the two levels is to be stored in the eyelet.

The hole in the center of the eyelet is used for reading. Some of the electrons focused on the eyelet from the cathode pass through this 0.02-inch hole to the reading assembly. When an eyelet is positive, that is, near the collector potential, the beam passes through the hole by virtue of its own inertia. When the eyelet is near cathode potential, however, it exercises gate action, repelling the beam and preventing it from passing through the storage element.

The presence or absence of the beam on the lower side of the eyelet determines the potential state of the eyelet. The selector bars pick out whichever eyelet is to be read. A positive pulse then applied to the reading plate allows any current through the selected element to proceed through to the output electrodes. If a beam passes into the Faraday cage, it strikes a coating on the plate on the other side. The secondary emissions which result are collected by the output wires and read to the external circuitry.

Except for its complex constructional details, and its cost, there is much to recommend the selectron as a memory system: It does not require regeneration; the access time is reasonable; there is no destruction on readout; the locating system does not drift since it is mechanical in character and fixed in relation to the storage element; and there is no resolution problem since the storage elements are isolated one from another. Somewhat like other electrostatic systems, the selectron is not subject to loss of memory in the event of a short power failure. A long power failure, however, will cause loss of memory.

Sticking-Potential System

The fourth variety of electrostatic storage utilizes the sticking potential of the material on the tube face. The face material will not allow more than a certain potential-difference to exist between it and the gun. This is the potential at which the secondary emission ratio becomes one again at the high-potential end.

If the sticking potential is (for the sake of discussion) 10,000 volts, then setting the gun potential at −11,000 volts will cause the area under the beam to be charged to 1,000 volts. If the gun potential is made to be −12,000 volts, the area will assume a charge of 2,000 volts. It is possible to operate the system using more than two stable states if that is desired. Reading can be done by holding both the gun and the target plate at a standard potential while observing the current through a resistor connecting the target plate to the external circuits.

The principal disadvantage of this type of memory is that none of the currently available face materials exhibits a sufficiently stable or uniform sticking potential for reliable operation. This, of course, does not gainsay the possibility that a reliable material may be found and the system may become a practical one.

The main advantages of all electrostatic memory and storage systems are the low latency time, which is a microsecond or less per binary digit, and the economy of being able to share regeneration circuits and deflection circuits among tubes. The characteristic of destruction on read-out, although it could be avoided by using smaller reading current, is not too damaging anyway. Computer applications frequently require that the inspected area be cleared; furthermore, the facilities for reading in are available for fuller use in recirculating the read-out data back into the memory.

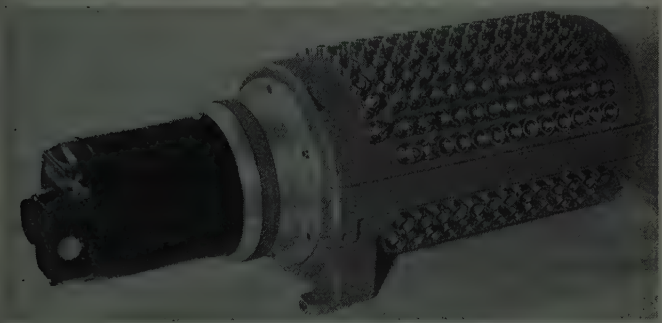


Fig. 13—Photograph of an ERA magnetic drum.

MAGNETIC DRUMS

Another storage system for digital computers is the magnetic drum. Engineering Research Associates have pioneered in the construction of practical magnetic-drum memories. A photograph of one of these drums is shown in Fig. 13. Many different examples have been built since then and are in wide use in many presently operating computing systems.

In this system, illustrated in Fig. 14, a cylindrical surface treated with a magnetically-sensitive material is rotated at a fixed speed under a row of heads. These heads, which are usually staggered around the drum, can serve for both reading and recording. External switching circuits select the proper head and the specific operation. The information stored takes the form of magnetized regions on the surface of the drum.

The schemes for writing on the drum can be either in a return-to-zero or a non-return-to-zero system. Manchester's computer in England uses a non-return-to-zero system which avoids a dc component yet produces a pulse for each bit by virtue of a probing pulse system. The return-to-zero method, used more commonly, can either pulse positively from a zero reference level for a one and pulse negatively for a zero, or it can use one polarity continuously for zero and pulse fully positive for ones.

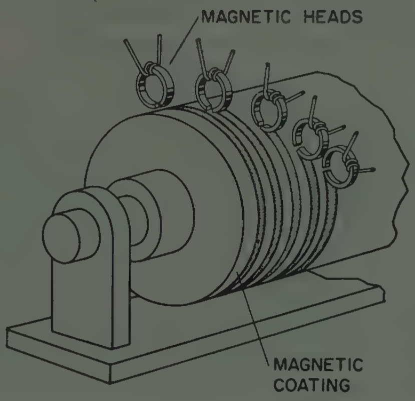


Fig. 14—The magnetic-drum system.

In some of the earlier schemes for magnetic drums a writing amplifier was supplied for each head, unless the speed of the system was sufficiently slow as to tolerate relay operating speeds. Circuits are now appearing which allow "power switching" at electronic speeds, allowing a few writing amplifiers to be time-shared by a large number of writing heads via high-speed switching circuits.

The timing problem—the problem of determining where on the cylinder a particular piece of information is located—is akin to the similar problem in a mercury-tank memory. Instead of depending on temperature, however, it depends on the speed of rotation of the drum. The resolution problem includes such factors as the spacing of the heads so that cross-talk is eliminated; the pulse densities used; and the accuracy with which the drum can be machined. This last aspect is critical because of the variations in signal strength which are caused by a change in distance between the head and the recording medium. If the drum has any sizeable variations in diameter, the variations in output signal may become intolerable. With fixed heads such as the illustration shows, the principal requirement is that the drum be circular under any head; the actual diameter of the drum may vary slightly from one end to the other. This variation may be compensated for in the initial setting of the heads.

One would at first think that currently achievable rates of rotation would make for long latency time compared, for example, to the latency time of a mercury tank. However, by means of interlacing and minimum latency coding much can be done to improve this situation. Further improvements are possible with increased drum speeds. Laboratory models have been operated in excess of 75,000 rpm.

The magnetic drum does not have a limited memory span and will retain its information if the power fails. The locating system does not drift, since it is fixed by the geometry of the head placement. Read-out does not destroy the record, and there is no regeneration problem. Since the drum has proven to be an inexpensive device per bit of information, the development of minimum latency and interlacing techniques and of higher-speed drive systems places it in the foreground as a contender of some importance in the computer field.

OTHER SYSTEMS

In any rapidly developing field there is a natural tendency to make the best use of those systems which appear the most likely to respond successfully to a given amount of engineering research. Once these avenues have been traveled and the immediate needs are satisfied, time can be taken to evaluate and experiment with other, initially less promising, systems. Moreover, experience provides an additional criterion with which to evaluate other ideas.

Magnetic Cells

Of the more speculative and experimental memory systems, the most promising are those utilizing materials whose magnetic properties are characterized by square hystersis loops. Work on magnetic cells was done at the Moore School in 1945 by Chu and the author.

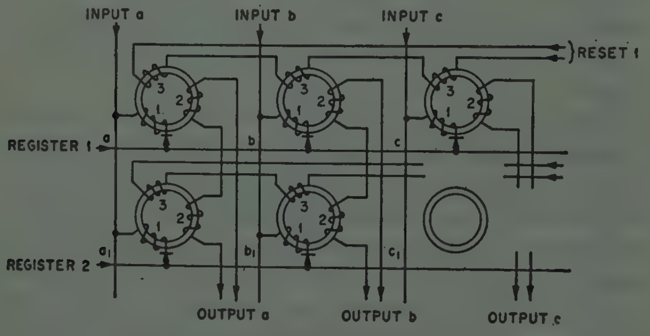


Fig. 15—Magnetic cell with diode.

Fig. 15 illustrates an early magnetic-cell system which used diodes. The magnetic material used here did not have the square hystersis characteristic now demanded for similar systems. The square characteristic enables the cell to perform both memory and selection functions; in the illustrated system, the diode performs the selection while only the memory function inheres in the material. In the horizontal direction of this array are registers one, two, and so forth. Vertically there are inputs *a*, *b*, *c*. For reading into the memory, the input lines are energized with the voltage levels representing the digit to be stored, and the selected register line is pulsed. This causes current to flow through the write coil (marked 1) and the diode. Reading-out of a register is accomplished by pulsing the reset line. This clears all the cells to the standard polarity of magnetization, and causes current to flow in the outputs of those cells which had previously been set at other than standard polarity.

Experimentation has recently been focused on materials having a more nearly square hysteresis characteristic. Fig. 16 is a diagram of a memory cell which uses these materials. In this system, the cells are arrayed with a matrix of wires crossing the *X* and *Y* directions. Exciting an *X*-wire and a *Y*-wire with current in the same direction will cause the cell to which the two wires are common to flip from one polarity to the other. The current in a single wire is not sufficient to cause the cells to flip.

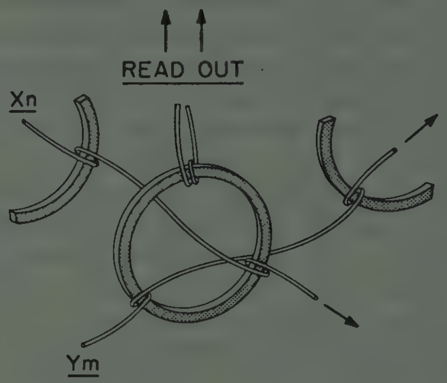


Fig. 16—Square-loop ferromagnetic cell.

The third coil in the drawing is the read-out coil, which listens for a magnetic shift in the core. In actual practice it may be possible to do away with the third coil if a current-sensitive device is attached to the two wires leading to the cell. This device could determine whether or not a coil had flipped by sensing the magnitude of the current in the line. These coincident current memories improve on the earlier type described above through use of rectangular hysteresis materials, and the elimination of the diode and soldered joints.

The magnetic-core "shifting register" type of memory, in which magnetic cores with square hysteresis characteristics are arrayed much as the elements of a lumped-parameter delay line, is a feasible type for small amounts of storage. Pulse trains can be read in and out either in series or in parallel. For serial operation diodes switch the pulses down the line as new pulses come in. The system is more expensive per bit of information than the magnetic-cell matrix type, but might be valuable in situations requiring both serial-to-parallel conversion and nonvolatility. The earliest version of this type memory operated at 25 kilocycles and was constructed at Harvard by An Wang and Way Dong Woo. Numerous laboratories have built examples since, working at higher frequencies up to 100 kilocycles.

Such magnetic systems are nonvolatile; there is no loss of memory on power failure. It requires little power for reading or writing, and none for regeneration. There is no resolution problem, nor any possibility of drift in the locating system. There is destruction on read-out, but this is not too serious, since most computers possess equipment for re-entering the data directly. Also, Buck of MIT is now speaking about nondestructive read-out for this type of memory.

Ferroelectric Cell

Operating on a somewhat similar principle is the ferroelectric cell, in which a ferroelectric material is sandwiched between two plates. The construction is similar to that of a capacitor. Unlike an ordinary dielectric, however, the ferroelectric material possesses a square, hysteresis-like characteristic, instead of a linear relationship of voltage and charge. This curve is identical with the curve for the magnetic phenomenon, but with D and E as variables instead of B and H. Once the voltage across the cell has been brought to a maximum and reduced to zero, a charge remains in the material. As the voltage across the cell is reduced to a negative maximum and brought back to zero, a similar charge of opposite polarity is left.

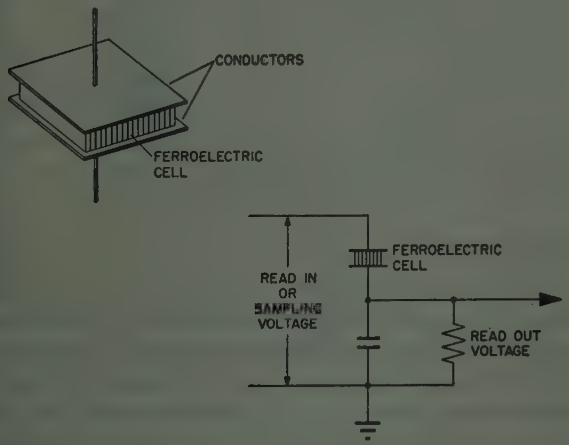


Fig. 17—Ferroelectric cell.

A typical circuit for reading a ferroelectric memory is shown in Fig. 17. If a pulse of the same polarity as that stored in the cell is applied across the circuit, there will be little current through the resistor and a negligible output signal. If, however, the applied pulse is of the opposite polarity a larger current will flow and develop an output signal across the resistor.

The ferroelectric cell memory requires adjustment of polarity and amplitude of voltage, instead of the adjustments effected on current in the magnetic cell system. The construction is also somewhat different, as shown in Fig. 18. Here a plate of ferroelectric material such as barium titanate is sandwiched between strips of conducting material. The arrangement of the sets of strips at right angles to each other results in a matrix of individual memory cells. To select a particular cell it is necessary only to energize an X-bar and a Y-bar in a manner similar to that employed in magnetic cell systems.

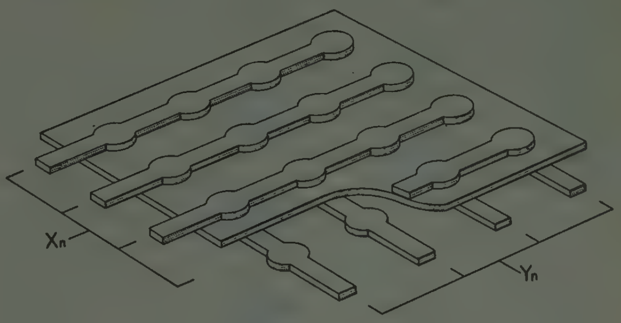


Fig. 18—Constructional detail of ferroelectric cell.

(In connection with the selection process in either ferroelectric or ferromagnetic cell memories, one should realize that there is a choice in the selection of the energizing voltages or currents. For example, the system could use a $+1$ value on one side of the matrix and a -1 value on the other. These could be applied to the selected line on each side, and all other lines kept at zero. No more than ± 1 is applied across any cell except the cell at the junction of the two lines. This cell, which is the "selected" cell, responds to a potential difference of 2. On the other hand, the normal for one side may be 0, and the energizing signal, 2; while $+1$ is applied as normal to the other side and -1 used for energizing the selected line. The junction of the $+1$ and -1 lines would then be the "selected" cell, while all other cells would have only a unit signal in one or the other direction—$+2$, $+1$, or 0, -1. This arrangement provides a 3:1 distinction between selected and nonselected cells, as compared with 2:1 in the first situation. The signals must be applied in the right order, however, with the $+1$ and -1 occurring first and the 2 signal afterward.)

The ferroelectric cell has a memory span as great as magnetic cells with similar hystersis characteristics. Most of the advantages and disadvantages of magnetic cells, as regards small-power requirements, resolution, lack of drift in selection and location, no regeneration, and destruction on read-out, also apply to the ferroelectric cell system.

Capacitor-Diode

A memory using capacitors as storage elements is feasible if capacitors could be developed which are capable of storing a charge sufficiently long. Fig. 19 shows a circuit developed by the Bureau of Standards and used by that agency in a number of experiments.

This capacitor-diode memory has no particular virtue as far as cost is concerned, since it requires two diodes and there are systems which require only one. The system requires regeneration to compensate for leakage over long periods of time within both capacitors and diodes.

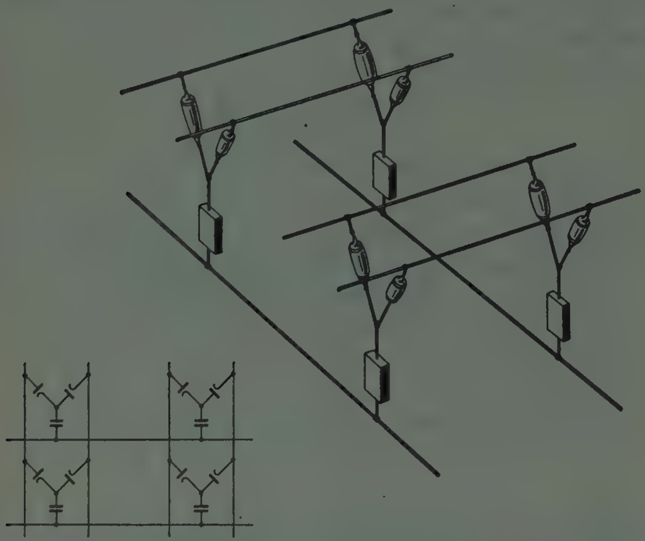


Fig. 19—Capacitor-diode memory.

Neon-Resistor

Another matrix-type system has been considered which uses neons and resistors in series at the junction points of the matrix. The principal requirement of such a system is that the firing potential of the neon must be well above the extinguishing potential. The system has a number of possible advantages, including that it would not be necessary to destroy on read-out: a small pulse put in on one co-ordinate of the matrix would appear on lines in the other co-ordinate only through the conducting neons.

Neon-Capacitor

Still another matrix-type system, conceived by Mauchly about 6 years ago, utilizes a capacitor and a neon bulb in series at each junction point. This system depends upon the capacitor to hold a charge for relatively long times, using the neon when not fired as a switching device. In operation the potential difference between the selected matrix lines would be increased until the neon fired. The neon will fire in a few microseconds and assume a low impedance; the capacitor is charged to a substantial voltage through the neon. As the potential between the lines is reduced, the neon is extinguished, becoming an extremely high impedance, and leaving a charge on the capacitor. To read from the memory, a smaller potential can be applied across the two lines in the opposite sense. If the capacitor is charged, the neon will fire and draw current, if the capacitor is not charged, the potential difference will not be enough to fire the neon. The destruction readout current is sensed and used as a means of detecting the condition of the memory after which any necessary regeneration takes place.

Phosphor Drums

A system utilizing drums coated with a phosphor has been considered at Harvard, but is not yet beyond the experimental stage. This memory system makes use of the property of phosphors that enables them to be excited into phosphorence by ultra-violet light, and extinguished by infra-red light. In the latter case the phosphor emits a bright flare of visible light.

In this system two cathode-ray tubes are used, one for reading and the other for writing. The writing tube emits ultra-violet light to ignite the phosphor in an area selected by the tube's deflection circuits. To read the same area the deflection circuits of the reading tube focus infra-red light on the selected band. A recorded spot will flare brightly and then die out; the bright flare of light is detected by a photocell and read out to external circuits. A nonrecorded spot will emit no light under infra-red bombardment.

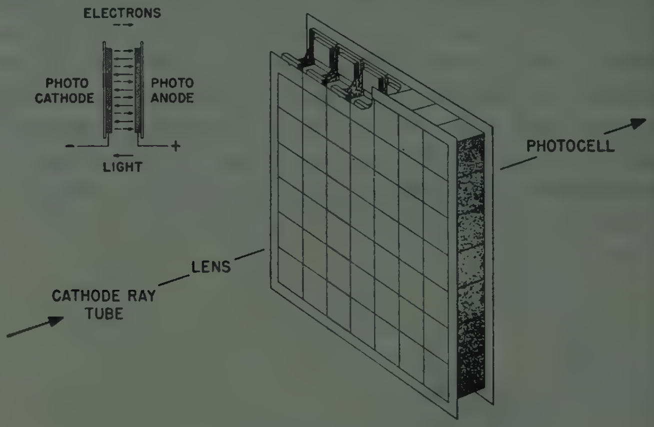


Fig. 20—Mellon optical memory system.

Mellon Optical

Another system utilizing light is the Mellon optical system developed at the Mellon Institute in Pittsburgh. Fig. 20 illustrates the Mellon memory. The elementary cell in the upper left-hand corner consists of two materials, one of which is photoemissive, and the other, phosphorescent. A high dc potential is placed across the two. When light strikes the photoemissive material, electrons pass toward phosphorescent material. This, in turn, emits photons which pass back to the photoemissive material. A continuous cycle of operation is set up once light has struck the photoemissive layer.

A typical array of cells is shown in the drawing. A cathode-ray tube and lens arrangement is used to select particular cells in order to ignite them. A convenient property of the system is that light focused on an already excited cell overloads and paralyzes the cell. Overloading or paralysis clears the cell. The change in total light can at any time be detected by the photocell, which is the output pickup of the system.

Krawinkel Tube

There are many other systems which have been suggested and which may yet be developed to a useful state. There is a variation of the electrostatic store suggested by Krawinkel. In this variation, the target is covered with a photoelectric layer upon which is superimposed a mosaic of insulating particles. Writing is done by the electron gun, but the output is obtained by shining light on the target from an external source. The backplate is made negative, and the charge areas consequently cause a phosphor screen to glow by photoemission.

Gas Triodes

Another promising matrix type of storage utilizes gas triodes. Typically, a thyratron whose striker is connected by a resistance divider to the two input lines can be fired when both input lines are sufficiently elevated. The output is read at the anodes. A variation on this system has one input fed to the grid and the other to the cathode of the gas tube. In either case, both inputs are required to fire a given tube, which then retains the single bit of information until cleared or until the power goes off. This system requires one tube for each bit of information.

Temperature-Sensitive Pigment

Another interesting optical storage system uses a temperature-sensitive pigment that exhibits what is known as color hysteresis in the temperature range between 0°C and 100°C. Under thermal stimulus the material changes color, remaining in the changed state at ambient temperatures and until an "opposite polarity" of heat is applied. Both heat and electrical discharge can be used to write, and no additional input is required beyond the energizing pulse. Read-out from these optical systems requires lenses and image tubes.

Electrolytic Diodes

Electrolytic diodes, which can be packaged with as many as 1,000 diodes per cubic inch, may lend themselves to the construction of small diode-matrix type memories. The active (columbium or tantalum) and inert (gold or silver) electrodes are immersed in a hygroscopic electrolyte, and the gases produced by the chemical reaction are catalytically recombined in a space above the cells. The electrolyte reabsorbs the vapor and thus maintains its chemical equilibrium. The back resistance of the electrolytic diode, due to the passive character of the inert electrode, is extremely high—ten to twenty megohms, compared to a typical forward resistance of ten ohms—except when the anodizing voltage is exceeded. The rather high interelectrode capacitances, of 500 mmf and more, render these diodes unfeasible for high-frequency work.

Coherers

Certain metallic powders act as insulators under weak electrical stimulus, but as conductors under the influence of stronger fields. A cell composed of a pair of electrodes immersed in one of these voltage-sensitive powders is called a coherer. When the potential difference between electrodes reaches the critical cross-over point, the resistance falls quite suddenly from a value of about 10^9 ohms to about 100 ohms. To effect decoherence—to restore the high-resistance condition—it is necessary merely to tap the cell mechanically (Marconi, who used a coherer to detect the first transatlantic wireless message, used the impact of a bell-clapper). The energy required to recohere a cell varies directly with the physical energy applied in the decohering. The disadvantage to the coherer system is, of course, the comparatively long time required to clear (decohere) the cell. Attempts to use supersonic or magnetic stimuli to clear the cell have not met with success. There have, however, been successful experiments in which thin layers of the voltage-sensitive powder immersed in a liquid (such as mineral oil) were decohered by electrical discharge across the electrodes, although this is believed to be a low-frequency electromechanical phenomenon.

Corona Discharge

In another type of memory system, a glass or other nonconducting disc rotates between pairs of probe-needle electrodes, or between a set of these electrodes on one side and a backplate on the other. Sufficiently high-voltage pulses applied to the writing electrodes leave coronas of electrostatic charge on the disc, which will remain for a few seconds. The corona discharge disc system, illustrated in Fig. 21, may contain a second set of electrodes for read-out into external circuitry and for external regeneration; regeneration may also be provided through the principle of the Wimshurst machine.

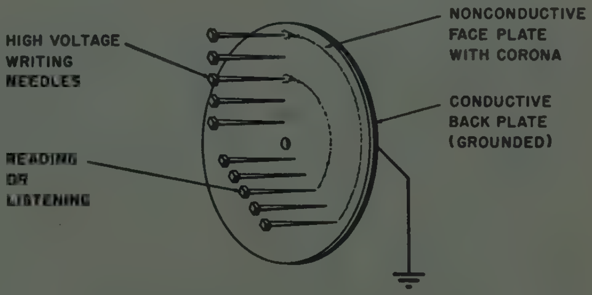

HIGH VOLTAGE WRITING NEEDLES
READING OR LISTENING
NONCONDUCTIVE FACE PLATE WITH CORONA
CONDUCTIVE BACK PLATE (GROUNDED)

Fig. 21—Corona discharge disc memory.

Erasing electrodes are charged to a high direct potential to destroy the corona. The system functions more efficiently in a partially evacuated chamber, or in one containing a readily ionizable gas such as neon or argon.

Still other systems make use of thixotropic liquids, crossed fields (magnetic, electric, or supersonic), and other phenomena. A form of memory is probably latent in the process of xerography. More sophisticated treatments of some of the systems already discussed here are possible: magnetic cells with multiple orientations or in multiple levels, for example.

Conclusion

A comparison of some of the important characteristics of the systems discussed here is presented in Fig. 22. The points of comparison are: destruction (a) on read-out, (b) in case of power failure, and (c) in the event of drifts in the locating system; the resolution problem; and the span of the memory, or its time existence. The yeses in the six starred cases under "Destruction by Power Failure" are conditional; power failures of short duration do not necessarily cause loss of memory, but long-time failures do. The conditional yes under resolution problem for the Mellon system is true only when the device lacks mechanical separation of cell areas.

	DESTRUCTION			RESOLUTION PROBLEM	LIMITED TIME EXISTENCE
	READOUT	POWER FAILURE	LOCATING SYSTEM DRIFT		
DELAY LINES	YES	YES	YES	YES	YES
ELECTROSTATIC INT PERIPHERY	YES	YES*	YES	YES	YES
HOLDING BEAM	NO	YES*	YES	YES	NO
SELECTRON	NO	YES*	NO	NO	NO
MAGNETIC DRUM	NO	NO	NO	YES	NO
FERROMAGNETIC CELL	YES*	NO	NO	NO	NO
FERROELECTRIC CELL	YES*	YES*	NO	NO	NO
DIODE - CAPACITOR	YES	YES*	NO	NO	YES
MELLON OPTICAL	YES	YES	YES	YES*	NO
PHOSPHORUS DRUMS	YES	YES*	YES	YES	YES

Fig. 22—Comparison and evaluation chart.

An important consideration in the evaluation of a memory system is that not all systems are equally applicable or economical for all purposes. For example, a storage system of 10^5 cells would not necessarily be economical if built with only 10^3 cells, and vice versa. For a small memory of 1,000 digits, a gas-tube arrangement might be best; the driving circuits are simple and cheap, and the price per cell is tolerable. An electrostatic memory, on the other hand, does not become economical until it includes at least 10^4 bits of information; the investment in switching and deflection circuits must be spread over a larger memory to be economical.

The favored memory system of this or that group becomes more blessed simply by being selected as the memory for a going computer. Thus, we can look with affection at delay lines and electrostatic stores, sometimes forgetting that our favorable feelings are due to our expenditure of work and our successful experience with them. Other systems, which have not received this attention, may possibly become as good as any of the present systems once someone has spent the effort on them.

It is also important to remember that there has been intensive effort in the computer field over a short period of time, and all the wood may not be hard. Had we been able to proceed more slowly, some of our decisions might have been different. We have not scratched the surface of the subject—not even thoroughly tested and evaluated the systems which have been suggested. The future undoubtedly will see the development of still more ideas, any one of which may become more nearly the ideal memory system than any which have been discussed here.

Acknowledgment

Credit is due the Radio Corporation of America for permission to reproduce Fig. 12, and John Wiley & Sons, Inc., New York, N. Y., publishers of "Storage Tubes and Their Basic Principles," by M. Knoll and B. Kazan, for Fig. 11.

Bibliography

Adams, J. F., "The Krawinkel Image-Storing CR Tube," *Fiat Final Report 1027;* April, 1947.
Auerbach, A. A., J. P. Eckert, Jr., R. F. Shaw, J. R. Weiner and L. D. Wilson, "The Binac," Proc. I.R.E., vol. 40, pp. 12–29; January, 1952.
Auerbach, I. L., J. P. Eckert, Jr., R. F. Shaw, and C. B. Sheppard, "Mercury delay line memory using a pulse rate of several megacycles," Proc. I.R.E., vol. 37; pp. 855–861; August, 1949.
Bell, P. R., G. D. Forbes and E. F. MacNichols, Jr., "Storage Tubes," *Wave Forms* (Chapter 21), Radiation Laboratory Series #19, McGraw-Hill Book Co., New York, N. Y., 1949.
Beveridge, H. N. and W. W. Keith, "Piezoelectric transducers for ultrasonic delay lines," Proc. I.R.E., vol. 40, pp. 828–835; July, 1952.
Davis, W. W., "The SEAC Memory Using Williams' Storage," NBS Electronic Computer Laboratory Report #12,3-7R; April 20, 1951.
Eckert, J. P., Jr., H. Lukoff and G. Smoliar, "A dynamically regenerated electrostatic memory system," Proc. I.R.E., vol. 38, pp. 498–510; May, 1950.
Goodell, John D. and Tenny Lode, "Multistable magnetic memory techniques," *Radio Elec. Eng.*, pp. 3–5; December, 1951.
Haeff, A. V., "A memory tube," *Electronics*, vol. 20, pp. 80–83; September, 1947.
Hill, J. L., "Design features of a magnetic drum information storage system," *Proc. ACM;* March 28, 1950.
Holt, Arthur W., "An Experimental Rapid Access Memory Using Diodes and Capacitors," NBS Electronic Computer Laboratory Report, pp. 133–141; 1953.
Knoll, M. and B. Kazan, *Storage Tubes and Their Basic Principles*, John Wiley & Sons, New York, N. Y., p. 22 et sqq., p. 44 et sqq., p. 85 et sqq.; 1952.
Lephakis, A. J., "An electrostatic tube storage system," Proc. I.R.E., vol. 39, pp. 1413–1415; November, 1951.
Mellon Institute of Industrial Research: Computer Component Fellowship #347, Quarterly Report no. 3 (April–July, 1951) Sections I through VI; *Quarterly Report* no. 5 (October–January, 1952) Sections I through V; *Quarterly Report* no. 6 (January–April, 1952) Sections II, III, VI; *Quarterly Report* no. 9 (October–January, 1953) Section III.
Olsen, Kenneth H., "A Magnetic Matrix Switch and its Incorporation into a Coincident Current Memory," Digital Computer Lab., MIT, *Report R-211;* June 6, 1952.
Papian, William N., "A coincident current magnetic memory cell for the storage of digital information," Proc. I.R.E., vol. 40, pp. 475–478; April, 1952.
Parker, C. V., "Charge storage in cathode-ray tubes," Proc. I.R.E., vol. 39, pp. 900–907; August, 1951.
Rajchmann, J., "The selective electrostatic storage tube," *RCA Review*, vol. XII, pp. 53–97; March, 1951.
Scorgie, D. G., "Lead Networks Utilizing a Saturable Core Memory," National Radiation Lab. *Report 4006;* July 16, 1952.
Wang, An, "Magnetic delay line storage," Proc. I.R.E., vol. 39, pp. 401–407; April, 1951.
Williams, F. C. and T. Kilburn, "A storage system for use with binary-digital computing machines," *Proc. IEE* (London), vol. 96, Part II, pp. 183–202; and Part III, pp. 77–100, 1949; and vol. 97, Part IV, pp. 453–454, 1950.

A Myriabit Magnetic-Core Matrix Memory[*]

JAN A. RAJCHMAN[†], FELLOW, IRE

Summary—**A coincident-current magnetic-core matrix memory was built giving random access to any of 10,000 bits in a few μsec. The memory cores, of a diameter less than 1/16″, are made on an automatic press from especially synthesized magnetic ceramic material with rectangular hysteresis loop. Automatic test techniques permit rapid sorting to insure uniformity of the magnetic properties of the cores. The memory array is driven by two ten-by-ten dc biased magnetic switches which reduce the number of address-selecting access vacuum tube drivers to 40 and the required driving current to the order of a few hundred milliamperes. The read-out signal originating from a winding linking all 10,000 cores is freed from the disturbing contributions of partially excited cores on the selected lines by integration over a period of time in which these cores are subject to equal and opposite magnetizing forces. The principles and techniques evolved for this experimental model demonstrate the practicability of an extremely reliable fast random access memory with a capacity of hundreds of thousands of bits, ushering in a new era in storage devices for information handling systems.**

INTRODUCTION

MAGNETIC CORES WITH rectangular hysteresis loops have the inherent storage and switching capabilities required from an element of a random access matrix memory based on current coincidence. This was recognized independently by J. W. Forrester[1] and the author, who initiated the early efforts to develop such a memory at the Massachusetts Institute of Technology and RCA Laboratories, respectively. Last year an operating unit with the relatively modest capacity of 256 bits was made to operate successfully,[2] and it was predicted[2] that extension to capacities with thousands of bits was possible in the near future.

This paper describes an operating experimental memory with a capacity of 10,000 bits, named Myriabit. (Myria means 10,000 or many, according to Webster.) This relatively large capacity was attained by basic changes in the cores themselves and in the systems used for driving and interrogating the memory.

Most of the initial work in this field was done with metallic cores which were the first materials to exhibit rectangular hysteresis loops. Cores obtained by winding 5 wraps of $\frac{1}{8}$ mil Mo Permalloy 4-79 on ceramic bobbins were used in the smaller memory built last year.[2] These cores have relatively long switch-over times of about five microseconds, when used in the coincident memory, and they are intrinsically expensive to fabricate. Owing mostly to their low electrical conductivity, the ferromagnetic spinel materials, often called "ferrites," have much faster switch-over times. Core fabrication, consisting of molding from a powder-like material, is inherently inexpensive. The potentialities of these materials prompted research at General Ceramics Co. and RCA Laboratories towards obtaining sufficient loop rectangularity in materials which otherwise were ideal. Early in 1952 some materials[3] were promising, and in the summer of that year both organizations synthetized a material for practical use. The properties of the G.C. material, used by the Digital Computer Laboratory of M.I.T., were described recently.[4] The nature and actual preparation of the RCA materials, which are "manganese magnesium ferrites," are to be published.[5]

The remarkable success of these ferromagnetic spinel materials offered a challenge to build a memory of very large capacity, since it became possible to obtain the cores cheaply and in great quantities. Of course, this required an automatic molding machine. We initiated a development to that effect at the Stokes Machine Co. which modified one of its machines for this use.[6] The necessary machine and tooling work will not be described as it is fairly conventional.

The operation of a large memory array poses two main problems: driving and obtaining a reading signal free of masking disturbances. The solutions to these problems found last year[2] were adequate for an array of 256 cores and would be useful for larger ones. We chose deliberately an array size large enough to exceed the limitations of these solutions and to force research into methods applicable to a size one order of magnitude greater. This determined the choice of 10,000 bits. This storage capacity had the incidental advantages of being greater than any obtained in a single electrostatic storage tube and of demonstrating the flexibility of magnetic switching by being an arbitrarily chosen integral power of ten.

The driving magnetic switches for the memory array were worked out to be themselves matrix switches arrays of ten-by-ten cores biased by a dc current. These switches lend themselves to a simple construction in which the limiting effects of the earlier switches are essentially eliminated.

A solution to the read-out problem was found which is applicable to practically any size, even when the array comprises cores with substantial departures from loop rectangularity and considerable variations in the magnetic characteristics. The read-out signal, originating from a winding linking all 10,000 array cores, is essentially freed from the disturbing contributions of partially excited cores on the selected lines by integration over a period of time in which these cores are subject to equal and opposite magnetizing forces.

---

[*] Decimal classification: 621.375.2. Original manuscript received by the Institute July 15, 1953.

[†] RCA Laboratories, Princeton, N. J.

[1] J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," *Jour. Appl. Phys.*, vol. 22, pp. 44–48; January, 1951.

[2] Jan Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Review*, vol. XIII, pp. 183–201; June, 1952. (Also presented at I.R.E. National Convention, N. Y.; March 5, 1952.)

[3] General Ceramic material body 666, RCA Laboratories Body 160B.

[4] D. R. Brown and E. Albers-Shoenberg, "Ferrites speed digital computers," *Electronics*, pp. 146–149; April, 1953.

[5] I. J. Hegyi, "Ferromagnetic spinel with rectangular hysteresis loops," to be published shortly in *Jour. of Appl. Phys.*

[6] "A3 Eureka Tablet Machine," F. J. Stokes Co.

We concentrated on the building of a memory with access to a single core in a large array because all essentials of switching into and reading from a memory having access to many cores in parallel are encountered in this simpler case. The principles evolved are indeed extendable to the parallel-access type for which the core memory is eminently suitable.

After a review of the principle of the memory itself this paper describes (1) the construction, core testing and characteristics of the memory array, (2) the principles, construction and operation of the driving switches, (3) the reading method, (4) the programming and the functions of the associated circuits. It concludes by predicting a great future for the magnetic matrix memory, which approaches the ideal rapid random access memory closer than any yet constructed.

The Principle of the Memory

Consider an array of magnetic cores arranged in rows and columns. Each core is linked by three windings. Two of the windings are connected in series by rows and columns, and a third is a common series winding. Single turn windings consisting of straight conductors linking the cores are shown on Fig. 1, as this is the most convenient way of constructing the array. All cores are magnetized to one or the other of the two remanant inductions represented by points P and N on the idealized hysteresis loop of Fig. 1. In this state, the array is holding information previously stored. In order to set any given core to the desired remanance, P or N, pulses of current in one or the other direction are simultaneously applied to the row and column of the core. The amplitude of these currents is so adjusted that their additive, i.e. doubling effects, produce sufficient magnetomotive force to exceed the knee of the loop for the selected core at the intersection of the lines but insufficient to exceed the knee for the other cores in the selected lines where they act singly. Consequently, the selected core will be magnetized in the desired direction while all other cores in the matrix will remain unaffected.

For the read-out, consider the voltage induced in the common winding when read-in currents of a standard direction, e.g., toward P, are sent through the lines of the core to be interrogated. Ideally, the flux can change only in that core, so that the existence of a voltage indicates that the core switched from N to P, while absence of voltage indicates that it was originally at P. This type of read-out signal was used successfully in previous memories.[1,2,4] In order to eliminate the contributions of other cores on the selected lines which actually occur because of imperfections of loop squareness, the interrogating currents in the present memory are pulses of first the one and then the other polarity, as will be explained. In any case the state of the interrogated core is ascertained by changing it, so that a restoring cycle controlled by the read-out signal is necessary, otherwise read-out would be destructive.

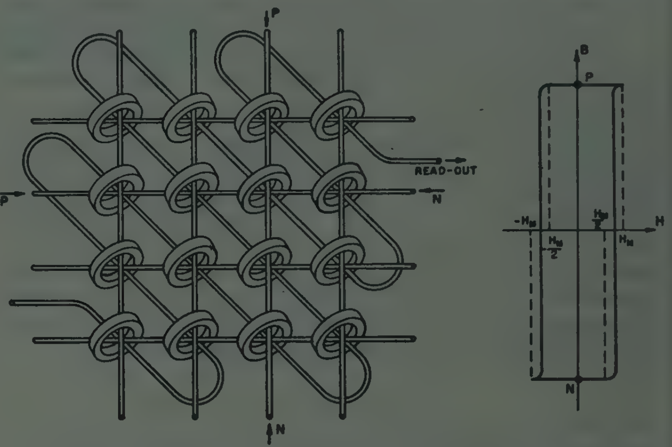


Fig. 1—Double coincident magnetic matrix memory and idealized hysteresis loop.

The Construction of the Memory Array

The 10,000 cores of the myriabit memory were molded from "manganese magnesium ferrite"[5] in the shape of tiny toroids, with 0.054″ O.D., 0.034″ I.D. and 0.016″ height. These cores, after individual tests, were wired into a plane array in a manner schematized on Fig. 1 and shown on Fig. 2, following page. The size of these cores, which is just about that of the printed letter *o* in the word core, can be appreciated also by comparison to a match head shown in the detailed Fig. 3 on page 1396. The row and column wires, #32 double formex total O.D. of 0.009″, pass straight through the cores positioned at 45° and serve as their supports. These line wires 0.080″ apart, with addition marker spaces between decades, are stretched between tiny terminals supported on a bakelite frame of about 10″×10″. The reading winding is a series connection of 100 smaller windings each linking the 100 cores of squares 10 by 10. These consist of bare 0.006″ wire running back and forth diagonally through the cores.

The miniature size of the cores, the smallest conveniently handled without special microtooling, was chosen to minimize the current and power driving requirements rather than to maximize the bit-per-unit volume packing density. Even so, the current for switching the core, at optimum discrimination in a two-to-one regime, is 1.1 ampere-turns, and the energy is about 5×10^{-8} joules. The brute force wiring of the myriabit array taxed the patience of a person for six weeks. Simple semi-automatic wiring techniques would reduce this time to hours.

AUTOMATIC CORE TESTING

The memory array must not comprise a single core failing to give some specified minimum performance. To insure this, it is absolutely necessary to test every core before it is wired in, because it is practically impossible to control the fabrication of the cores to the absolute degree required even though the average yield may be very high. Manual testing of the cores far exceeds the effort required to make them on automatic molding machines, hence the need for automatic testing.

The principle of an automatic core tester which we devised is shown on Fig. 4, page 1397. The cores are poured into the dish of a "syntron elevator." The vertical and angular vibrations of the dish force the cores up a helical track on its periphery. The top core is held by a slotted stop (the only part of the vibrator visible on the left of the figure) and is picked up by one of the radial metal pins of a rotating wheel. Test trains of current pulses obtained through a transformer are sent through the pin as it passes on slide contacts. The resulting induced voltages, characterizing the core, are taken by a second set of contacts and are analyzed according to specified criterions by electronic circuitry which does or does not produce an acceptance signal. This signal activates a relay which positions a slotted arm so as to "wipe off" the accepted core. The unacceptable cores pass the location of the unactivated wiping arm and fall in a reject container. The experimental model of the tester operates at the rate of 40 to 60 cores a minute which is comparable to the rate of the core molding machine. Unfortunately, the tester was not available in time so the cores for the Myriabit were tested by tedious manual methods.

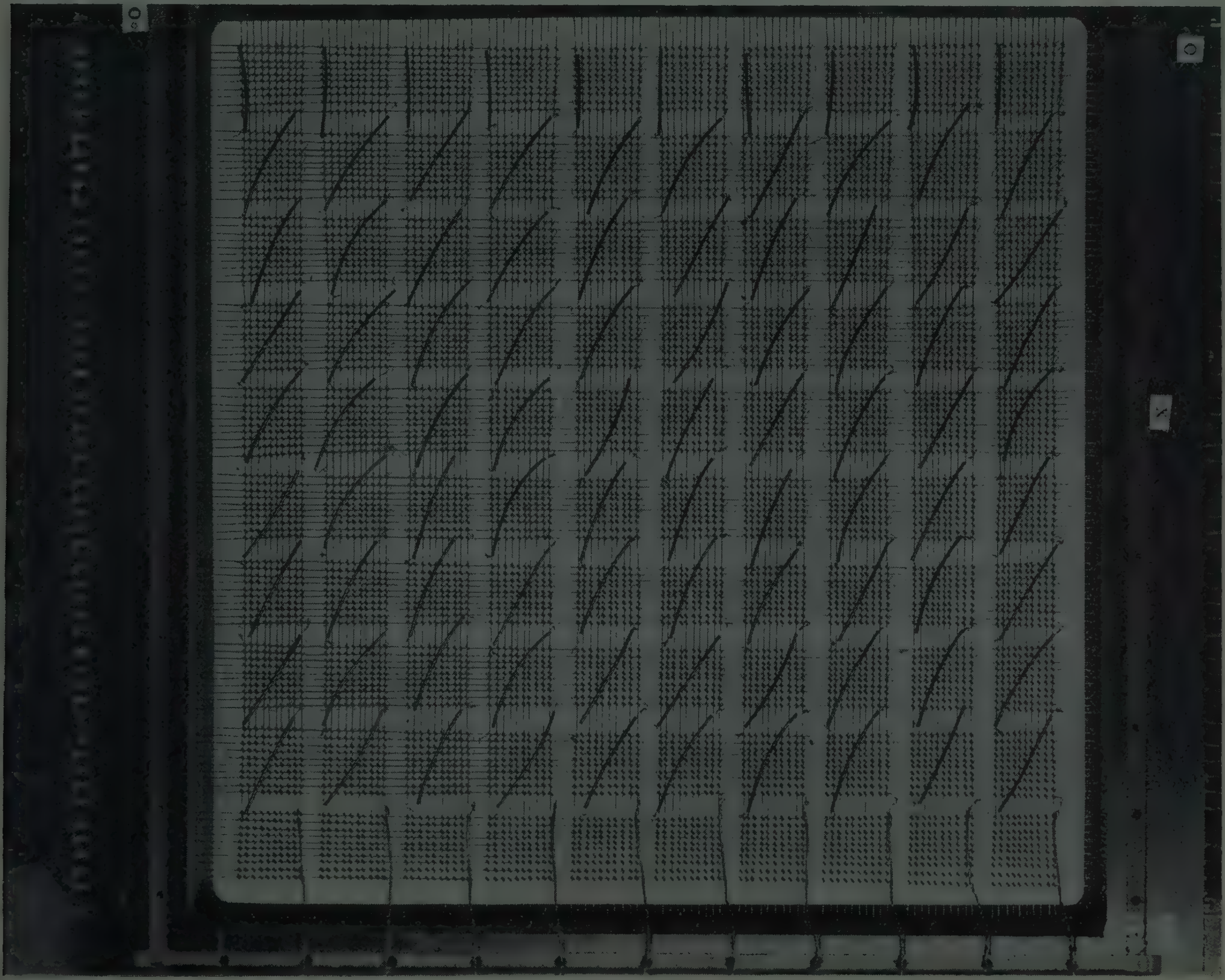


Fig. 2—Myriabit array.

In speculating about the relative merits of memories with discrete storing elements and those with a continuous storing medium, one often considers the latter preferable because no tedious fabrication of a large number of elements is required. But because in most applications of digital storage no single inoperative element can be tolerated, an imperfection in the continuous medium renders the entire device useless. As the imperfections can be detected only by the operation of the completed memory, the possibility of pretesting every element to gain certainty of its operation before assembly shifts the preference to memories with discrete elements. This is particularly true when both manufacture and testing of the elements are automatic.

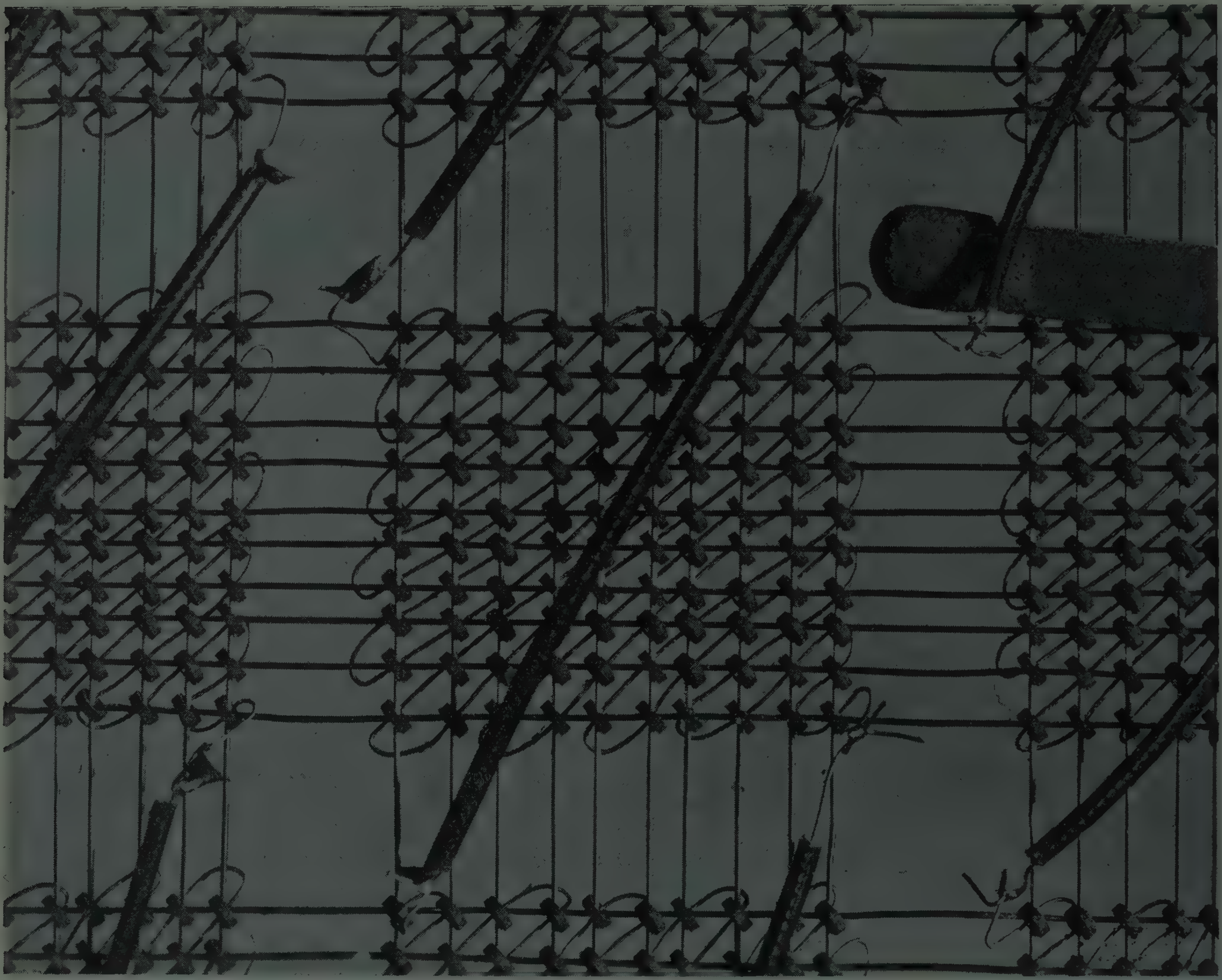


Fig. 3—Detail of Myriabit array.

The Characteristics of the Memory Core

The actual properties of the single core, which necessarily depart from ideal rectangularity, ultimately determine the performance of the memory array in any system.[7] A typical "manganese magnesium ferromagnetic spinel" core of 0.054″ O.D., 0.034″ I.D. and 0.016″ height used in the myriabit has been measured by magnetizing it by various current pulse trains and observing the resulting induced voltages on an oscilloscope synchronized so as to superimpose the traces, as shown on page 1397, Fig. 5. The amplitude of the current pulses, adjusted to obtain optimum ratio of full-excited to half-excited responses, turned out to be 1.1 ampere-turn and is referred to *P* or *N* depending on the polarity. The voltages resulting from the schedules $P\frac{N}{2}\frac{N}{2}\frac{P}{2}N\frac{P}{2}$ and $P\frac{N}{2}\frac{N}{2}PN$ show the high degree of rectangularity of the hysteresis loop by the smallness of the traces due to half excitations which had to be expanded ten times to be measurable. The hysteresis loops of Fig. 6, page 1398, were constructed by integrating the voltage wave shapes of Fig. 5 (including the part due to current decay) and other similar ones obtained for the different pulse schedules, such as $N\frac{P}{2}\frac{N}{2}P$, $P\frac{N}{2}\frac{N}{2}\frac{P}{2}\frac{N}{2}N$ and *PPN*. These minor loops, drawn to an expanded scale, show the essential core behavior, although good accuracy was hard to obtain in spite of averaging over several curves and the consideration of obvious symmetries.

We found it convenient to describe the state of the core by the series of pulses to which it was submitted. Following this convention, the selected core in the memory array is at P after the simultaneous $\frac{P}{2}$ excitations of its selecting lines, since it is subjected to a full P excitation. When these are followed by two $\frac{N}{2}$ excitations of its selecting lines occurring in succession—as in a write-in system to be described—the selected core is brought from P to $P\,\frac{N}{2}$ and then from $P\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}$. When the $\frac{N}{2}$ excitations are simultaneous, the core is brought to N, since the state PN is equivalent to N. The state of the core at the peak of a current pulse is denoted by putting in parentheses the last letter referring to the current pulse yet unterminated as shown on Fig. 6 for the magnetizations of ±0.55 and ±1.1 amp.

---

[7] William N. Papian, "A coincident-current magnetic memory cell for the storage of digital information," Proc. I.R.E., vol. 40, pp. 475–478; April 1952. (Also "A coincident-current magnetic memory unit," Master's thesis, E.E. Dept., M.I.T.; Aug., 1951).

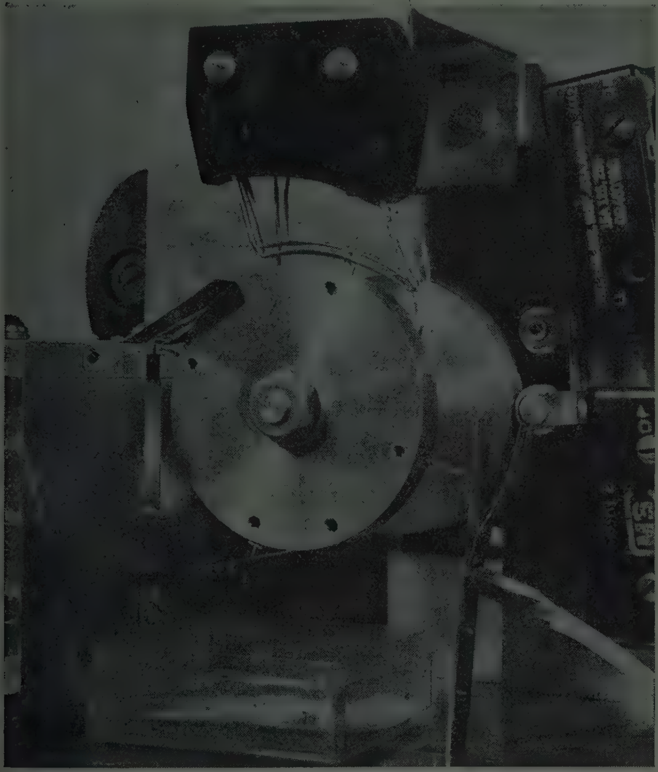


Fig. 4—Automatic core tester.

turn. The rate of current rise and the losses[8] in the cores determine the length of the voltage pulses and their peak values, the latter not corresponding necessarily to the flux changes of the hysteresis loops such as those of Fig. 6. For very fast rising pulses (0.05 μsec), the core switches over in about 0.3 μsec and the voltage pulse exhibits the familiar double maxima observed with metal cores.[9] The slower current pulses of Fig. 5, rising in 0.2 to 0.3 μsec, are more significant for memory applications, since they simulate more closely the pulses furnished by cores of the magnetic switch described below. The turn-over time is now about 0.6 μsec, almost half of it being due to the current pulse rise.

When access is made to some core(s) of a line many times in succession, the remanant state of the other cores, suffering many half excitations, must remain near P or N, so as to retain the stored information. With a magnetic switch drive, every access necessarily produces a $\frac{P}{2}$ excitation followed by an $\frac{N}{2}$ one, and cumulative demagnetizations tend to be prevented, as was pointed out previously.[2] This may be verified on Fig. 6. The loop $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$ is closed within measurable accuracy. The loop N to $N\,\frac{P}{2}\,\frac{N}{2}$ is not closed, but it is found that the loop from $N\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$ to $N\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$ is closed, so that on the third access the core has essentially reached its asymptotic minor loop. We found, incidentally, that the schedule $N\,\frac{P}{2}\,\frac{P}{2}\,\frac{P}{2}\,\frac{P}{2}\cdots$ leads also to an asymptotic value $N\,(\frac{P}{2})_\infty$ near the value $N\,\frac{P}{2}\,\frac{P}{2}$ for this core.

MANGANESE; MAGNESIUM; FERROMAGNETIC,
SPINEL CORE
0.54″ O.D. 0.34″ I.D. 0.016″ H.

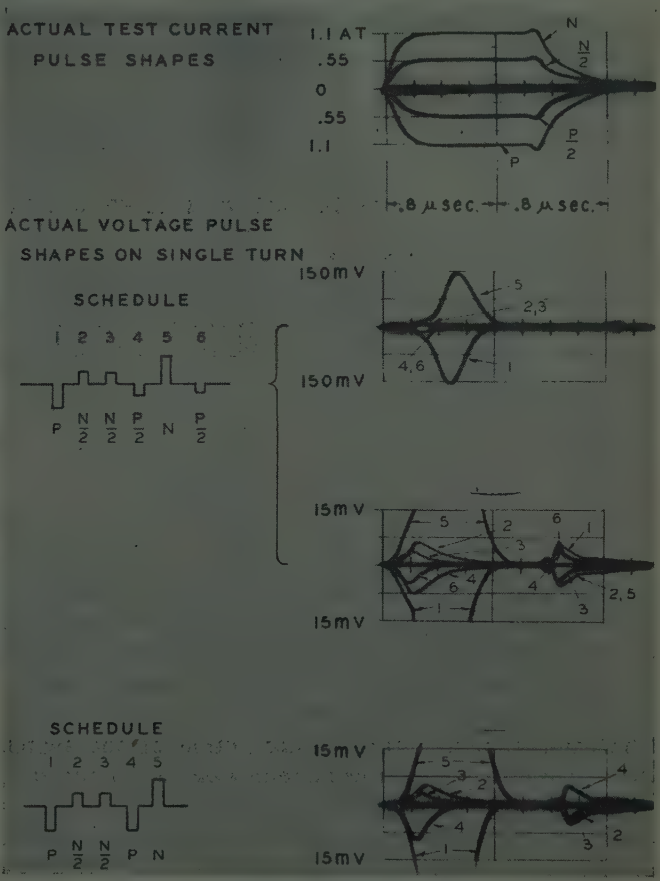


Fig. 5—Voltages from typical memory core.

On the other hand, for cores made of a less "rectangular" material we found that $N\,(\frac{P}{2})_\infty$ was essentially at the origin ($B=H=0$), while $N\,(\frac{P}{2}\,\frac{N}{2})_\infty$ was only somewhat lower than P. This shows the virtue of the demagnetization—remagnetization cycle inherent with transformer drive (but not with unscheduled direct tube drive).

SWITCHING THE MEMORY ARRAY

The problem of switching into the n cores of the memory array is reduced to that of switching into $2\sqrt{n}$

---

[8] The relaxation losses are dominant in ferrospinel materials.

[9] J. Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Review*, vol. XIII, pp. 183–201, fig. 6; June, 1952.

channels because the cores themselves provide double coincidence switching. Because both polarities of current are required in each channel, the number of drive tubes or of any other uni-directional electronic device is double. Although $4\sqrt{n}$ can be relatively much smaller than n it is still very large, for example, 400 tubes would be required to drive a 10,000 core array.

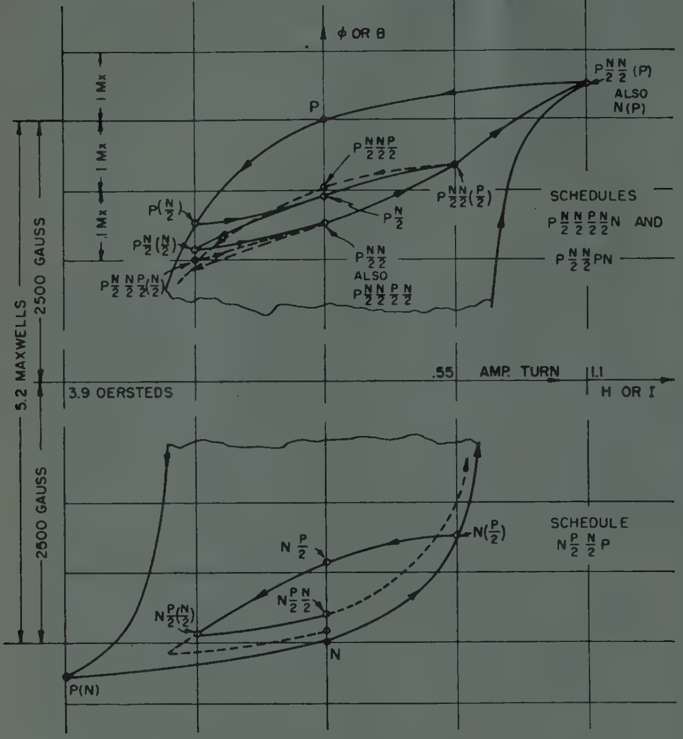


Fig. 6—Minor hysteresis loops of memory core.

"Commutator" magnetic switches were designed last year[2,10] in which one out of 2^k channels is selected by k input push-pull channels. When two such switches drive the memory array, the number of input channels is reduced to the minimum possible, i.e. $\log_2 n$, and at the same time the transformer action of the switch cores can provide a better matching of the driving tube impedance. Two commutator switches with 4 inputs and 16 outputs each were used to drive the 256 memory core array,[2] requiring in all only 16 relatively small driving tubes (8 push-pull channels).

These commutator switches are a most elegant solution for the binary to one-out-of-many conversion or "decoder." However, as the number of binary positions increases, there is a greater number of combinatorially required turns on each core to establish the k-way coincidence, and this sets some practical limitations to the size. The construction becomes a great deal more complicated, and it is more difficult to put sufficient number of turns on the driving primaries to properly match the tube impedances. This is true even when the window of the cores is full of copper because an increasingly large proportion of that copper carries no useful current when the core is switched over. Furthermore, the electrostatic capacities between the many multi-turn windings produce delays and ringing, effects particularly serious with fast ferrite cores. The delays, which differ for the various windings linking a given core, are detrimental to the operation of the type of switch in which the selecting current pulses themselves turn over the selected core, since they must be in exact time coincidence.[11] In the type of commutator switch in which the selecting currents are inhibiting—leaving only the selected core uninhibited—and the drive winding links all cores, the effects of the delay and ringing can be reduced when a longer pulse scheduling involving "priming" and "driving" periods is used. As considerable analysis has shown, a practical solution to the many position decoder switch is in a cascaded use of the "commutator" switches in a sort of a tree where the outputs of a first commutator are the drivers for the next. Such an arrangement would no doubt be practical for the 100-way switches required to drive the myriabit memory. In these, full decoding could be obtained from two binary coded decimal digits, the octuple coincidence being obtained, for example, in two quadruple coincidence steps.

Double Coincident Biased Switches

Actually, we developed much simpler 100-way switches based on double coincidence. The switch cores are in a matrix array, 10 by 10 in our case, and are linked by row and column windings, as shown on Fig. 7. In addition, there is a winding linking in the same sense every core and carrying a dc biasing current. Each of the 100 switch cores has a single turn output winding

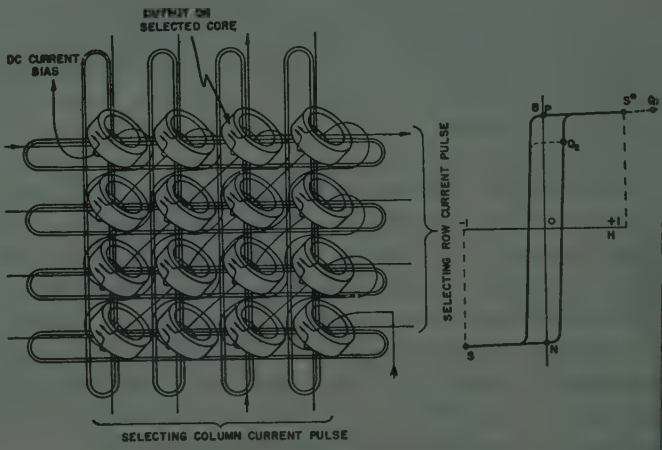


Fig. 7—Double coincident biased magnetic switch.

---

[10] Similar switches were designed independently by K. Olsen of M.I.T.

[11] In spite of this difficulty, R. Stuart-Williams and M. Rosenber in June, 1952, drove a 256 array by two 16-way commutator switche all cores being "ferrites," in a manner identical to the all-met memory described by the author, previously.

which energizes a line on one side of the myriabit memory array. Another similar 100-way switch energizes the other side as shown on Figs. 8 and 9.

The combinatorial principle of the switch is as follows: The biasing magnetizing force of one unit (−1) keeps all cores well saturated (point S on Fig. 7). The selecting row and column current pulses produce magnetizing forces of one unit (+1), so that only the doubly excited selected core is subject to a positive magnetizing force ($1+1-1=1$), while all singly excited line cores are subject to no magnetizing force ($1-1=0$) and the remaining cores simply remain biased (−1). The discrimination between selected and unselected cores depends only on the saturation characteristics (or slope of the $B-H$ loop for large H's) of the cores and not on distinguishing between excitations in the ratio two-to-one as is the case for the memory cores, so that the bias and driving currents may be arbitrarily large. When the selecting line pulses rise, the selected core is switched from negative saturation to or towards positive saturation (e.g. points S^* on Fig. 7), and when these pulses decay the dc biasing current automatically brings the selected core back to negative saturation without the necessity of a programmed restoring pulse. Correspondingly, a positive and then a negative voltage pulse are induced in the output winding of the selected core. The switch requires, for m outputs, $2\sqrt{m}$ driving tubes and not $4\sqrt{m}$ as it would without common restora-

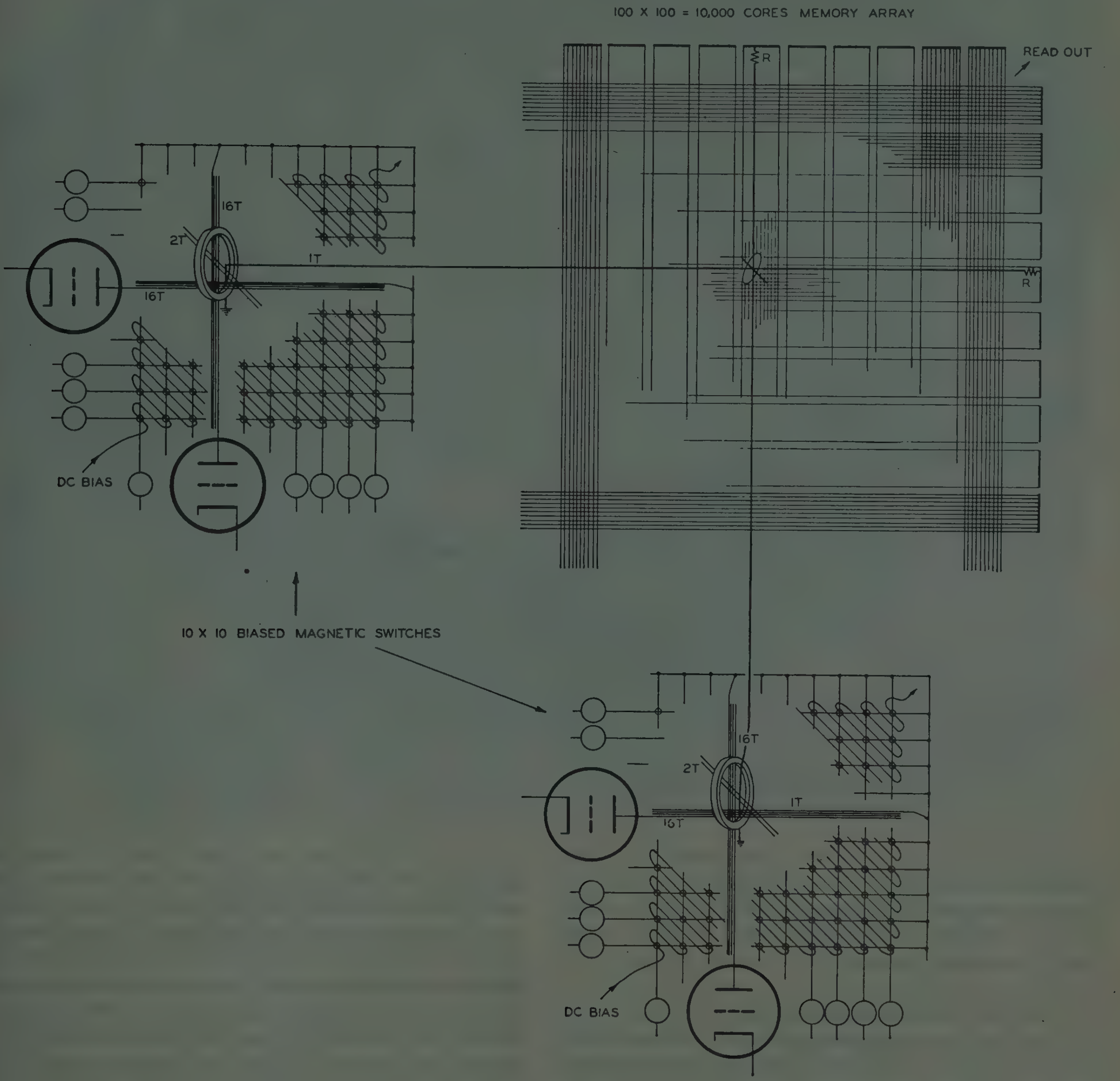

100 X 100 = 10,000 CORES MEMORY ARRAY
READ OUT
R
R
16T
2T
IT
16T
DC BIAS
10 X 10 BIASED MAGNETIC SWITCHES
16T
2T
IT
16T
DC BIAS

Fig. 8—Myriabit memory.

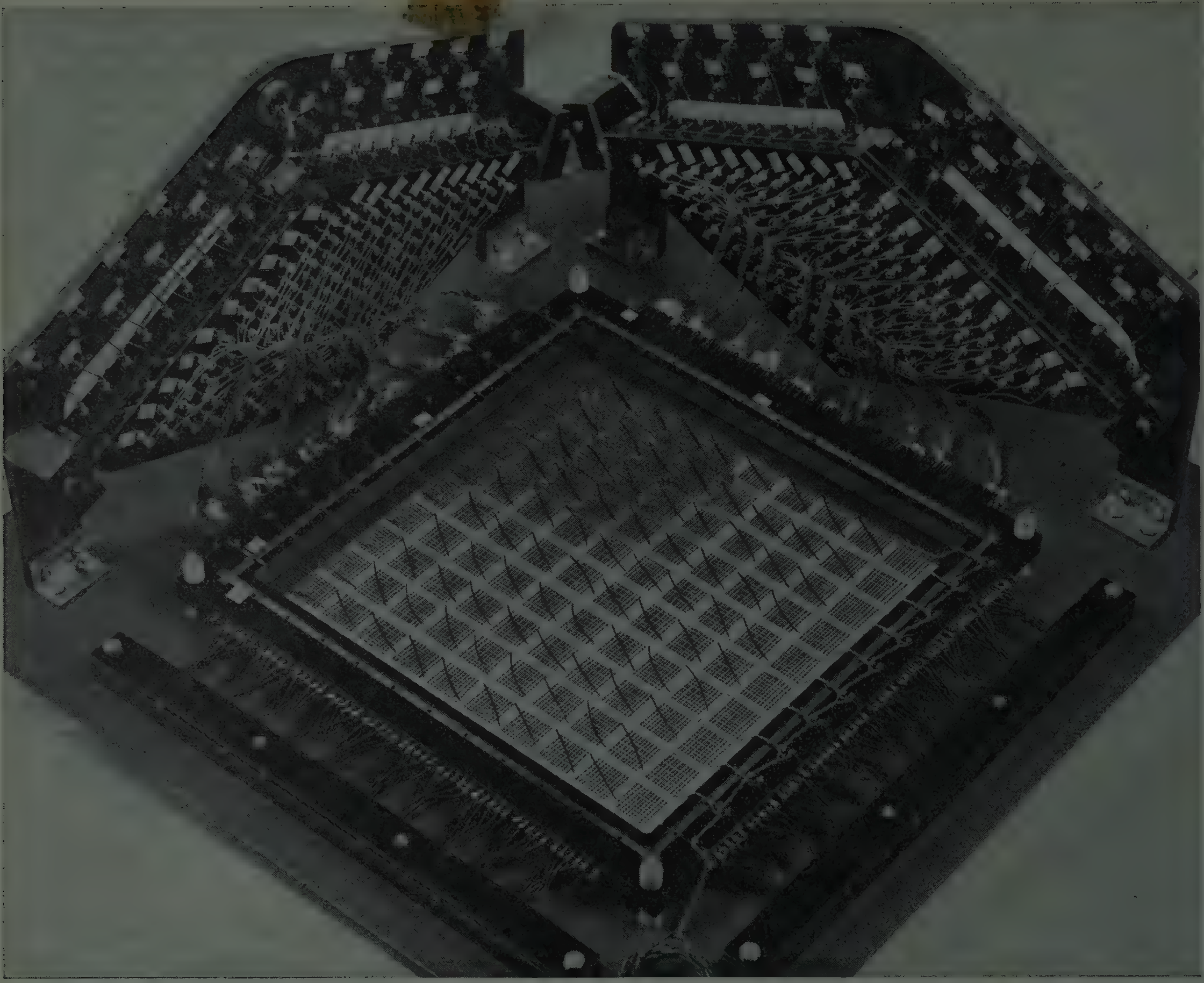


Fig. 9—Memory array and switches.

tion. It is not a decoder down to the binary code, but in our case, the loss of driving tube economy is insignificant because only twenty tubes are required per switch or a total of 40 tubes for both switches, as compared to two sets of 8 pairs of push-pull tubes required in a binary-coded decimal system or a total of 32 driving tubes.

Complete magnetic decoding could be obtained by driving each of these "double coincidence biased" switches by two quadruple coincidence commutator switches. In fact, this would be the preferred way of using magnetic switches cumulatively: Use double coincidence only in the last switch with most cores, and multiple coincidence in the first or early switches whose total number of cores is relatively small. We chose direct drive of the double coincidence switches in this project and conventional electronic binary to one-out-of-ten decoding, in order to devote most development efforts to the memory array itself.

The two ten-by-ten switches operate the memory array of 10,000 cores as follows. Current pulses are applied to the address selecting row and column windings of both switches. All four currents rise simultaneously and remain constant for a time at least equal to the switching time of the switch and memory cores. The two corresponding switch cores turn over and induce currents in the memory array lines to which they are linked. The sense of linkage is so chosen that their effects are additive, so that the selected core in the memory array is set to a given remanance, e.g. point P of Fig. 6. If all four current pulses decay simultaneously, reverse effects are produced and the selected memory core is set from state P to state N. If, however, the two pulses on one of the driving switches terminate at a different time than the two pulses on the other switch, the negative currents on the lines of the memory array will occur in succession and will bring the selected memory core to $P\frac{N}{2}\frac{N}{2}$ after inflicting two partial demagnetizations $\frac{N}{2}$ upon it. This proves a simple method for registry or writing information in the memory: control of the length of the pulses on one switch. Such control is obtained conveniently by feeding all the driving tubes from a common master pulse (see Fig. 15). To write P, the action of the master pulse is inhibited before its termination on one of the switches, while such inhibition is omitted to write N. The simultaneity of the relevant pulse edges is insured, since they originate from a common master pulse.

The biased switches can be used in a variety of ways to drive a memory in which access is in parallel to a group of digits. For example, consider the cores of the 100×100 myriabit plane subdivided for parallel access to ten digits into subplanes of 10×100. The lines in the 100-way x direction are driven by a 10×10 switch, as described above, and are excited by the longer standard current pulses. The ten groups of lines in the y direction are driven by ten, 10-way switches. Every position of these decade switches is controlled (directly or by double coincidence in a 2×5 arrangement) by the address selecting pulses which are also the standard longer pulses. For example, core #7 in all ten decade switches is excited if the 7th line in every digit subplane is to be addressed. In addition, each decade switch may be inhibited by the write signal corresponding to its digit position, so as to shorten its standard exciting pulses. The inhibited switches will cause a P write-in (or rather $P\ \frac{N}{2}\ \frac{N}{2}$), while the non-inhibited ones will cause an N write-in, in the corresponding subplanes. Of course, a three-dimensional arrangement physically paralleling the digit planes is possible.

CONSTRUCTION OF THE SWITCHES

The ten rows and ten columns primary windings have 16 turns, while the outputs are single turns so that the cores act not only as switches but current step-up transformers. Each turn of these windings links every core, i.e. any line of cores is wound by a single common winding as shown schematically In Fig. 7. In this way the effects of interturn capacity, which would be very severe if separate 16-turn winding on each core of the line were in series, are greatly reduced. The pulse shape deterioration is equalized and differences in time of pulse occurrence are negligibly small. Also, this winding method lends itself to a very simple switch construction. The row and column windings are set at an angle, 45° in our case, allowing straight passage of both windings through the cylindrical hole of the core which was appreciable height-to-diameter ratio. The two sets of windings are spaced approximately a core diameter apart, which permits them to be the mechanical supports of the cores and keeps the interwinding capacity to a minimum. Fig. 10 shows the diamond-shaped switches.

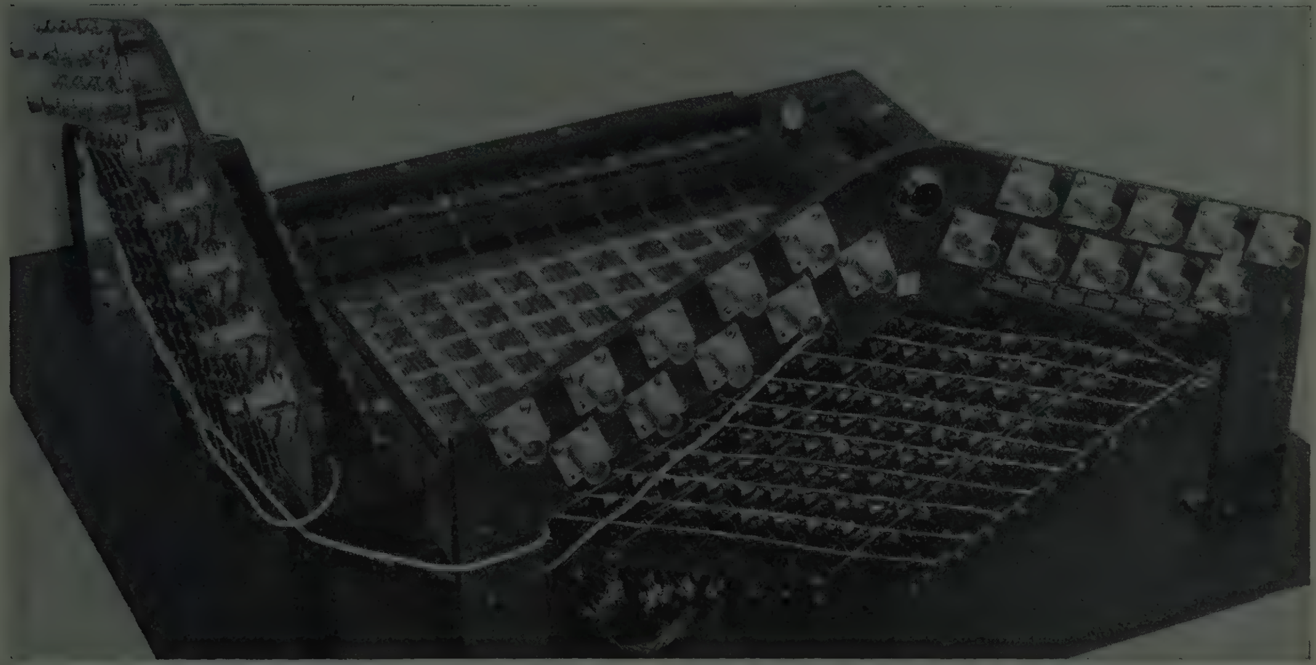


Fig. 10—Diamond-shape switch.

The cores of the switches are wound of 40 wraps $\frac{1}{8}$ mil Mo-Permalloy $\frac{1}{8}''$ wide tape on ceramic bobbins about 5/16″ O.D. and 3/16″ I.D. This does not limit the speed of operation, as it does when similar cores are used in a memory array, because the driving current is not limited by the requirements of good discrimination under a two-to-one regime, but can be made as large as required by the losses inherent in the fast turn-over.[12]

---

[12] e.g. The voltage responses of Fig. 6 ("Static magnetic matrix memory and switching circuits").

The turn-over time seems to be, on the basis of a few tests, inversely proportional to the drive. Switching times of about one microsecond are obtained for current drives comparable to those required for turning over presently available ferrospinel magnetic cores. The large magnetizing force is required in metals because of high losses and in ferrites because of high coercivity. The advantage of the metal core lies in its better saturation characteristic, resulting in smaller disturbing outputs on partially excited cores. To obtain similar performance in an experimental ferrite switch it was necessary to use several cores on each switch position so as to minimize by neutralization the otherwise larger disturbing signals.

THE OPERATION OF THE SWITCHES DRIVING THE MEMORY ARRAY

The detailed analysis of the operation of the switch, whose combinatorial principle was explained above, is beyond the scope of this paper because the cores act as very lossy nonlinear transformers with nonlinear and variable loads. The empirical results will be explained by considering first the behavior in the loads.

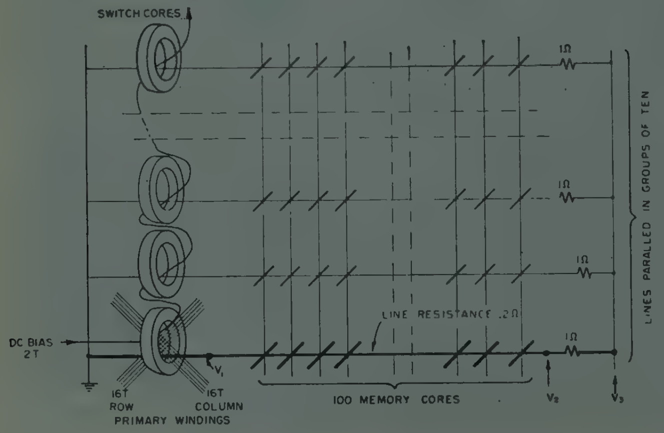


Fig. 11—Output circuit of switch core.

Consider the output circuit of a switch core loaded by a memory line as illustrated on Fig. 11. If ϕ_s is the flux in the switch core, ϕ_m the total of the flux of the 100 memory cores on a line, R the total resistance of the circuit and i the instantaneous current, then:

$$\frac{d\phi_s}{dt} = \frac{d\phi_m}{dt} + iR \tag{1}$$

and

$$\Delta\phi_s = \Delta\phi_m - \int_0^t Ridt, \tag{2}$$

where $\Delta\phi_s$ and $\Delta\phi_m$ are the changes of flux from 0 to t. The capacities are so small that displacement currents can be neglected. The verification of these equations for the particular values required by the typical memory-core characteristics will be taken as a demonstration of the switch operation.

The voltage wave shapes V_1, V_2 and V_3 as defined on Fig. 11, are shown on the oscillophotographs of Fig. 12. The current i, given as $V_2 - V_3$, rises in 0.2 μsec to a peak of 600 ma while remaining above 500 ma for about 0.4 μsec, so that it is fairly similar to the test current pulses of Fig. 5. Consequently, the memory core operates near optimum drive. The voltage $V_1 - V_2$ is produced by the change of flux in the half-excited 100 memory cores on the line and the resistive drop of the driving wire itself. At the peak, this difference is 2 volts, the resistive drop 0.1 volt and the contribution of the selected core 0.16 volt, so that the 99 unselected cores contribute each about 17 mv. This value is to be compare to the 4.5 mv produced by the core when going from $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,(\frac{P}{2})$ and 8 mv when going from N to $N\,(\frac{P}{2})$, as seen on Fig. 5. The large discrepancy of these results can be partially accounted for by the higher current peak and somewhat faster current rise in the switch as compared to the test pulses. But it is mostly due to the fact that the voltages are very sensitive to the loss characteristics of the cores whose average, in the myriabit, may be slightly different from the typical core chosen for tests.

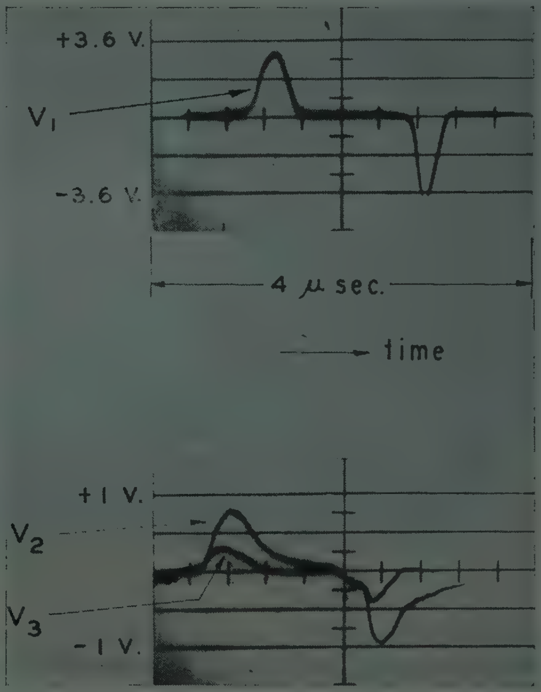


Fig. 12—Voltages in output circuit of switch core.

The agreement of flux changes, independent of core losses in this instance, is much closer. The flux change $\Delta\phi_s = V_1 dt$ is 101 Mx (1 Maxwell $= 10^{-8}$ volt-sec), and $\int V_2 dt$ is 76 Mx, as determined by measuring the areas under the curves on Fig. 12. The integrated voltage drop across the 0.2 ohm of the 10″ line wires is about 10 Mx. This leaves 15 Mx for $\Delta\phi_s$. This value should be between $99 \times 1.2 + 5.2 = 17.1$ Mx and $99 \times .08 + 5.2 = 12.1$ Mx, depending on the storing state of the 99 cores, on the basis of the measured changes of flux of the typical core as shown on Fig. 6, since the change from N to $N\,\frac{P}{2}$ is 0.12 Mx, and from $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}$ is 0.08 Mx and for the selected core from N to P is 5.2 Mx.

The series resistance of 1 ohm was inserted in the myriabit array lines in order to shorten the time constant L/R of the circuit and obtain the desired effective differentiation of the primary pulses. This resistance acts also as a current regulator for the variable counter-voltage produced by the half excited line cores which depends on the state of these cores (nominally varying from 0.45 to 0.8 V).

The driving primary current pulses and the dc bias were adjusted so as to obtain the desired outputs just described. The dc bias is 3.8 A.T. (or 1.9A. in 2 turns) and the driving pulses in each switch line 4.4 A.T. (275 ma in 16 turns). The effective positive magnetizing force $(2\times 4.4-3.8=5)$ is somewhat higher than the negative magnetizing force due to the dc (3.8 A.T.) acting alone after the termination of the exciting pulses (points S and S^* on Fig. 7), while the positive output voltages are somewhat smaller than the negative ones. This asymmetry is due to the fact that the voltages are dependent on the variations of current, which, near maximum, rises more slowly than it decays near the end. The switch can be deliberately driven unsymmetrically, the positive drive terminating in points such as Q_1 or Q_2 on Fig. 7 if it is desired to obtain a sharp positive and a broad negative pulse or vice-versa, corresponding naturally to equal positive and negative flux changes.

The voltage peak induced in the primary 16 turns is 50 volts or 3.1 volts per turn, while only 2.8 volts are obtained in the single turn secondary showing some leakage of flux. From the total effective current drive of 8.8 A.T., about half overcomes the dc bias; most of the remaining current overcomes the high losses of the fast-switched metal core while only about $\frac{1}{2}$ A.T. appear in the useful load. Even with this poor performance from the point of view of a power transformer, the over-all performance of the switch is efficient, as it allows the use of 40 tubes capable of carrying 275 ma instead of 400 tubes capable of carrying 550 ma which would be required in a myriabit array driven directly by tubes.

READING FROM THE MEMORY

Reading from the memory or interrogating it at a given address is accomplished by sending definite current pulses through the appropriate lines and observing the induced voltages in a winding linking all 10,000 cores of the array. Consider first the simultaneous $P/2$ drives on both selecting lines used in earlier memories[2] bringing the core from N to (P) or from $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,(P)$. If the selected core were the only one on the reading winding, the discrimination between the two peak voltages would be 160 mv to 9.5 mv or 17 to 1 and between the two flux changes 5.2 Mx to 0.2 Mx or 26 to 1, as can be seen on Figs. 5 and 6. Incidentally, the ratio of final flux change N to P to that from $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}$ is 35 to 1. Unavoidably, each of the 198 cores on the two selecting lines contributes its small share of peak voltage, which is 4.5 mv when going from $P\,\frac{N}{2}\,\frac{N}{2}$ to $P\,\frac{N}{2}\,\frac{N}{2}\,(\frac{P}{2})$, and 8 mv when going from N to $N\,(\frac{P}{2})$, or almost 8 mv from $N\,(\frac{P}{2}\,\frac{N}{2})_\infty$ to $N\,(\frac{P}{2}\,\frac{N}{2})_\infty\,(\frac{P}{2})$. If the reading winding linked all cores in the same direction, these voltages could add up to $198\times 8\text{mv}\approx 1.6$ volts or ten times the voltage from the selected core. With the checkerboard pattern of linkage polarities, the direction of linkage changing for every core on every line, used already in all previous memories,[2,4] these voltages tend to cancel each other. At best, when all cores are uniform and storing in the same polarity, the contributions of 98 cores on one line exactly cancel the contributions of the 98 cores on the other and the two remaining cores increase the already high discrimination of the selected core. When the cores on the selected lines are in different remanant states, the cancellation is no longer perfect even if the cores were uniform, since their contributions are 4.5 or 8 mv depending on the polarity of their remanant state. At worst there will be 100 cores contributing 8 mv and 98 contributing 4.5 mv in the opposite direction, so that the total disturbance will be 357 mv or roughly 2.2 times as much as the voltage from the selected core.

The peak voltage is seen to be a completely inadequate signal even when the cores are uniform. The strobing of the voltage past the peak provides a much better signal. This system was used in previous memories[2,4] and is particularly adaptable to the slower metal core arrays. With very fast magnetic ceramic cores and large arrays driven by switches, as in our instance, the strobing technique is more difficult.

By exciting the selected core first in one polarity and then the other, it is possible to neutralize the unwanted contributions of the half excited unselected cores obtained in the first step by those of the second. Such a cancellation method does not depend, in principle, on the remanant state of any core nor whether it has like properties to other cores. One such method consists in integrating the signal over the period of time in which the selected core is excited to P and then to N. Consider first the contribution of the selected core to the integrated signal. If the core is initially at N, it will be driven to P and then returned to N, so that the net change of flux is precisely zero. If initially at P, the core will be driven to PP (very close to P, not shown on Fig. 6) and then to N so that the net change of flux is large, i.e. 5.2 Mx in our case. Consider next the contribution of an unselected core on the selected lines which was initially at $P\,\frac{N}{2}\,\frac{N}{2}$ going to $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}$ and then $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$. As far as we could measure, the states $P\,\frac{N}{2}\,\frac{N}{2}$ and $P\,\frac{N}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$ are identical as mentioned before, and the core describes a closed minor loop with zero contribution to the integrated signal (see Fig. 6). Finally, consider an unselected core initially at N, changing to $N\,\frac{P}{2}$ and then to $N\,\frac{P}{2}\,\frac{N}{2}$. Here the minor loop is not closed and there is a slight net change of flux of about 0.04 Mx.

This non-closure of the minor loop, from N to $N\,\frac{P}{2}\,\frac{N}{2}$, is not detrimental because the filling of the memory array by the regular writing-in process necessarily leaves most negatively storing cores in the state $N\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}\cdots$ where the cycle $\frac{P}{2}\,\frac{N}{2}$ is repeated not less than three times. As was mentioned before, the minor loops after the first excursion are almost closed, and after the second, are completely closed. Therefore it is only the unselected cores in state N which contribute to the integrated signal. There can be at most two such cores, since writing along any line necessarily subjects all cores to cyclic $\frac{P}{2}\,\frac{N}{2}$ excursions. (In the five-step schedule actually there are two cycles, i.e. $\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$, for each write-in.) The greatest integrated unwanted reading signal occurs when the selected core changes from $N\left(\frac{P}{2}\,\frac{N}{2}\right)_\infty$ to N and the two unselected cores in their non-asymptotic states N are unfavorably linked by the checkerboard reading winding and change from N to $N\,\frac{P}{2}\,\frac{N}{2}$. For our cores this total flux change is about 0.22 Mx or about 1/25 of the wanted signal of 5.2 Mx (points $N\,\frac{P}{2}\,\frac{N}{2}\,\frac{P}{2}\,\frac{N}{2}$ and $N\left(\frac{P}{2}\,\frac{N}{2}\right)_\infty$ not shown on Fig. 6).

The ratio of wanted-to-unwanted reading signal in the integration method is seen to be large and is independent of the size of the array and of the uniformity of core properties. In practice, this ratio is determined primarily by the characteristics of the integrating circuit.

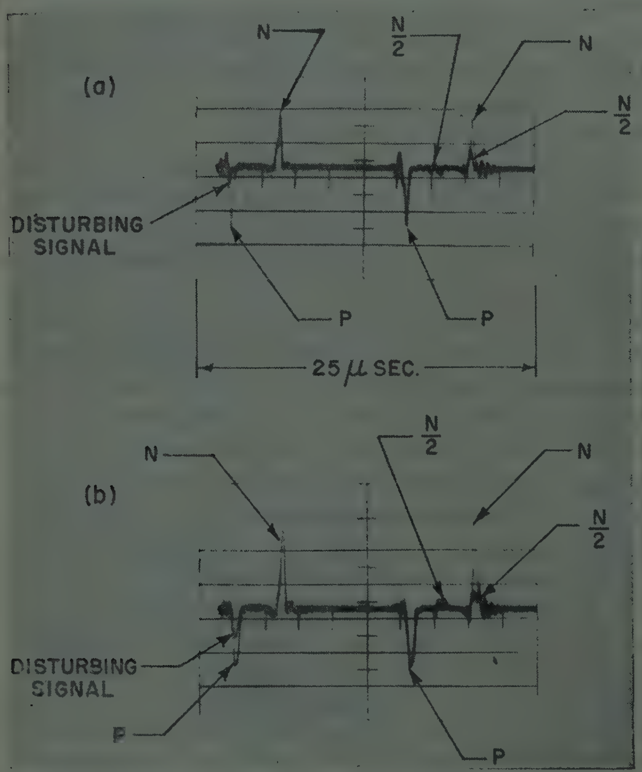


Fig. 13—Voltages on reading winding for typical core on lines with (a) well-balanced, (b) poorly balanced cores.

The experimental myriabit was wired with cores which were tested manually, every core only once, while standards of tests were being worked out. This resulted in poor uniformity as the bulk of the cores have outputs varying in the ratio 2 to 1, while about 50 cores are outside that range, including 15 positions giving practically no output (one core missing). The lack of core uniformity is apparent from the typical direct reading signals illustrated for two lines on Fig. 13. Even so, the integrated signal is useful for all but the 15 positions and sets reliably an output flip-flop.

The reading winding can, but does not need to be, in a checkerboard pattern with the integration read-out system, since the disturbances from a given core are cancelled by opposite disturbances from the core itself rather than by disturbances from other cores. Nevertheless, the myriabit array was checkerboard wound in order to reduce the excursion of voltage in the integrating circuit. Also, in order to neutralize the voltages induced in the relatively large read winding loop through straight air linkage the 100 subdivided, checkerboarded read windings were connected themselves in an appropriate checkerboard.

PROGRAMMING

The program of pulses for the memory operation, shown on Fig. 14, can be considered to be made of 5 steps of equal duration. To read from the memory, identical pulses of current are applied to both x and y switches in step 1. During the plateau of these pulses, the selected core is set in P. The minimum length of this plateau, determined by the time constant L/R of the load circuit so as to allow the positive current to decay to zero, was found to be 2.5 μsec as has been explained. With a larger resistance, this duration could approach the limit of 0.3 μsec set by the switch-over time of the memory core itself, but excessive drive power would be required if it was desired to shorten the length below 1 μsec. After the end of the pulse the memory core is set to N, but again 2.5 μsec must be allowed in step 2 for the decay of the negative current (see Fig. 12). The voltage appearing on the reading winding is integrated over the 5 μsec of steps 1 and 2, and its integrated value at the end of step 2 is the signal indicating the initial state of the interrogated core. In step 3 current pulses are again applied to the switches

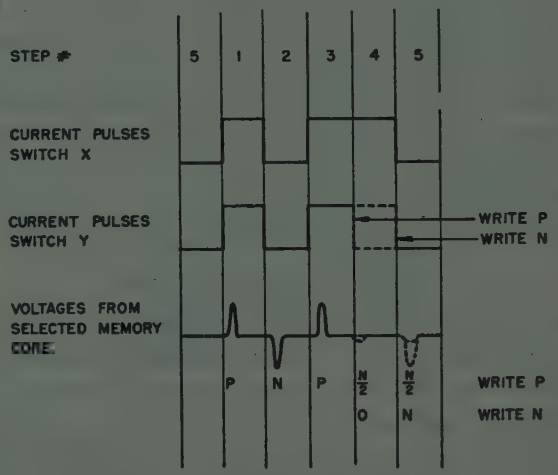


Fig. 14—Five-step schedule of operation.

setting the selected core back to *P* and simultaneously the signal sets the circuits which will control step 4. In step 4, both pairs of currents driving switches *x* and *y* remain at their plateau if the core was initially at *N* while the pair of pulses driving switch *y* are terminated if the core was initially at *P*. In step 5, the negative currents in the output die off. The core is seen to be restored to its initial condition in the steps 3, 4 and 5 which constitute the rewrite. These three steps could be omitted if the core were found to be in *N*, but by their use the time of step 3 is available for the reading integrated signal to set the controlling circuits.

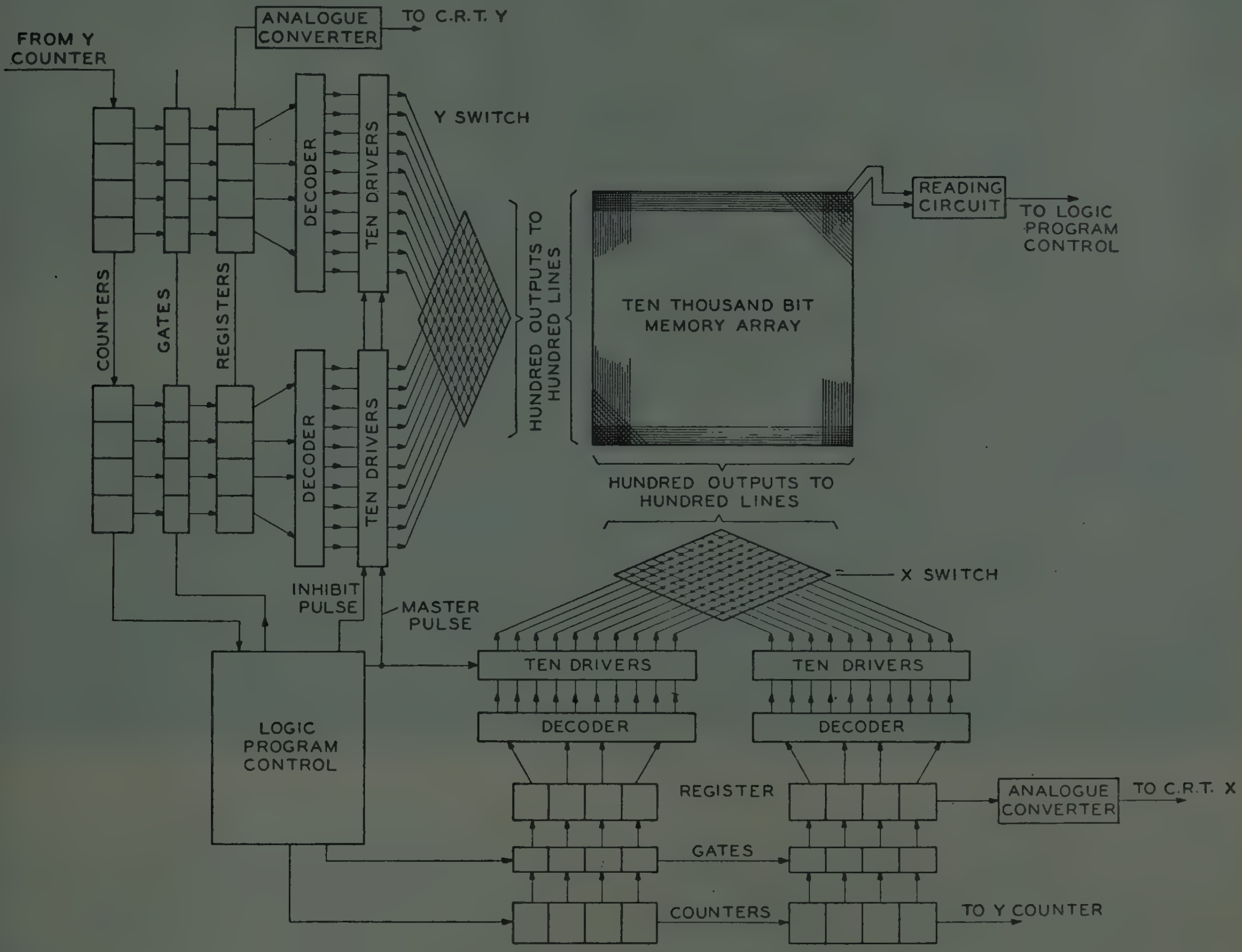

ANALOGUE CONVERTER
TO C.R.T. Y
FROM Y COUNTER
Y SWITCH
DECODER
TEN DRIVERS
COUNTERS
GATES
REGISTERS
DECODER
TEN DRIVERS
HUNDRED OUTPUTS TO HUNDRED LINES
READING CIRCUIT
TO LOGIC PROGRAM CONTROL
TEN THOUSAND BIT MEMORY ARRAY
HUNDRED OUTPUTS TO HUNDRED LINES
X SWITCH
INHIBIT PULSE
MASTER PULSE
TEN DRIVERS
TEN DRIVERS
LOGIC PROGRAM CONTROL
DECODER
DECODER
REGISTER
ANALOGUE CONVERTER
TO C.R.T. X
GATES
COUNTERS
TO Y COUNTER

Fig. 15.—Block diagram of circuits.

To write or register in the memory, only steps 3, 4, and 5 are required. For simplicity, all 5 steps are used in our system. The write signal is used instead of the read signal to control whether the currents driving the switch *y* in step 4 are present or not.

The total time for a write-in or read-out, leaving the memory ready for the next write or read operation, is $5 \times 2.5 = 12.5$ μsec. This time, which may be considered as the random access time, could be reduced to 5 μsec as mentioned above. Further saving of time could be accomplished by omitting steps 1 and 2 in writing.

ASSOCIATED CIRCUITS

The electronic circuits built to test the myriabit memory are shown in Fig. 16 and in block form on Fig. 15. The address is set on the four address registers in the binary coded decimal form. It is decoded to the straight decimal system by vacuum tubes and it primes one switch driver in each group of ten. The driver tubes are two 6AU5's in parallel. A master pulse derived from the logic control fires the primed drivers at the appropriate time. A four-digit binary coded decimal counter allows scanning through all the memory addresses. The scan can be through all 10,000 cores, or any manually selected 1000, 100 or 10, or it can be stopped on any particular core. The logic control furnishes pulses required for the five step program (or other test programs). The reading integrating circuit is of a "bootstrap" variety and is followed by amplifiers, clamps and discriminating circuits. The output flipflop-controls the restoring circuits in the logic control. The addresses are converted to analogue voltages for deflecting the beam of a cathode-ray tube. The partial or total contents of the myriabit can be displayed on the tube by controlling the beam intensity by the reading signal.

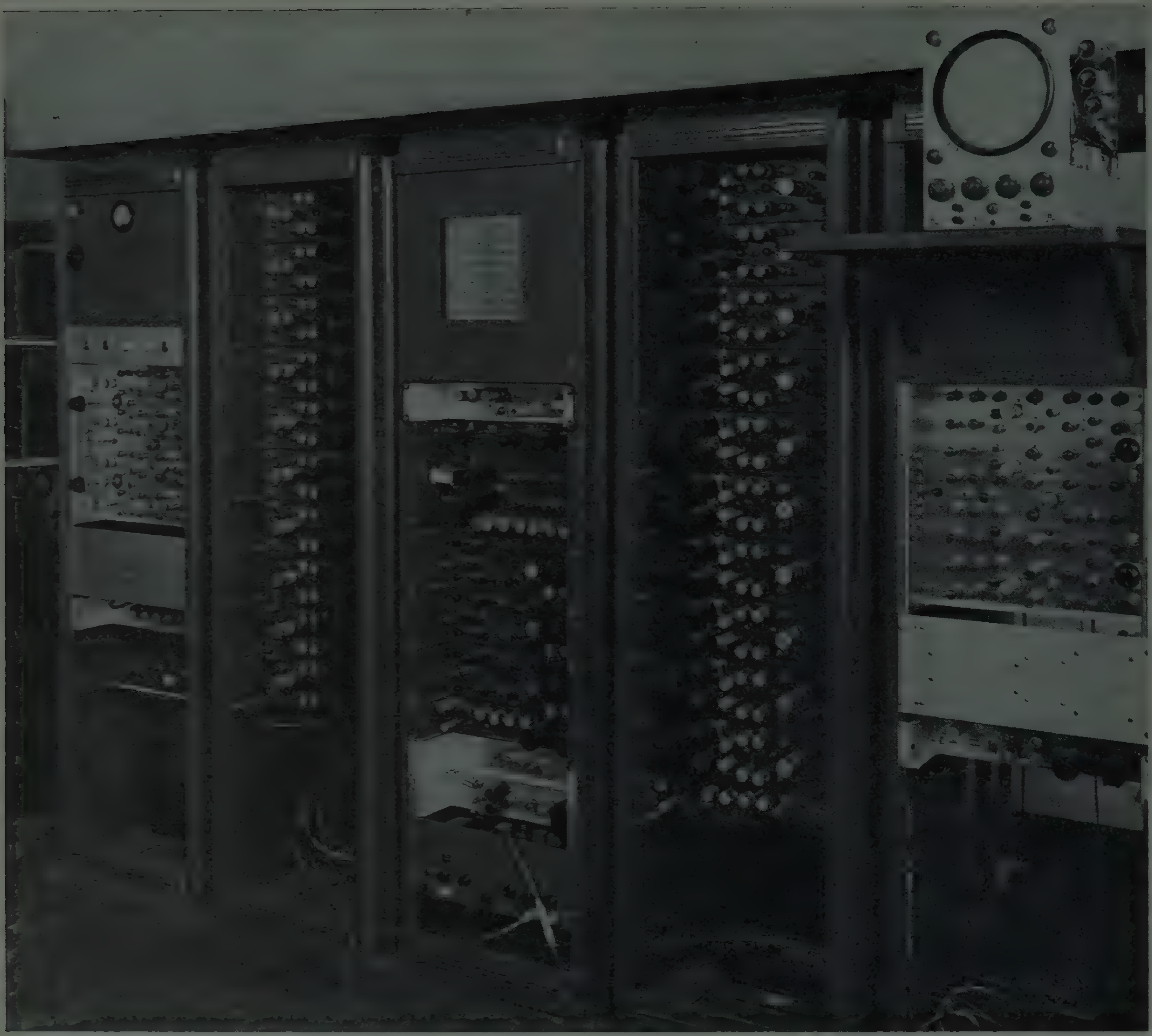


Fig. 16—View of circuits.

These circuits, for experimenting with the memory, were overdesigned on purpose. Properly engineered circuits for operating the memory in a computer could be simpler, require less power, and would be combined with the computing circuit themselves. While little is said here of the almost conventional circuitry, it did constitute a major part of our effort as seems unavoidable in high-speed memory research.

The Experimental Results

At the time of writing of this paper, testing of the memory is still in progress, but the results obtained show that the memory performs as expected. The stored information in any core was always found to be retained, even after a very large number of accesses to other cores on its selecting lines. The integrated signal from any of the 9985 operating cores reliably sets the output flip-flop even when the pattern of stored information is deliberately set to give maximum disturbance. The 15 non-operative core positions include one with a missing core, and others which are cracked or accidentally passed the relatively crude testing to which the cores were subjected. Most of the tests were made with a 5 step program lasting 25 μsec, step #3 being 15 μsec, but the memory was operated also with the designed 5 step cycle time of 12.5 μsec.

Conclusions

Ferrospinel magnetic materials with rectangular hysteresis loops were developed in the middle of last year. By the use of automatic molding and testing machines it became practical to envisage memories with capacities in tens of thousands of bits. The basic problems in the realization of such memories are the switching and read-out methods by which fast random access can be obtained efficiently. Successful solutions to these problems are demonstrated in the experimental 10,000 bit memory reported in this paper.

Last year, on the basis of a memory with 256 bits, we predicted[2] that in the near future storage capacities of thousands or tens of thousands would be achieved and capacities of millions, in a more distant future. As the first part of this prediction is now realized we venture to reiterate the second. Of course, this will require great innovations in construction techniques and still further improvements in magnetic switching. But we have no doubt that memories in which random access to millions of information bits in a few microseconds will be available at a relatively low cost. This will usher in a new area in information handling systems which may have profound consequences, not only in scientific computations, but wherever complicated or repetitive computations burden our lives.

ACKNOWLEDGMENT

This project was brought to success by many members of the RCA Laboratories, principally R. Stuart-Williams[13] and M. Rosenberg[13] who made important original contributions. The essential ferrospinel materials research work was done by I. J. Hegyi, R. S. Weisz and R. L. Harvey. Many of the attendant tests were made by T. Arbaeus, American-Scandinavian trainee at the Laboratories. J. Lehmann and S. Sternberg designed many of the circuits and C. H. Vose the circuit lay-outs. A. Lo and W. Modlinski participated in initial measurements and M. Kaplan from RCA Victor Division did most of the final testing of the system. R. L. Hunyady wired the myriabit array, and J. Walentine contributed in the design and built the automatic core tester.

The project had the constant supervising interests of V. K. Zworykin.

---

[13] With International Telemeter Co. since May, 1953.

Photographic Techniques for Information Storage*

GILBERT W. KING, GEORGE W. BROWN, AND LOUIS N. RIDENOUR†, SENIOR MEMBER, IRE

Summary—**Photographic media are examined as vehicles for the storage of digital information. Storage devices of total capacity in the range from 10^7 to 10^9 bits, with favorable random-access features, appear to be achievable. Alternative methods of reading are suggested. The logical association of a much smaller erasable storage unit (such as a magnetic drum) with a large photographic store completely removes, for most practical applications, the difficulties arising from the fact that rapid erasure and rewriting are not possible in a photographic storage medium. Methods for writing in the information to be stored are briefly considered.**

I. INTRODUCTION

PHOTOGRAPHIC MEDIA suggest themselves as means of information storage for computers and other information-processing machines because of the high density of information storage that available emulsions can yield. The resolving power of the best photographic emulsions is in excess of 10^3 marks per millimeter, corresponding to superficial information densities of about 10^6 bits/mm^2. Even when this number is reduced by practical considerations involving registration in the reading process, discrimination against spurious signals arising from dust or scratches, etc., a very substantial information density remains. It has been appreciated for some time that all the information ever written in books could be stored in a few cubic yards of photographic plates, and equally well realized that such a library is impracticable because of the difficulty presented by suitable access to the stored information.

The high information density offered by photographic storage has led to some work on its use in connection with computers. In 1947, Arthur W. Tyler[1] and R. D. O'Neal[2] of the Eastman Kodak Company reported at a Harvard symposium the results of some preliminary work which they had done. The point of view motivating this work was rather different from that which is appropriate today. Tyler and O'Neal were concerned with the use of photographic storage as an input or an input-output device for high-speed digital computers. This led them to put major attention on strip film as the photographic medium, and the well known difficulties of registering film in a gate forced them to an excessive reduction of the information density actually used. In addition to difficulties of registration, the handling of strip film inevitably produces degradation of the emulsion surface through scratches produced by the handling mechanism and dirt deposited on the film during handling.

Because Tyler and O'Neal also wished to provide for random access to the information stored on the film, their film-handling apparatus had to provide for rapid starting, stopping and reversal. All in all, the ground

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 1, 1953.

† International Telemeter Corporation, Los Angeles, California; aided by the Office of Naval Research.

[1] Arthur W. Tyler, *Annals of the Computation Lab.*, Harvard Univ., vol. 16, p. 146; 1948.

[2] R. D. O'Neal, *Annals of the Computation Lab.*, Harvard Univ., vol. 16, p. 260; 1948.

rules adopted by Tyler and O'Neal at the outset of their investigation were such as to eliminate or greatly degrade the inherent advantages offered by film as a medium for storing information. It is therefore not remarkable that these authors appeared to prefer the use of phosphor-coated strips to the use of film for the application they had in mind.

It is our purpose in this paper to recognize at the outset the capabilities and limitations offered by photographic media, and to consider which applications of these media to information storage may best exploit the unique capabilities of the photographic emulsion, while avoiding the more troublesome limitations associated with its use. It is apparent that ordinary photographic media do not lend themselves well to applications which require even moderately high speeds of writing, erasure or re-writing. The type of use that is appropriate to photographic media is then one characterized by the following conditions: (a) large quantities of information must be stored, (b) random access to any item of the stored information is needed and must be accomplished in a time which should be substantially less than a second, and (c) the stored information is either of permanent nature or else changes rather slowly. Fortunately, situations of this kind do exist. Indeed, it is one of the deficiencies of present information-processing machines that the capacity of the largest high-speed random-access storage systems now available is limited to a few million bits. If more information must be stored, then it is put on long magnetic tapes or into decks of punched cards, with a corresponding increase in the time required for random access.

II. Storage Density Achievable

As already mentioned, suitable emulsions will store marks and spaces representing digital information at a maximum information density in the neighborhood of 10^6 bits/mm². The linear density of information storage should probably be reduced by an order of magnitude or more in order to provide an adequate safeguard against difficulties of registration. This means that the resulting information density is in the range of 10^3 to 10^4 bits/mm². Depending upon the reading method chosen, it may be necessary to diminish this density further, but there is no necessity for reducing the information density to 8/mm² as suggested by Tyler and O'Neal, providing that the photographic medium is mounted on a backing which can be positioned more accurately and better reproduced than could the strip film they were considering.

Let us compare these figures for photographic media with current standards for magnetic recording. Engineering Research Associates, who have had extensive experience in the use of magnetic media for information storage, have standardized on 80 bits per inch (for return-to-zero recording) and use a track-to-track spacing of 1/16 inch. This yields an information density of about 2 bits/mm², between one and two orders of magnitude lower than that which can probably be realized by the use of photographic media. It is important to notice that the track-to-track spacing in magnetic recording is fixed at some rather large value, not by the difficulties of mechanical registration (as in the case of photographic recording), but rather by the far more fundamental difficulty that there will be crosstalk between adjacent channels if they are spaced too closely. There appears to be very little leeway remaining in the present standards of information-density for magnetic recording; in the case of photographic recording, the medium itself affords us several orders of magnitude of potential increase above the densities we are choosing to consider in this preliminary investigation. If we are clever enough, some of this potential increase in density will be realized through the development of improved techniques.

Another point worth noting when magnetic recording and photographic recording are compared concerns the rate at which the stored information can be read out. There is no lower limit on the reading speed using photographic media. The upper limit is not set by the medium, but rather by the auxiliary electronic circuits concerned with reading and processing the stored information. In the case of magnetic recording, on the other hand, a lower limit in reading speed is fixed by the fact that the signal is produced by changing flux in the reading head and therefore has a magnitude which, to the first order, is proportional to the reading speed. An upper limit to the reading speed is set, in the magnetic case, by various factors, of which the frequency response of the reading head is usually the most important. The highest practicable information rate at which magnetic media can be read is now between one and two times 10^5 bits/sec. Of course, there is no such upper limit on the speed of reading information stored in photographic media. This is a fortunate circumstance, since a given speed of physical movement of the storage surface past a reading "head" will yield an information rate which is directly proportional to the linear information density along the track being read. Since we are proposing to increase this linear information density by a factor between 10 and 100, a corresponding change in the rate at which information is read will enable the storage medium to be moved at comparable speeds in the two types of storage.

A relatively small, but perhaps important, increase in the density of information storage in photographic media may be achieved by the use of color photography rather than black-and-white. With existing commercial three-color emulsions, three bits of information can be stored in a single mark. Each reading station would involve color filters or dichroic mirrors to separate the three bits stored at each spot.

The reason three bits can be stored in the place of one lies in the fact that there are three dyes and filters known which are orthogonal in the sense that the integral of the dye and filter functions over wavelength is zero except for the three pairs. Clearly "*n*-color photography" would increase the capacity by a factor *n*. A large number of orthogonal filters can be made; e.g., the Billings type. It should be noticed that the demands of a digital photographic memory on the dye are not as stringent as those of color photography, because we are not concerned with faithfulness of reproduction of shades, etc. In fact, one can anticipate relaxation of the definition of orthogonality, to the extent that white light through the many combinations of dyes and filters must not be greater than 10 per cent of the intensity obtained by the correct pairs. Electrical circuits could readily discriminate between these two levels of output from the photocells.

The number *n* is thus determined by the half-width of the absorption spectrum of available dyes. It seems that all types of dyes have a half-width of about 1000 Å, determined by the number of vibrational levels in each electronic state. This number is large and about the same for all organic dye molecules or inorganic crystals. Thus it would seem that the maximum value of *n* is four, using visible light. Four-color photography would be very useful, either in pure binary or mixed binary-decimal recording.

III. Methods of Reading

There appears then to be no difficulty in storing all the information of immediate requirements in reasonable areas. The real difficulty lies in scanning such areas conveniently; and this is determined by the size of the field measured in units of resolvable lines.

In order to read out the information stored in a photographic medium we may either: (a) hold the emulsion stationary and move the reading head, (b) move the emulsion past a stationary reading head, or, (c) combine these two techniques in some suitable fashion. Examples of schemes involving each of these methods will now be given.

A. Flying-Spot Scanner, Two Dimensions[3]

If the photographic storage medium is mounted on a transparent backing, then the illumination of the storage surface by a fine spot of light whose position can be adjusted will be equivalent to moving a reading "head," provided that the photosensitive device serving as a pickup and its associated optical system are so arranged that the sensitive surface of the pickup element can be illuminated for any position of the scanning spot. This arrangement is exactly like that of a flying-spot scanner used in television broadcasting. A single flying-spot scanner can illuminate only as many stored bits of information as the ratio between its limits of beam motion and the diameter of its spot will allow. Since the image of the flying spot can be enlarged or condensed by optical means, the absolute spot diameter is unimportant, but the number of distinguishable bits of information will not be increased by such enlargement or reduction in the image of the flying spot.

Present-day cathode-ray tubes can resolve about 1000 distinguishable spots over the distance corresponding to one full line of scan. This means that a stationary photographic storage medium illuminated by a single flying-spot scanner can store, at most, about 10^6 bits of information. If the information is read off the emulsion at a megacycle rate, one second would be required to scan the entire contents of the stationary storage surface. The size of the area storing the one megabit which is accessible to a flying-spot scanner may be of any size. Since it is reasonable to photograph 30 lines/mm, our megabit could be stored in an area slightly greater than one square inch. If the access time of one second per megabit were acceptable for some specific application, the storage capacity of this system could be extended indefinitely by having many separate megabit "cards." All the advantages of sorting, collating, and coarse random access which are peculiar to cards could then be obtained. Alternatively, the megabits could be photographed in frames of strip film, and the advantages peculiar to tape storage systems could be realized.

The two-dimensional flying-spot scanner may not be practical, because the registration of the flying spot on any particular digit or line of digits depends upon the precision of control afforded by analogue devices producing the deflection voltages or currents. The problem is similar to that of constructing an address generator for the so-called Williams type of electrostatic storage system, but it is more difficult because 30 times as many "addresses" need to be generated for each coordinate.

However, when the logic of the information indexing is such that location by single address is impossible, and a sequential search is demanded, the requirements on the analogue deflection circuits are far less stringent than in the electrostatic storage system. It is relatively easy to start the spot off at the correct point, and by a suitable design of bit symbols and tracks, to keep the spot in the track by feedback systems. Examples of such systems are given later. Moving from one track to the next parallel one may be somewhat more difficult, and packing in this direction may have to be relaxed correspondingly.

B. Motion of the Emulsion Past a Stationary Reading Head

This reading scheme was the only one to be considered by Tyler and O'Neal.[2] They planned to have an optical system which would have a field of view encompassing an array of several information-storage positions in the focal plane of the reading system. Individual photocells were to be mounted behind apertures in a suitable mask, each aperture in the mask corresponding to one storage position on the photographic medium. At high information-densities in the medium, quite substantial magnification would be needed to get from the size of the tiny storage positions to the size of a two-dimensional array of reading devices. The use of phototransistors for reading enables the reading array to be made more compact, but it is still true that a considerable magnification is required.

---

[3] F. Roberts and J. Z. Young, *Proc. Inst. of Elec. Eng.*, vol. 99, series IIIA, no. 20, 1952; *Nature*, vol. 167, p. 231, 1951 and vol. 169, p. 963; 1953

However, there is no reason to suppose that a scheme of this sort would be impossible to realize. The main objection to it lies in the circumstance that the field of the reading head is only one bit, so that one must either provide one head per information channel on the moving medium (Tyler and O'Neal proposed to provide two per channel in order to check on the accuracy of reading); or else one must move a reading head, containing one or a small number of reading stations, in a secular and very precise fashion from track to track. Neither of these schemes is very attractive. The difficulty of the first can be indicated by a simple computation. Let us suppose that our photographic storage medium is mounted on the cylindrical surface of a drum 30 cm in diameter and that we have chosen a linear storage density of 30 bits/mm along any track. The total length of a single track will then be a little under 10^3 mm, and the total information in a single track will amount to 2.7×10^4 bits. To get a storage capacity of even a single megabit would require 36 tracks, each with its own photosensitive device, amplifier and associated circuitry. This is not a formidable requirement, but we have chosen a total storage capacity so low that it can be reached by magnetic storage devices. If we wish to store 10^7 bits or 10^8 bits, we shall have to provide hundreds or thousands of individual reading stations.

Moving a single reading head or a gang of reading heads from track to track along the drum may be useful in some applications, but this also appears to offer considerable difficulties. For any reasonable number of single reading heads ganged together, the access time for a store of 10 to 100 megabits would become quite long. Let us return to our earlier example. We saw that 36 tracks were necessary to store a megabit, so that a store having a capacity of only 10 megabits would involve 360 tracks. At a megacycle reading rate the rotational speed of the drum in our example would amount to about 2100 rpm, a quite reasonable speed. However, to search 36 tracks at this speed (as would be required by a 10-station movable reading head) would take a full second. Further, a store of 10 megabits does not exhaust the storage capabilities of a drum of reasonable size. Reasonably good machine work should permit the device transporting and registering the heads to index sufficiently well so that neighboring tracks could be placed on the surface of the drum at a spacing of 4 per millimeter. The 360 tracks comprising a ten megabit store would occupy 90 mm, or less than 5 inches, along the cylindrical surface of a drum about a foot in diameter.

It seems clear that the information-storage capabilities of photographic emulsions lend themselves to rotating drums of reasonable dimensions containing a total amount of information up to about 100 megabits. It seems equally clear that reading techniques derived so directly from those useful in magnetic-drum technology are far too slow to cope with the problem of rapid access to a total quantity of stored information of this size. New techniques better suited to the requirements of the new storage medium must be devised.

C. *Combination of the Flying-Spot Scanner with a Moving Storage Surface*

As we saw earlier, a two-dimensional flying-spot scanner viewing a stationary medium can distinguish one megabit at most. To extend the amount of stored information accessible to a single flying-spot scanner, we shall have to move the emulsion past the scanner. It is now appropriate to restrict the flying-spot scanner to motion in one dimension, which rather simplifies the problem of locating the spot by analogue means. We have then a class of devices in which the scanning spot is moved along a line perpendicular to the direction of motion of the storage medium. Let us make some elementary design considerations for a storage unit of this class. Consider a circular plate rotating about an axis passing through its center and coated on one side or the other with photographic emulsion. A flying-spot scanner can view the storage medium through a radial slit whose width is at our disposal. The use of such a slit eliminates the effects of spot size in the dimension across the slit. The information density along a track is then fixed by the width of the slit, and not by the size of the spot. No such consideration applies in the direction along the slit, however, so that we must have a spacing from track to track, and therefore a total number of tracks, determined by the resolving power of the scanning spot, rather than by that of the photographic medium. The resolving power of the scanning spot will be fixed either by the ratio of spot excursion to spot diameter, or else by the limits of reproducible control of the radial deflection of the spot. It is intended in this arrangement that the light from the flying-spot scanner be gathered by a suitable optical device and caused to fall on a single photoelectric reading head, independent of the position of the flying spot. Such an arrangement is shown schematically in Fig. 1, following page.

Let us make a few calculations regarding such a device. Suppose that the disk is 50 cm in diameter and that we use a slit 5 microns wide. Using a pair of marks to represent a bit and allowing a factor of two for safety, this permits the storage of 50 bits/mm along any track. The average track near the edge of the disk is about 1500 mm long, and would thus contain 7.5×10^4 bits. Let us suppose that control of the radial deflection in the flying-spot scanner permits us to distinguish with certainty any one of 64 tracks; this is a slight extension of Williams-tube address-generator

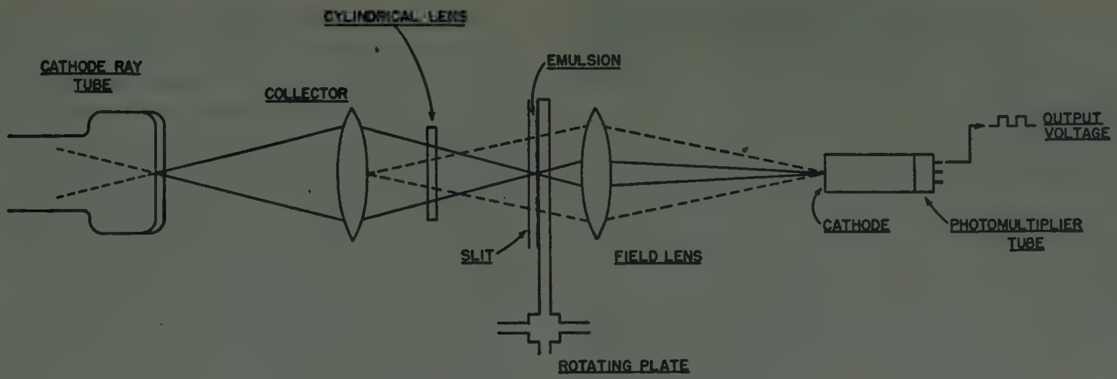


Fig. 1—Flying spot scanning a rotating disk.

techniques now in common use. The disk storage device defined by these parameters would then have a total capacity of 4.8 megabits. The use of color would multiply the storage capacity by 3, bringing it to 14.4 megabits.

Reading through the entire stored information at a megacycle rate with a single head (or a single three-color head) would require nearly 5 seconds, so that this device is most useful when it is employed in conjunction with a sort of "index" which specifies the address of the information wanted. Once this address is known, the flying-spot scanner can select the desired track in a very few microseconds. The rotational speed corresponding to a reading rate of one megabit per second is 13.3 revolutions per second or 800 rpm. This is a reasonable speed for a device of such size.

The access time of a rotating store is determined by the speed of rotation, which has to be kept below a critical value which, for glass, corresponds to about 1000 ft/sec peripheral velocity. Parallel reading by a number of independently controlled reading stations around the circumference of the disk, or duplication of the information on the disk, will diminish access time and speed up the rate at which information can be taken from the store.

It appears that the major design difficulty presented by a storage device in which the photographic medium moves past a reading head may lie in minimizing the mechanical irrgularities in the motion of the medium; these must produce a maximum displacement smaller than the size of the bit symbol. Vibrations of the disk as a circular membrane will move the track out of the plane of focus, eccentricity of a track or radial vibrations will be troublesome, and angular vibrations or non-uniform rotational speed will interfere with bit identification. Calculations of the expected performance of a $\frac{3}{8}$″ glass plate rotated on air bearings make it appear that no difficulties of these sorts will be experienced.

D. High-Capacity Storage Unit with Integral Index

In a large class of practical information-storage applications (directories, dictionaries, catalogues, etc.), the stored information is accompanied by a much more compact index. This index is often integral with the stored information, as for example in a dictionary, where the words beginning and ending each page are entered at the top of that page.

The inspection of such an index is governed by the fact that the index is not a dense set of all binary numbers having a given number of digits. Instead, the index is usually highly redundant in having many more digits (say n) than are necessary to describe the number of items $N \ll 2^n$. Thus a given "address" will not serve to direct the reading head to the proper location in the index; rather, the index must be scanned in an extensive, if not exhaustive, fashion.

We have already noticed that storage systems having total capacities in the 10 to 100 megabit range cannot be completely read in microsecond time intervals (which are often wanted), even at the rates of reading in the megabit-per-second range permitted by photographic storage, without requiring an undesirably large number of individual reading heads. In many problems which demand storage systems of this size, fortunately, it is possible to provide a greatly condensed index which can be scanned in order to determine the location of the information that it is desired to read in detail. A well known example of precisely this (and, incidentally, one involving a photographic storage medium) is Vannevar Bush's Rapid Selector. Documents are photographed on microfilm and beside the image of each document on each microfilm is placed a digital code-group identifying the contents of the frame. The reel of film containing the frames is then run through a reader which reads only the index information; when an index entry of interest appears, the information stored in the corresponding frame is photographed onto a fresh film by techniques of flash photography. A complete search through all the index entries contained in a reel then results in producing a new reel of film containing only those frames whose information is of interest in connection with the subject of the search.

A philosophically similar technique appears to be possible using the combination of flying-spot scanner and rotating storage medium which we have been considering. Suppose that the information stored on the periphery of a photographic drum is laid down, not in a number of circular channels parallel to one another, but instead in a series of lines which run parallel to one another and nearly parallel to a generator of the surface of the cylinder (Fig. 2). The angle between one of these lines of information and the generator will be the angle whose tangent is the ratio of the peripheral speed of the cylinder to the linear speed of the flying spot. Thus, when the flying spot scans along the axis of the cylinder at its standard rate, it will follow along one of these tracks on the surface of the drum. When the tracks are packed as closely together as the resolving power of the flying-spot scanner will allow, the time required for the execution of a scan along one track and the return of the spot to its starting position would be sufficiently long so that adjacent tracks could not be scanned in the same rotation of the drum. Let us make some preliminary design considerations to show this.

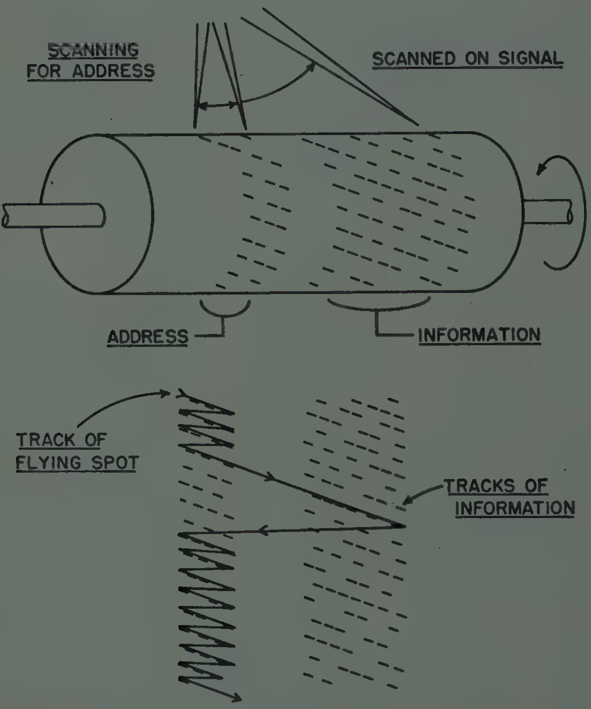


Fig. 2—Arrangement of information with integral index on a rotary drum.

Let us suppose that the flying-spot scanner can resolve 1000 bits along a single scan. If this scan is executed at a speed corresponding to a reading rate of one megabit/sec, the total time it will occupy will be 1000 μsec, and a few more microseconds will be needed for the flyback to the starting point. Let us suppose that our drum is 30 cm in diameter, or 944 mm in circumference, and is rotating at a speed of 2000 rpm. Under these circumstances, the surface of the drum will move 31 mm during the time of approximately one millisecond that is occupied by the scan of a complete line and the flyback. Clearly, we wish to be able to put lines of information closer together than this on the surface of the drum. The lower limit to the distance from one track to its neighbor will be set by the resolving power of the flying-spot scanner, unless we make use of a slit in this device. Let us suppose that we choose to put the tracks one millimeter apart. The scan of an entire line will then cause us to miss about 31 tracks following the one which we choose to read in full.

Now suppose that we have a scanning schedule which reads only the early part of every track, executing a flyback and restart on the next line just in time to catch that line as it comes into the field of view of the flying-spot scanner (Fig. 3). In the example we have chosen, the total time available between the appearance of the nth track at the scanner and the appearance of the $(n+1)$th track is 35 microseconds. If we allow 5 microseconds for flyback (a generous allowance in view of the short distance to be traversed), we are then able to read the first 30 bits of every line consecutively. This group of 30 bits at the beginning of each line can then be used to indicate the contents of the following line (not the line containing the 30 bits, but the one after it). We can then decide whether or not we are interested in reading the line which contains the index designation we are currently reading. When the line which is to be read is located, the early flyback of the scanner is inhibited, and the scan is continued to the end of the line of interest. This occasions the missing of the next 31 lines, but for most types of storage search this is no disadvantage. Observe that the entire index is searched exhaustively about 33 times per second, and that random access to any line of stored information is available with a maximum delay of 30 milliseconds.

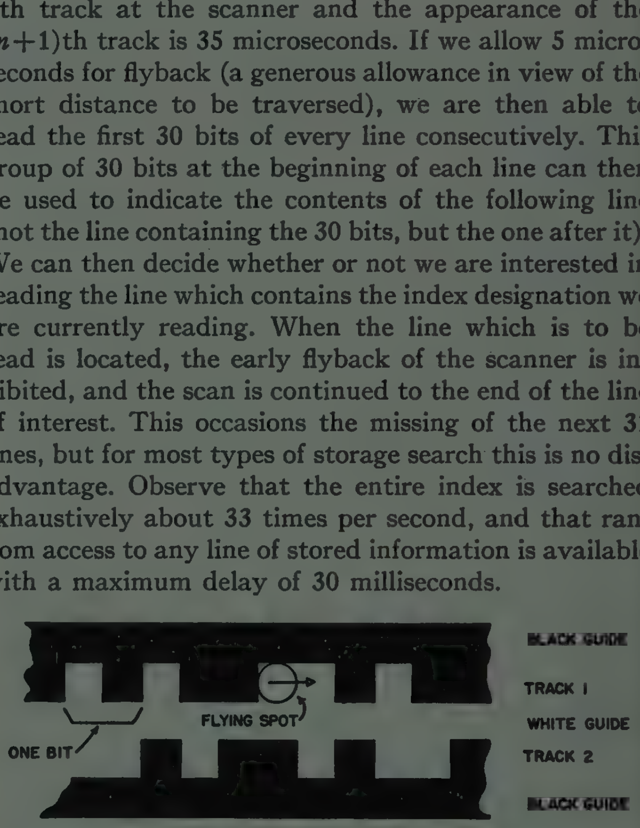


Fig. 3—Design of bit symbols and border by which the flying spot can be kept in the track by feedback.

Let us now calculate the capacity of this storage system. We have assumed that each track contains 1000 bits and that the tracks are spaced one millimeter apart on the periphery of the drum. Since the circumference is 944 mm, we have achieved a random-access store of about one megabit (with color, 3 megabits). Despite its favorable random-access feature, this type of storage device has a disappointingly small total capacity. The capacity can be raised, however, by suitable demagnification of the flying-spot scanner, which would permit a closer packing of tracks on the surface of the drum without affecting any of the other features of the design except rotational speed. A 10-megabit store might be realized very readily in this fashion.

If larger total storage capacities are wanted, one drum of the type described might be used as an index drum capable of choosing among a multiplicity of storage drums or disks associated with it, and in the case of the chosen storage drum indicating the track containing the information of interest. The storage devices controlled by such an index drum might be of the general sort described above under Section III-C.

The primary limitation on the storage capacity attainable by this scheme lies in the spacing necessary from one track to its neighbor on the surface of the drum. It may be possible to achieve closer spacings if curve-follower techniques are used to cause the spot to follow the line it has commenced to scan. This might be done, for example, by a scheme of the following sort (see Fig. 3). Let us suppose that each bit recorded occupies the space which considerations of over-all system resolving power would assign to a pair of distinguishable marks. The digit zero could then be represented by black followed by white, and the digit one by white followed by black. Digits would be recognized by the "non-return-to-zero" technique often used in magnetic recording. On the average, each bit would be grey. If there is now a white border at the top of the track and a black border at the bottom, then wandering of the spot away from the track would be attended by a secular increase or decrease in the average level of transmitted light. The sense of the deflection correction required to bring the spot back to the center of the track would be indicated by the sense of this change in light travel. Filling the spaces between neighboring tracks with alternate black and white strips would require an inversion of the sense convention between each track and its neighbor; this should provide a valuable check on the fact that no track has been missed. The fact that when the spot is in the track there is a strong signal at twice the bit frequency might also be used as an additional means of control. It is clear that a self-tracking scheme of the sort described could also be used in color emulsions.

In order to keep sufficiently square in shape the pulses that are produced in reading, the minimum size of the bit symbol should be between 10 and 100 times the limiting resolving power of the photographic medium used. This suggests that fine structure purposely introduced into the bit symbol could be used to improve reliability: for example, by distinguishing a written zero from the lack of information, by distinguishing genuine symbols from the effects of dust and scratches, etc. Alternatively, fine structure of the bit symbol might enable the use of a ternary- or higher-base set of symbols. In this last connection, the exploitation of the grey scale of a photographic emulsion might be considered. In general, it is not advisable to use an analogue property such as this for the representation of digits, but the latitude afforded by silver-halide emulsions might be wide enough to permit two or more grey levels to be reliably distinguished. Even if this could not be done, the grey scale of the photographic medium might be used as a check against error.

IV. Combination of Photographic and Magnetic Storage

So far in this discussion, we have ignored the circumstance that the writing of information into photographic media is at best a slow process, involving, as it does, the exposure of the emulsion and subsequent chemical development and fixing. When the information that is to be stored in the drum is of a permanent character, this is no great disadvantage, for a complete file of the stored information can be produced once for all in photographic form. In many practical applications demanding large-capacity rapid-access information storage, however, it is necessary to make periodic alterations in the stored information. Sometimes the information which is to be stored can be divided into two parts on the basis of its permanence. In a machine designed to keep inventory records, for example, the designations of the items comprising the inventory are either permanent or else change very slowly; the information representing these catalog descriptions is thus suitable for storage on photographic media. The quantity in stock of each item is altered whenever items are drawn from or added to stock. The numbers representing these quantities will therefore change far too rapidly to enable them to recorded on photographic storage media.

In an application such as that of the inventory machine just mentioned, we notice that the information describing the items in stock is usually several times as voluminous as the information specifying how many items of each sort are on hand. The former information is permanent or quasi-permanent; the latter is subject to change. This is clearly a case which can be dealt with by associating a photographic storage system with a magnetic store of smaller capacity. Descriptions of items can be carried in the photographic store, together with an address for each item which specifies the location on the magnetic drum at which is stored information regarding the quantity on hand of the item in question. Since the magnetic storage system lends itself to rapid erasure and re-writing, the numbers specifying the quantities in stock can be altered as rapidly as desired; since the catalog descriptions of the items stocked do not alter over any reasonable period of time, they can be carried in the more permanent photographic storage.

There is at least one other situation which requires associating a magnetic storage system with a photographic one. We noted that the catalog description of the items carried in the inventory machine is subject to some change, even though this change is slow. If it happens that changes in the catalog occur at intervals more frequent than those which justify the preparation of a new photographic surface containing new information, then we can make use of the following arrangement. We can associate with the photographic storage system (in addition to the magnetic drum which carries information on quantities in stock) another magnetic drum on which we record the new or altered catalog descriptions which have come along since the last edition of the photographic store was prepared. Any catalog reference demanded of this combined storage system will then be routed first through the magnetic drum containing the new or altered catalog information. If the item in question is represented by an entry on this magnetic drum, then the address of the quantity designation on the other magnetic drum will be secured from this first magnetic drum. If no entry regarding the item in question is found in the magnetic drum bearing the catalog addenda, then the inquiry is routed on to the photographic store in order to find the address of the storage location bearing information on stock in hand.

It is clear that the logical association of a necessarily smaller magnetic storage system with a very large photographic store will remove much of the limitation that is occasioned by the difficulty of writing and erasure in photographic media. Other practical applications of this technique of dual storage are very numerous, including, for example, that of maintaining a reservation-file machine for a public carrier such as an airline or a railroad.

V. Writing Information into a Photographic Store

The preparation of a photographic emulsion bearing digital information is admittedly a slow process; for this reason, the demands of speed placed on the writing apparatus need not be severe. However, a large number of marks must be entered on the emulsion in a controlled fashion. Presumably, a human operator will originate through a manual process all of the information that it is desired to store. It is therefore appropriate to record the information on punched cards as the first step in the writing process. Once this is done, conversion of the primary information to binary form and its rearrangement into the geometrical sequences desired for recording in the photographic store can be accomplished mechanically at reasonably high speed through the use of standard punched-card equipment.

The actual preparation of the photographic store is similar to, but less exacting than, the photographic preparation of reticles, an art which is highly advanced. Geiser,[4] for example, describes the preparation of a circular track 440 mm long containing 8192 binary symbols. This density of 18 lines/mm is below that contemplated in the present paper, but there appears to be no limitation in writing technique or in emulsion resolving power which would prevent an increase of one order of magnitude in linear storage density.

In many applications, the fact that contact printing will enable the duplication of photographically stored information is of great value.

VI. Conclusions

It seems apparent, even on the basis of the rather superficial consideration we have given to the use of photographic media for information storage, that the proper exploitation of photographic techniques should yield useful storage systems having total capacities in the range from 10 to 1000 megabits of information. With proper schemes for indexing, it should be possible to gain random access to any entry in such a store in a time comparable to that which is needed to look up a random address on the sort of magnetic drum that is in common use today. There seems little doubt that these potential capabilities of photographic storage, when fully realized by further research and development, will put into our hands a new type of device. The absence of such a device is now severely limiting the application of modern computing and information processing techniques to practical non-numerical problems, as those encountered in the large scale clerical work of business and the industrial control of industry.

---

[4] Ralph D. Geiser, *Photo. Eng.*, vol. 4, p. 1; 1953.

◆

The Logical Principles of a New Kind of Binary Counter*

WILLIS H. WARE†, SENIOR MEMBER, IRE

Summary—**In a shifting register or binary counter, there is a real logical requirement for a short term or temporary storage facility. In the counter, this occurs during the interval in which the actual count process is occurring. A positive memory counter is described in which this auxiliary storage is provided by elements which have the same time-indefinite storage property as the principal storage elements of the counter. This leads to a device which has two ranks of storage elements: the "true" and the "false" rank. The behavior of the single-stage and multiple-stage counter of this kind is derived, and the rules of formation for all numbers appearing in the true and in the false ranks are derived. The basic device is then generalized to one with four modes of operation, and the behavior and rules of number formation are discussed. Example of the application of the extended counter to a computing machine is given.**

Introduction

In some types of digital computing circuits, it is logically necessary to provide a short-term storage facility which is quite independent of any long-term storage facility which the circuit may otherwise possess. For instance, the toggle elements which constitute a shifting register contain a long-term storage property which enables them to hold information for as long as desired. Yet, at the instant of shifting, each toggle must accept new information from the toggle standing on one side of itself, but eject old information to the toggle standing on the other side of itself. These are conflicting requirements for the duration of the shift and hence, there is a very real logical requirement for a transient memory which can hold information for an interval which is of the order of the width of the shifting signal.

This same problem again arises in a binary counter. Quiescently, the toggles or other storage elements of the counter hold the accumulated count. However, during the interval of the actual count, and any ensuing carries within the several stages of the counter, a toggle, in one form of counter, may be called upon to accept new information from the stage on one side of it, but to provide old information to the stage on the other side of it. In another form of counter, something must remember the previous state of a toggle so that an incoming carry signal *knows* which way to turn it. In any arrangement, however, a sufficiently close examination will reveal that there is an unavoidable logical requirement for a transient memory which can retain information for a time related to the width of the signal which causes the count and perhaps related to the carry time down the counter.

For that type computer which is tied to absolute time in the sense that a master clock provides all activating signals within the machine at known intervals, this transient memory can and has been provided by delay lines, either stray or explicit capacitance, and by inductance. In such a design, the relation of the time constants of the circuit to the width, and the rise and fall times of the input signal, and of the signals generated within the counter proper is of utmost importance. In another type of machine however, which is in no wise tied to absolute time but which performs operations at a rate which is determined only by its own time constants and by its environment,[1] it is decidedly risky to depend upon elements with time-limited storage.

There has arisen a design philosophy for this type of asynchronous machine which provides the required auxiliary storage in elements which are like the principal storage elements; hence, the associated storage has the same time indefiniteness as the primary storage. With each primary storage element, there is associated a secondary element whose only function is to remember the state of the primary element during any interval in which it is changing or is in a state of change.[2] In a practical realization this requires that for every element which is present to store a bit of information, there must exist a second element which knows the state of the first; and which is, itself, not in a state of change in any interval throughout which the first element is changing or is otherwise unsettled. This style of design has been applied to shifting registers and to binary counters, and it is the purpose of this paper to explore the logical behavior and possibilities of a binary counter constructed in this way.

The Single Stage Counter

The behavior desired in a single stage binary counter is simple to describe: by the end of each input signal the storage element shall have changed to the opposite state. If a toggle circuit happens to be used as the storage element, it shall alternate normal and abnormal states, and since most circuit realizations of a binary counter use a toggle of some form—Eccles-Jordan, Schmidt, dynamic, etc.—the following arguments are phrased in terms of the toggle as the storage element. It

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, April 27, 1953. (This paper is part of a dissertation submitted in March, 1951, to the Dept. of Electrical Engineering, Princeton University, in partial fulfillment of the requirements for the Ph.D. degree.)

† The Rand Corporation, Santa Monica, Calif.

[1] The machine at the Institute for Advanced Study, Princeton, N. J., is an outstanding example of this type.

[2] This principle was first suggested by J. H. Bigelow, of the Electronic Computer Project, Institute for Advanced Study, Princeton, N. J.

is easily seen that the logical principles evolved are general and may be applied to any form of storage element and its associated gating technique.

In the "positive memory" style of design, there is, as previously indicated, two toggles in the single stage counter. Let one of these be called the "true toggle"; the other, the "false toggle". (The significance of these names will be more apparent later on.) It is required in the positive memory technique that no toggle be altered in state unless its information is elsewhere stored in a second toggle. Accordingly, the first act in causing this pair of toggles to behave as a counter is to establish a gate such that the true toggle can communicate its information to the false toggle. Since it is then desired that the true toggle alternate its state, there must exist a gating path which transmits the 1's-complement of the information in the false into the true toggle.[3] Hence if these two gate paths are caused to operate alternately, the state of the true toggle will reverse and it will, in fact, behave as required for a single stage binary counter. Let the input signal consist of two time sequenced signals and a count cycle consist of a true-to-false transfer followed by a false-to-true transfer.[4]

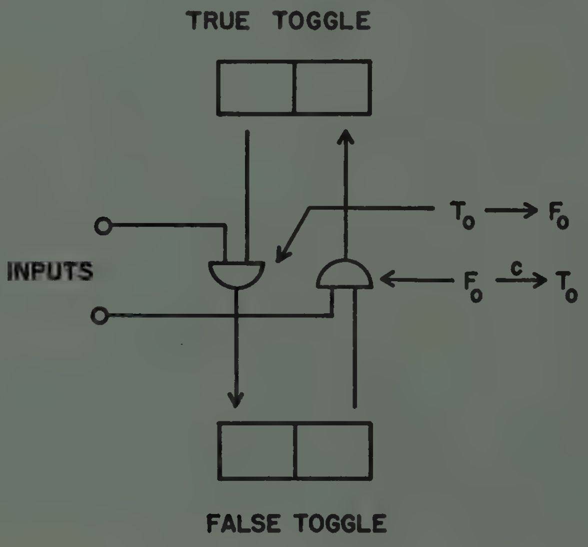


Fig. 1—The single stage positive memory counter.

Notice that the false toggle also alternates although it is not a priori clear that the false and true pair in other stages of a many-stage counter will behave similarly. Fig. 1 summarizes this argument and also indicates the symbology for later use. T_i means the contents of the true toggle of the ith stage where i commences at 0; therefore, if the counter is considered to be handling the binary integers, the ith stage contains the coefficient, in a positional notational representation of the number in the counter, of 2^i. $T_i \rightarrow F_i$ means that the contents of the true toggle of the ith stage shall be transferred without alteration to the false toggle of the ith stage; $F_i \xrightarrow{c} T_i$ means that the 1's-complement of the information in the ith false toggle shall be transferred into the ith true toggle. The divided rectangle indicates a toggle; and the circular segment with several inputs and an output, a logical and-gate.

The Many-Stage Counter

With the requirements of the 0th stage of a counter in mind, what can be deduced about succeeding stages of a several stage counter? First, the positive memory philosophy requires that there be two toggles per stage, and certainly there will have to be within any stage a set of gates communicating from false to true, and a set from true to false. One of these will have to be direct and one will have to complement; but now, however, these gates must take cognizance of carry information from the previous stage. From the properties of the binary number system, it follows that:

(a) If the $(i-1)$st stage changes from a 0 to a 1, then there will be no carry and no change need be made in the contents of the ith stage, whether it contain a 0 or a 1.

(b) If the $(i-1)$st stage changes from a 1 to a 0, then there will arise a carry and the state of the ith stage must be changed. If it had been 1, it must be changed to 0, and vice versa.

It has already been indicated that false may not be changed at the same time as true; hence, since requirement (b) demands that T_i shall be changed when T_{i-1} changes from 1 to 0 (i.e., when T_{i-1} is 0),[5] it follows that F_i will have to be changed when T_{i-1} is 1. Thus, the way in which carry information controls the intrastage gating has appeared. The rules for the gating in the ith stage of the counter are then:[6]

$$\begin{aligned} &\text{If } T_{i-1} = 0, \text{ then } F_i \xrightarrow{c} T_i \\ &\text{If } T_{i-1} = 1, \text{ then } T_i \rightarrow F_i. \end{aligned} \tag{1}$$

It has been assumed that the complementing occurs in the $F-T$ gating, as was assumed in the discussion of the single-stage counter. Clearly, since a false toggle only supplies information to the true toggle of its own stage, and does not supply carry information to the next stage, it is immaterial where the complementing occurs. It can be in the $F-T$ gate[7] or in the $T-F$ gate equally well; if there is reason to be so, it can be in different places in the various stages. The only effect is to change 1's for 0's and 0's for 1's in the numbers which appear in the false toggles. The above rules may be considered to apply to the 0th stage as well, if the conditions due to the carry are removed:

---

[3] Throughout this paper, "complement" where unqualified shall be taken to mean "1's-complement."

[4] Certain engineering details of positive memory counters, a more detailed description of the experimental model, a discussion of resolution time of this type counter and of the various ways in which the input signals may be handled, will be presented in a companion paper now in preparation.

[5] It is not necessary, logically, to recognize the change from 1 to 0; it is sufficient to know that the state is 0.

[6] In any set of rules of this kind it must be realized that any gating possibility not specified does not exist; i.e., for $T_{i-1}=0$, there is no true-to-false gate or gate operation.

[7] $F-T$ is a contraction of false-to-true.

$$F_0 \xrightarrow{C} T_0$$
$$T_0 \mapsto F_0. \qquad (2)$$

These arguments are summarized in Fig. 2. Here the inputs to the and-gates are assumed to be enabled for the condition shown, and the output of an and-gate is assumed to exist when each input condition is satisfied. The effect which the output of each and-gate causes is also indicated.

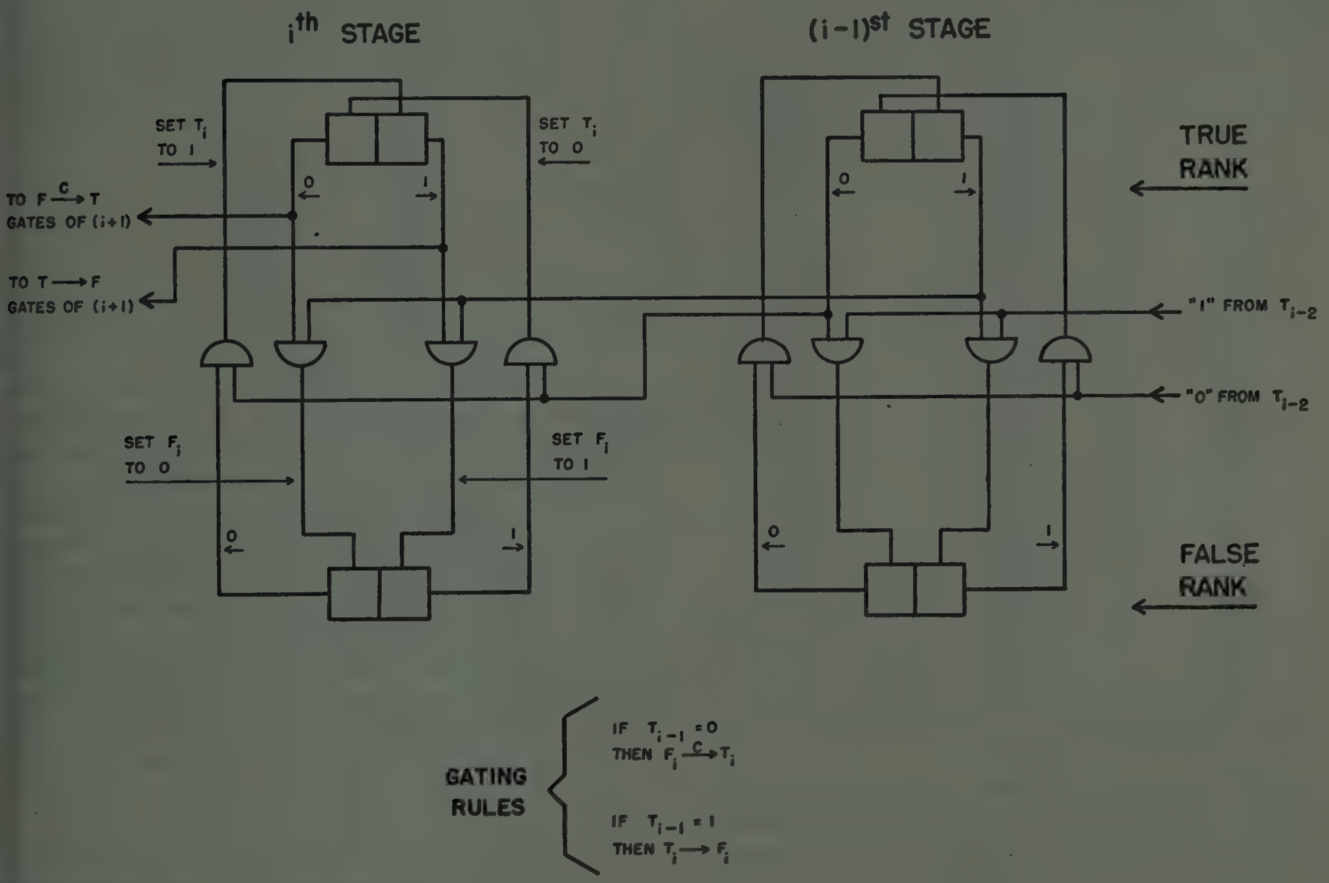

i^{th} STAGE
$(i-1)^{st}$ STAGE
SET T_i TO 1
SET T_i TO 0
TO $F \xrightarrow{C} T$ GATES OF $(i+1)$
TO $T \longrightarrow F$ GATES OF $(i+1)$
0
1
TRUE RANK
"1" FROM T_{i-2}
"0" FROM T_{i-2}
SET F_i TO 0
SET F_i TO 1
FALSE RANK
GATING RULES
IF $T_{i-1} = 0$ THEN $F_i \xrightarrow{C} T_i$
IF $T_{i-1} = 1$ THEN $T_i \longrightarrow F_i$

Fig. 2—Interior stages of a positive memory counter.

The True and False Numbers

The rules which have just been deduced permit the construction of the numbers which will appear in the false rank[8] of the counter. It is clear since the properties of the number system have determined the interstage carry connections that the numbers which appear in the true rank will be the sequence of binary integers and hence the name "true." Since the false numbers are generated from the true numbers by a set of unambiguous rules, it follows that the false numbers will be unique and in one-to-one correspondence with the binary integers. Further, since they are generated from a series of numbers which are a sequence of binary integers, the false numbers will most certainly not be a sequence of binary integers; hence the name "false."

The set of rules (1) say in effect the following: If the $(i-1)$st true digit is a 0, then the ith false and true digits are opposite; but if the $(i-1)$st true digit is a 1, then the ith false and true digits are alike. Hence, given any number in the true rank, the number which corresponds to it and must appear in the false rank can be easily constructed. For the sake of argument, consider a 5-stage counter $(0 \leqq i \leqq 4)$ and assume the binary point to be at the right of each number; let the initial state of the true rank be 00000. In the 0th stage, the last operation to happen was the transfer of the 1's-complement of false into true. Hence, F_0 must be 1. Similarly, since T_0 is 0, T_1 and F_1 must be opposite, and therefore F_1 is also a 1. Continuing in this way, it is found that the false number dual to the true number 00000 is 11111. In this way, Table I may be constructed.

There are several interesting properties about this table. The entries in the 0th column change every count; the entries in the 1st column change every 2 counts; and in general, the entries in the jth column change every 2^j counts. Further, the initial number of 1's at the head of each column is: a single 1 for the 0th column, a single 1 for the 1st column, two 1's for the 2nd column, four 1's for the 3rd column; and in general, except for the 0th column, 2^{j-1} 1's for the jth column. These observations are sufficient to extend such a table as far as desired.

---

[8] "Rank" is a group or row of toggles.

TABLE I

TRUE AND FALSE NUMBERS FOR A SELF-INSTRUCTED ADDING COUNTER

Count and Decimal Equivalent if the True Number	True Rank	False Rank
0	00000	11111
1	00001	11100
2	00010	11001
3	00011	11010
4	00100	10011
5	00101	10000
6	00110	10101
7	00111	10110
8	01000	00111
9	01001	00100
10	01010	00001
11	01011	00010
12	01100	01011
13	01101	01000
14	01110	01101
15	01111	01110
16	10000	01111
17	10001	01100
18	10010	01001
19	10011	01010
20	10100	00011
21	10101	00000
22	10110	00101
23	10111	00110
24	11000	10111
25	11001	10100
26	11010	10001
27	11011	10010
28	11100	11011
29	11101	11000
30	11110	11101
31	11111	11110
0	00000	11111

There is also a way of arithmetically forming the false number dual to a given true number. Table II gives the decimal equivalents of the first few false numbers. Notice many of these are given (decimally) by the rule $(31-3N)$ where N is the decimally expressed count. Observe that F_0 is $1-T_0$; and further, that to obtain any F_i, add modulo 2, the digits of T_i and T_{i-1}, and then complement with respect to 1. Since counting modulo 2 amounts to discarding any carries which may arise, the false number may be found by the following rules:

(a) T_i and T_{i-1} can be added together by shifting the true number one place to the left (i.e., doubling it), and performing a stagewise modulo 2 addition.

(b) Construct the 1's complement of the number resulting from rule (a); i.e., in the case of a 5-stage counter, subtract the number formed by rule (a) from 11111 (decimal 31).

Shifting the true number (N) one place to the left generates $2N$ and if there were no carries generated in the stagewise addition, rule (a) would form $3N$. However, in general there will be carries; hence the addition performed by rule (a) will yield a number N', which is smaller than $3N$ by the sum of these lost carries:

$$N' = 3N - \Sigma\,(\text{lost carries}).$$

Now the number appearing in the false rank is $31-N'$ or $31-[3N-\Sigma\,(\text{lost carries})]$ or finally:

$$31 - 3N + \Sigma\,(\text{lost carries}). \tag{3}$$

TABLE II

DECIMAL EQUIVALENTS OF THE FALSE NUMBERS

Count	True Number	False Number	Decimal Equivalent of False
0	00000	11111	31
1	00001	11100	28
2	00010	11001	25
3	00011	11010	26
4	00100	10011	19
5	00101	10000	16
6	00110	10101	21
7	00111	10110	22
8	01000	00111	7

Now, it is clear why some false numbers are correctly given by the rule $(31-3N)$, and why others are not. Lost carries will occur only when two 1's stand adjacent in the true number; this occurs for the first time at the third count (00011). When T_0 and T_1 are added to form the digit F_1, there is a carry into the second stage of value 4; since this is discarded, it is expected that the false number will be 4 larger than $(31-3N)$. This is precisely the case, $(31-3N)$ being, for N equal to 3, 22; and the false number is found to be 26—exactly 4 too large. The next cases are 6 (00110) and 7 (00111) and again their false numbers are out of step by the correct amount—8 for the count of 6 and 12 for the count of 7.

EXTENDED POSITIVE MEMORY COUNTER

The Generation of a Dual Number. It is not uncommon in digital computing applications to require a counter to begin counting from some arbitrary number within its range. Herein lies the great importance of the dual numbers. Since they are unique, not only must the arbitrary starting number be inserted into the true rank, but the false number dual to it must be inserted into the false rank. Otherwise the counter will fail to operate properly. Rules for generating a false number dual to a given true number easily follow from the previous discussion.

In the 0th stage, since the information is complemented in the false-true transfer, F_0 must be the complement of T_0. An interior stage containing a 1 in the true toggle will have enabled a direct (as opposed to complemented) transfer from true to false in the following stage; and hence if T_{i-1} is 1, then F_i and T_i are alike. Similarly if T_{i-1} is 0, it will have enabled a complemented transfer from false to true; and hence if T_{i-1} is 0, then F_i must be the complement of T_i. More specifically,

$$\begin{gathered} T_0 \overset{c}{\longrightarrow} F_0 \\ \text{If } T_{i-1} = 0, \text{ then } T_i \overset{c}{\longrightarrow} F_i. \\ \text{If } T_{i-1} = 1, \text{ then } T_i \longrightarrow F_i. \end{gathered} \tag{4}$$

It is seen that these rules are similar to those describing the counting action of the system. Notice, however, that not all of the gates required to mechanize the formation of a dual are present in the counter which has only a counting property. In particular, the set described by:

$$\text{If } T_{i-1} = 0, \text{ then } T_i \overset{c}{\longrightarrow} F_i$$

and (5)

$$T_0 \overset{c}{\longrightarrow} F_0$$

is not required for simple counting, and must be added to the counter if it is desired to start it from an arbitrary origin; note that this gating must be disabled during counting.

It will be observed in this process that there is present nothing similar to a carry. Once a number exists in true, it is completely determined what must exist in each stage of false; the state of F_i is completely determined once T_{i-1} and T_i are fixed. This means that the digits of the false number need not be constructed sequentially, but may be constructed simultaneously or in arbitrary order. This, in turn, implies that the whole set of dual-constructing gates may be operated by a signal whose width is only sufficient to cause a transfer into a toggle; the width of this signal is in no way influenced by the carry time down the length of the counter.

Dynamic Interior Gating. In the initial discussion of the interior gates (those in all stages except the 0th), it had been implicitly assumed that they were static gates in the sense that the output signal appeared as soon as the last input condition was met—no specific activate signal appeared as an input condition of any and-gate. It immediately follows from the previous argument that this need not be the case. If desired, all interior true-false gates may be dynamic in the sense that a specific action signal appears as an input condition to each and-gate. Such "separately-instructed" gating as opposed to the original "self-instructed" gating will be useful later.

Separately-instructing the false-true interior gates, however, is a different story. Certainly the F_0 to T_0 transfer will change T_0. This may enable or disable a false-true gating operation in stage 1, depending upon the previous history of stage 0. If it does enable an $F-T$ operation in stage 1, T_1 will change, and it may enable or disable an $F-T$ operation in stage 2, again depending upon the previous history of stage 1. Thus it is seen that the carry propagation process is associated with the gating operation from false to true. Hence, it is strictly necessary that this gating must proceed sequentially through the stages, starting at stage 0. If the interior $F-T$ gates are self-instructed, this happens automatically. If, however, they are separately-instructed, the action signal must last longer than the longest carry time of the counter; it is not determined by the transfer time into a toggle as was the separately-instructed $T-F$ action signal.

TABLE III

TRUE AND FALSE NUMBERS FOR A SEPARATELY-INSTRUCTED ADDING COUNTER

Count and Decimal Equivalent of the Numbers in True	True Rank	False Rank
0	00000	11111
1	00001	11110
2	00010	11101
3	00011	11000
4	00100	11011
5	00101	10010
6	00110	10001
7	00111	10100
8	01000	10111
9	01001	00110
10	01010	00101
11	01011	00000
12	01100	00011
13	01101	01010
14	01110	01001
15	01111	01100
16	10000	01111
17	10001	01110
18	10010	01101
19	10011	01000
20	10100	01011
21	10101	00010
22	10110	00001
23	10111	00100
24	11000	00111
25	11001	10110
26	11010	10101
27	11011	10000
28	11100	10011
29	11101	11010
30	11110	11001
31	11111	11100
0	00000	11111

If now, the true-false interior gates are separately-instructed it might be expected that the numbers appearing in the false rank would be different. In particular what will happen is that certain true-false gating combinations will be set up, but will not occur until a specific action signal appears. There is no reason to make this specific action signal different from the one which causes the $T-F$ gating in the 0th stage; hence it is expected that the digits of columns 1 through 4 in the false numbers would translate one count down with respect to the digit of column 0. Table III may be built up in this way from Table I; or the rules may be followed through as for Table I, taking into account that certain gating actions are postponed one count.

Separately-Instructed Duals. Consider the effect of applying the following set of rules to any number in true:

$$\begin{aligned} &T_0 \to F_0 \\ &\text{If } T_{i-1} = 1, \text{ then } T_i \to F_i. \\ &\text{If } T_{i-1} = 0, \text{ then } T_i \xrightarrow{C} F_i. \end{aligned} \tag{6}$$

These rules are exactly like those previously determined for constructing a dual (4) except that the input stage is now a direct instead of a complemented transfer. Notice that the first two of these rules are those for counting. Applied to 01100, they yield 01010 in false which in Table III is not the false number dual to 01100 but the false number which will be dual to the number next after this, namely 01101. This means, that if all the interior $T-F$ gates are separately instructed and operated synchronously with the $T-F$ gate in stage 0, the complete set of dual-constructing gates can be operative at all times; they need not be disabled during counting. This is an important simplification in the operation of the counter. Now, to start at an arbitrary point, it is only necessary to insert the beginning number (N) in the true rank. The first operation in the first count cycle is a $T-F$ transfer which immediately creates in the false rank, the number which is the dual of ($N+1$) and is therefore exactly what belongs in false in order that the $F-T$ transfer of the first count cycle will form ($N+1$) from (N) in true.

The Subtracting Counter. Another feature which is often convenient in digital equipment is to be able to count backward, or to subtract. In the 0th stage of the counter thus far developed no change need be made, since in the binary number system, adding or subtracting in the 0th place yields the same result. In the interior stages, however, the gating must be altered so that the carry is propagated when a stage changes from 0 to 1 rather than when a stage changes from 1 to 0, as in addition or counting forward. This means that the false-true transfer must occur when the preceding stage contains 1, and that the true-false transfer must occur when the preceding stage contains a 0. As with addition, the particular transfer in which complementation takes place is arbitrary.

For the purpose of creating dual numbers, the gating system:

$$\text{If } T_{i-1} = 0, \text{ then } T_i \xrightarrow{C} F_i$$

has been constructed. Hence, a minimum of new equipment will be needed if the complementing is done in the $T-F$ path. Only the new gate system:

$$\text{If } T_{i-1} = 1, \text{ then } F_i \to T_i$$

need be added. Thus the rules for a subtracting counter are:

$$\begin{aligned} &F_0 \xrightarrow{C} T_0 \\ &\text{If } T_{i-1} = 1, \text{ then } F_i \to T_i \\ \text{and} \quad &T_0 \to F_0 \\ &\text{If } T_{i-1} = 0, \text{ then } T_i \xrightarrow{C} F_i. \end{aligned} \tag{7}$$

Assuming that the true rank initially contains the number 11111, these rules indicate the dual false number is 11110. In this way, the entries in Table IV may be found. It will be noted that the column of false numbers in Table IV are exactly those of Table I, which further justifies the choice of the complementation in the true-false path. This means that, whether the counter is to go forward or backward from an arbitrary origin, the same rules for constructing the dual may be used.

TABLE IV

TRUE AND FALSE NUMBERS FOR A SELF-INSTRUCTED SUBTRACTING COUNTER

Count	Decimal Equivalent of the Number is True	True Rank	False Rank
0	0	00000	11111
1	31	11111	11110
2	30	11110	11101
3	29	11101	11000
4	28	11100	11011
5	27	11011	10010
6	26	11010	10001
7	25	11001	10100
8	24	11000	10111
9	23	10111	00110
10	22	10110	00101
11	21	10101	00000
12	20	10100	00011
13	19	10011	01010
14	18	10010	01001
15	17	10001	01100
16	16	10000	01111
17	15	01111	01110
18	14	01110	01101
19	13	01101	10000
20	12	01100	01011
21	11	01011	00010
22	10	01010	00001
23	9	01001	00100
24	8	01000	00111
25	7	00111	10110
26	6	00110	10101
27	5	00101	10000
28	4	00100	10011
29	3	00011	11010
30	2	00010	11001
31	1	00001	11100

As with the adding counter, the interior $T-F$ gates may be made separately-instructed, and a modified set of dual numbers obtained (Table V). Further, the set of dual-constructing rules of (5) permits the same simplification in operating procedure; i.e., the complete set of dual gates may be active even during counting. Also as in the adding counter, the rules of (5) generate the number which will be dual to the next number in the counting sequence (($N-1$) in this case).

As with the column of false numbers of Table I, those of Tables III, IV and V exhibit regularities in the vertical direction. Sets of rules similar to those stated for Table I may be easily derived.

Review of False and True Numbers. It will be well to pause and to summarize the pertinent facts relative to these numbers appearing in the two ranks of the positive memory counter.

First, the definition of dual must be particularized. Let "false" describe any number which appears in the false rank. Let "self-instructed dual" and "separately-instructed dual" describe the numbers which form in the false rank opposite a given true number according as the interior $T-F$ gates are self-instructed, or separately-instructed respectively. Hence the column of false numbers in Tables I and IV are "self-instructed duals" whereas the column of false numbers in Tables III and V are "separately-instructed duals." It is evident that these two kinds of duals can be constructed one from the other by shifting the digits in the 1st through 4th places one count up or down as required.

Now, it was found in the initial discussion of this counter that for every number which appears in true, there appears a unique number in false. This particular number which co-existed with the true number after the completion of a count cycle was labeled a "dual" and a set of rules was discovered which related any true and its dual. These rules (4) must now be called the "self-instructed dual-construction rules." To this point in the discussion, the interior gates were all static; as a result, part of each dual number (F_0) was formed when the $T-F$ transfer was made and part of it (all F_i's except F_0) was formed when the $F-T$ transfer was made. Table I tabulated these numbers.

Next it was shown that the interior gates could be made separately-instructed. It was pointed out that the effect of this so far as false was concerned was to delay until the following count all true-false gating which was set-up as a result of changes in true after the false-true gating. It is exactly this gating which generated digits in false beyond the 0th. Therefore, it is found that the digits F_1 through F_4 which appear in the self-instructed case after $(j-1)$ counts, will appear in the separately-instructed case after j counts. Thus, to construct in the separately-instructed case the number which is dual to the jth number in true, use digits F_1 through F_4 from the $(j-1)$st self-instructed dual and digit F_0 from the jth self-instructed dual.

Because of this postponement of construction of digits F_1 through F_4 until the following count, the rules (4) which are stated above for constructing the $(j-1)$st self-instructed dual in the self-instructed case will yield for the separately-instructed case, the digits F_1 through F_4 of the jth separately-instructed dual. Since F_0 alternates 0 and 1, the dual constructing system as stated in (4) will yield the complement of the correct F_0 for the jth separately-instructed dual. Thus a set of rules which will construct, having installed an arbitrary number (N) in true, the separately-instructed dual of $(N+1)$ (for an adding counter) or of $(N-1)$ (for a subtracting counter) is given in (6).

It was found in discussing the subtracting counter that any true number gave rise to the same dual number (either for an adding or subtracting counter) so long as the interior gates were self-instructed. Thus, the same self-instructed dual-constructing rules are valid for the adding or subtracting counter. It was also found that the dual-constructing rules modified as in (6) generates the separately-instructed dual of the next true number in the sequence. Hence, in a counter with separately-instructed interior gates, if the separately-instructed dual-constructing system operates on an arbitrary number (N) in the true rank, it will generate a number which may be dual to either $(N-1)$ or $(N+1)$ depending upon what sort of false-true gates are subsequently enabled. Thus, it follows that for a given false number, the number it will pair with in an adding counter will differ by 2 from the number it will pair with in the subtracting counter. Comparison of Tables III and V verifies this.

TABLE V

TRUE AND FALSE NUMBERS FOR A SEPARATELY-INSTRUCTED SUBTRACTING COUNTER

Count	Decimal Equivalent of the Number in True	True Rank	False Rank
0	0	00000	11101
1	31	11111	11110
2	30	11110	11111
3	29	11101	11100
4	28	11100	11001
5	27	11011	11010
6	26	11010	10011
7	25	11001	10000
8	24	11000	10101
9	23	10111	10110
10	22	10110	00111
11	21	10101	00100
12	20	10100	00001
13	19	10011	00010
14	18	10010	01011
15	17	10001	01000
16	16	10000	01101
17	15	01111	01110
18	14	01110	01111
19	13	01101	01100
20	12	01100	01001
21	11	01011	01010
22	10	01010	00011
23	9	01001	00000
24	8	01000	00101
25	7	00111	00110
26	6	00110	10111
27	5	00101	10100
28	4	00100	10001
29	3	00011	10100
30	2	00010	11011
31	1	00001	11000

The Counter with Complete Gating. There now exists for the several functions investigated, the following systems of gates in the counter.

Input Stage	*Interior Stage*
$T_0 \rightarrow F_0$	(A) If $T_{i-1} = 1$, then $T_i \rightarrow F_i$
	(B) If $T_{i-1} = 0$, then $T_i \xrightarrow{c} F_i$
$F_0 \xrightarrow{c} T_0$	(C) If $T_{i-1} = 1$, then $F_i \rightarrow T_i$
	(D) If $T_{i-1} = 0$, then $F_i \xrightarrow{c} T_i$.

For counting positively gates (A) and (D) are required; for counting negatively, gates (B) and (C); and for constructing separately-instructed duals, gates (A) and (B). Throughout it must be remembered that when a function involves a transfer in only one direction (such as dual construction which involves only a $T-F$ transfer), the unwanted gate in the input stage must not be operated.[6]

There still remains the combination (C) and (D) which constitute only a transfer from false to true. It can be readily seen by studying the detailed operations which these particular gates perform, that they will construct in the true rank, the 1's-complement of the number which originally stood there. If (N) is in the true rank and its dual is in false, then the operation of only gates (C) and (D) and the $F-T$ transfer of the 0th stage will form in true the 1's-complement of (N).

Thus, the completely gated counter has four modes of operation: it can count forward; it can count backward; it can form a dual; and it can form a 1's-complement. So far all of these except the last have found a use in digital machinery.

THE MULTIPLE-RANKED COUNTER

Consider now the following points, all of which have been previously made.

(a) The false numbers are unique and are in one-to-one correspondence with the binary integers.

(b) The transfer from true to false has no carry or carry-like behavior associated with it.

(c) The rank of true-false gates may be operated as separately-instructed, rather than self-instructed, gates.

Items (b) and (c) together mean that in the time required to effect a transfer into a toggle, the information is solidly installed in the false rank; and further it cannot change (because of (c)) until the next input signal. The information in false is completely static for the interval between input signals and may therefore be used during this period to supply output to other circuits or devices.

In contrast to this is the situation in the true rank. For some, or if the counter is operating at its maximum rate, all of the time between input signals, carry information is rippling along the true rank; and the information in true does not become static until some indeterminate time, as it cannot be known a priori how far the carry will propagate in the random case.

Usually it is desired to use the information in the counter at the earliest possible moment, and if the unusual correspondence which exists between false and the binary integers is an acceptable one for the application, the counter can supply from the false rank output information within one toggle transfer time after the input signal is received. The carry is then propagating during the interval in which the information in false is being utilized; the time required for carry propagation runs concurrently with the period of utilization of the counter information, rather than being directly added to the utilization period. In some applications this allows an increase in operating rate and, in fact, this logical arrangement gives the most favorable operating speed for a given kind of toggle and gate technique.

Having seen how the false rank can be utilized as an output terminal, consider now what happens if, at the end of any count (i.e., after all carries have completed), all gates between the false and the true ranks are completely disabled. The two ranks are independent devices and may be manipulated in any fashion which proves useful. In particular, suppose the false rank is now connected via an appropriate system of gates to a second true rank. Since it is known how to form dual numbers, it is possible to now have false and the second true rank co-operate together as a counter; meanwhile, the first true rank retains its information, awaiting the time when it again will resume counting.

The possibility of using one false rank in conjunction with several true ranks leads to the concept of a "central exchange" counter. In it, the false rank co-operates with whichever of the true ranks is required to count at a given time. This central exchange scheme is particularly attractive when the false rank may be used as the output terminal of the counter; the false rank may be directly connected to the load, and the gates within the counter do all the necessary switching of the load to the various sources of information, as well as accomplish the counting action. If any of these alternate sources of information need not have counting properties, it is certainly not necessary to provide for it a true rank. There need only be provided the gating which makes false think that it is receiving information from a true rank; i.e., the system of dual-constructing gates.

The example illustrated in Fig. 3 will consolidate these ideas. There is assumed an electrostatic memory which requires regeneration; hence one source of information for the address circuit of the memory is the counter which keeps track of the regeneration process. Another source of information is certainly an arbitrary address for the purpose of selecting data or instructions from the memory. Many computing machines store in their memories a routine of instructions which are performed sequentially, and the counter which keeps track of the instruction sequence is yet a third source of address information. Assume further that a magnetic wire or tape is associated with the machine. There will probably be a counter associated with it which is "locked" to the wire and so must count either backward or forward to keep track of position on the wire. If it is desired to locate an address in the memory which corresponds to a particular position on the wire, the true rank associated with the magnetic wire switches from its own false rank to the false rank associated with the address-selecting circuit. And so on.

Certainly such an arrangement is a counter in the broadest sense. In Fig. 3 is indicated the various gate systems which must exist between the various ranks for the assumed properties.

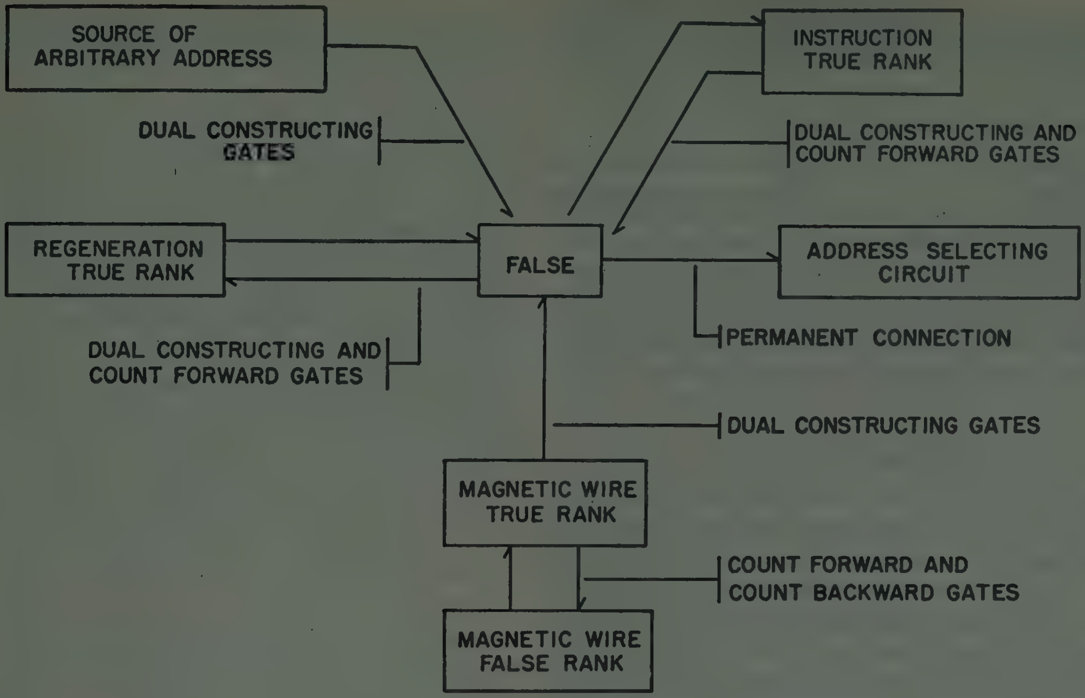

SOURCE OF ARBITRARY ADDRESS
DUAL CONSTRUCTING GATES
INSTRUCTION TRUE RANK
DUAL CONSTRUCTING AND COUNT FORWARD GATES
REGENERATION TRUE RANK
FALSE
ADDRESS SELECTING CIRCUIT
PERMANENT CONNECTION
DUAL CONSTRUCTING AND COUNT FORWARD GATES
DUAL CONSTRUCTING GATES
MAGNETIC WIRE TRUE RANK
COUNT FORWARD AND COUNT BACKWARD GATES
MAGNETIC WIRE FALSE RANK

Fig. 3—A multiple-marked counter for a specific computing machine application.

EXPERIMENTAL RESULTS[4] AND CONCLUSIONS

A 5-stage counter based on the principles outlined herein has been constructed and operated. All of the predicted modes of operation have been verified; the entries in the various tables of false numbers have been checked and the various properties described in this paper demonstrated.

A counter based on a positive memory philosophy is seen to offer advantages in speed of operation and in simplification of required equipment for some applications. It is of course essential to obtain these benefits that one be willing to accept the unusual correspondence which exists between the false numbers and the binary integers; for the particular case of addressing storage locations, it is quite immaterial how the various locations are labeled. Further the time indefiniteness of the logically required associated memory facility offers distinct engineering advantages in that it is no longer necessary to carefully control time constants or to carefully shape input signals.

As a numerical example assume that the regeneration interval required by the memory proper is 20 microseconds; assume that a transfer into a toggle requires 3 microseconds, and that the carry time of the counter is 10 microseconds. If the output to the address selecting portion of the memory is taken from the false rank of the counter, the address is available in 3 microseconds and this plus the time required by the memory itself leads to a regeneration cycle of 23 microseconds. The 3 microsecond transfer from false to true and the 10 microsecond carry time run concurrently with the 20 microsecond interval of the memory. If, however, the address circuit of the memory receives information from the true rank of the counter, the regeneration cycle now becomes of the order of 35 microseconds—3 for the true-false transfer, perhaps 2 for the false-true transfer before the carry begins to propagate, 10 for the carry, and 20 for the memory. Hence by a logical rearrangement of the same equipment and without extra equipment, there is a gain in speed of about 1.5.

ACKNOWLEDGMENT

Part of the work described in this paper was supported by U. S. Army contract W-36-034-ORD-7481 between the Ordnance Department and the Institute for Advanced Study. The author wishes to express his appreciation for permission to use these results and also to acknowledge the encouragement and support of the administration and of the engineering staff of the Electronic Computer Project of the Institute for Advanced Study, Princeton, New Jersey.

* * *

Combined Reading and Writing on a Magnetic Drum*

J. H. McGUIGAN†, ASSOCIATE, IRE

Summary—**This paper points out that the characteristics of magnetic recording make it possible to combine reading and writing in the same cell as it passes just once under the head. Amplifier requirements for this method of operation are discussed and a suitable design presented. A single head is used for both reading and writing. The process can be repeated in every successive cell at a cell rate of 60 kc. The techniques described, which are applicable to either parallel or serial systems, extend the utility of magnetic drums by allowing data processing as well as data storage.**

I. INTRODUCTION

MAGNETIC DRUMS are well known and widely used as digital data storage devices. In these devices the operations of storing information at a given address and of reading it back are divorced from each other and are performed during separate accesses to the address. This paper deals with the technique of combining these operations so that both can be performed with a common head during the course of a single access to an address. The usefulness of this "single-pass" mode of operation lies in the possibility of using magnetic drums for data manipulation in addition to their familiar application to data storage.

The paper will open with a brief review of magnetic recording principles, followed by an explanation of single-pass operation. The remainder of the paper will deal with a practical, working embodiment of single-pass operation. The heads and the drum surface will be treated only briefly; the major emphasis will be on the circuit features of a combined reading-writing amplifier which meets the rather special requirements imposed by single-pass operation.

II. MAGNETIC DRUM RECORDING PRINCIPLES

A. *Definition of Terms*

The surface area of the drum is divided into *cells*, which are grouped into *tracks* and *slots*. A cell is the area assigned to a single bit of information. A track consists of all the cells which pass under a single head. A slot consists of all the cells—one in each track—which are centered under their respective heads at the same time.

B. *Magnetic Recording Review*

All magnetic drum digital memories are based on the principle of producing a pattern of magnetization on the surface of the drum for each item of information to be remembered. Any one of several codes, or relationships between the magnetized pattern and the component bits of information, can be used; the code discussed below is the so-called "return-to-zero" code, in which each bit of information is represented by a spot magnetized to saturation in one direction and surrounded by a background field magnetized to saturation in the other.

The basic operations of magnetic recording consist of writing spots, reading them, and erasing them. Writing and erasing are complementary processes which will be spoken of as "writing X" and "writing 0" respectively. The three basic operations will now be discussed with reference to Fig. 1. The circuitry in this drawing is arranged to aid the following explanation; practical circuits for doing the job will be presented later.

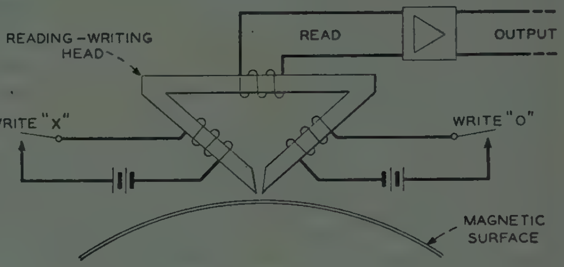


Fig. 1—Magnetic head and drum.

Each magnetic head is placed in a position relative to the drum about as shown in the drawing. A small clearance, of the order of 0.002 inch, is maintained between the pole tips and the surface of the drum, in order to avoid wear of the pole tips. Since there is no contact between the head and the drum coating, all the writing and reading depends on the existence of fringing flux.

A necessary preliminary to the recording process, when a return-to-zero code is used, is to produce the background field by magnetizing the whole track to saturation in a direction which may for convenience be called "negative." One way of doing this preliminary biasing job is to close the key marked "write 0" in the figure, and to keep it closed long enough for the drum to make at least one complete revolution.

To write a spot in a given cell, it is necessary to wait until that cell is centered under the pole tips of the head. A short pulse of current is then passed through a winding of the head, of amplitude and polarity such as to produce saturation of the drum coating in the opposite or "positive" direction. This may be done by momentarily closing the key marked "write X" in the figure. The current pulse may be considered to be of such short duration that the drum does not move appreciably during the time of the pulse. When the cell is again centered under the head, a spot can be erased in the same manner in which it was written, using a current pulse of opposite polarity, which may be obtained by momentarily closing the key marked "write 0." Saturation values of magnetization are used in order to render the system insensitive to variations in the amplitude of the current pulse provided a limiting minimum value is exceeded.

---

* Decimal classification: R365.35×621.385. Original manuscript received by the Institute, May 22, 1953.

† Bell Telephone Laboratories, Murray Hill, N. J.

The "write X" procedure just described produces a spot which is magnetized to positive saturation in the middle of the cell, with a smooth transition back to negative saturation toward the edges of the cell. The distribution of flux is qualitatively as shown in the first graph at the left in Fig. 2.

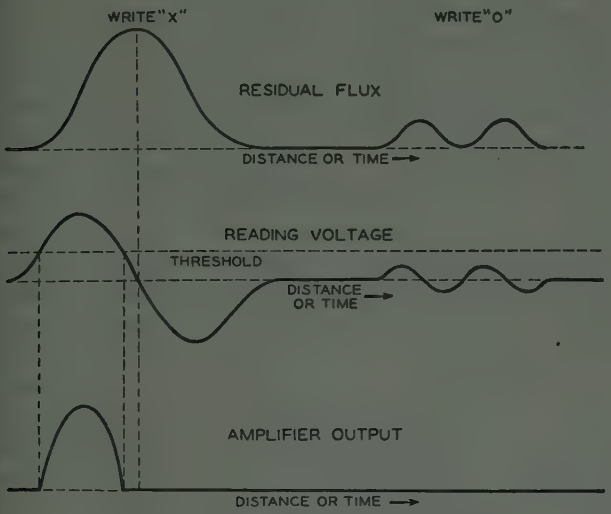


Fig. 2—Magnetic recording wave forms.

The skirts of this curve extend appreciably on either side of the area which was directly under the pole tips when the spot was written. When the "write 0" procedure described is used to erase a spot, it is found that the spot is not completely obliterated. The center of the cell is returned to negative saturation, but the area surrounding the center is left with an intermediate value of magnetization, as shown by the first graph at the right in Fig. 2. This effect is caused by hysteresis and by the fact that the fringing flux from the head produces weaker magnetizing forces at points more remote from the pole tips.

When a spot passes under the pole tips of the head, a voltage is induced in the head winding which is for practical purposes proportional to the time-derivative of the flux distribution in the cell. This voltage is used for reading. In the circuit of Fig. 1 a separate winding is shown, across which the reading voltage is observed; obviously with appropriate circuit design the windings used for writing could also be used for reading.

The second pair of graphs in Fig. 2 show reading voltages for a cell in which an X has been written and for a cell in which writing X has been followed by writing 0. The abscissa for all the graphs in the figure may be taken as representing either distance or time, the two quantities being related by the surface velocity of the drum. The read-back voltages for a cell with an X and a cell with a 0 differ in both amplitude and wave shape. They can be readily distinguished by setting up an amplitude threshold, as shown by the dotted line in the second pair of graphs, at such a level that the read-X voltage passes the threshold while the read-0 voltage does not. When this is done, the output from the reading amplifier is qualitatively as shown in the third pair of graphs; the amplifier delivers a pulse when a cell with an X passes under the head, while there is no pulse in response to a cell with a 0.

C. Single-Pass Operation

The graphs of Fig. 2 exhibit an important characteristic of magnetic recording which, though not conspicuous, is readily apparent when pointed out. This is the fact that the reading output from a cell is available some little time before the cell reaches the point at which writing is to take place. The ideal time to read is when the read-out voltage is a maximum. The time to write is, by definition, when the center of the cell is under the head. Between these two times there is a definite interval which can be used to interpret information and arrive at decisions. This feature makes it possible to read the information contained in a given cell, or in a combination of cells in the same slot; to determine on the basis of this information, together with the program of the system and any available input information, whether the information should be altered; and, if so, to alter it, all as the slot passes just once under the head. This method of operation, which has come to be called "single-pass" operation, was developed by O. J. Murphy, N. D. Newby, and the writer.

Single-pass operation is important because it offers the possibility of building data-processing systems to handle large amounts of information rapidly with a small amount of equipment. Preliminary design estimates on a particular data-processing job, a part of the DIAD telephone switching control system described in a companion paper, indicated that to do the job without single-pass operation would require twice as many drum tracks, twice as many amplifier vacuum tubes, and four times as many heads.

The use of single-pass operation gives rise to two major design problems which, though challenging, were not found insuperable. The first of these, and the more readily solved, has to do with the design of logical circuits. In the DIAD system the interval between the time at which the reading output is available and the time at which writing must be performed is of the order of 2 μsec. This 2 μsec interval is all the time that is available for performing all the logical operations required by the system layout. Fortunately, however, vacuum tube and germanium diode logic circuits can be made to operate without great difficulty within this interval, even when several successive stages of logical connectives are required.

The second problem has to do with the design of amplifier circuits to meet the rather special requirements imposed by a single-pass operation. This problem is analogous to that encountered in radar receivers, which must withstand the "main bang" transmitting signal and then recover rapidly from overload in order to respond to weak reflected signals.

In the magnetic drum equipment for DIAD, the read-X voltage, as shown in the second graph at the left in Fig. 2, is 30 mv peak-to-peak, while the output of the reading amplifier, as determined by system design considerations, is a pulse of some 50 v amplitude. Thus, a fairly high-gain amplifier is required.

Now in the writing operation a strong pulse of current is forced through the head winding. The voltage appearing across the winding due to this current pulse is about 30 v peak-to-peak, some 60 db higher than the reading voltage. Such a large input signal may well be expected to overload the reading amplifier. In any given cell, the overload causes no difficulty, since the reading process is completed before the writing begins.

The main amplifier design problem arises from the fact that the circuits must consider each successive cell as it passes under the head. Some figures from the DIAD system will illustrate the problem. The cells on the DIAD drum pass under the heads at the rate of sixty thousand per second; that is, the time-separation between successive cells is a little more than 16 μsec. The duration of the writing pulse is 3 μsec, so that there is an interval of 13 μsec between the end of one writing pulse and the beginning of the next. Allowing 2 μsec before the next writing pulse for reading, we have left only 11 μsec during which the amplifier must recover from a severe overload and the writing voltage must decay more than 60 db, if the amplifier is to read unambiguously the information in the cell immediately following a cell in which writing has just taken place. The amplifier to be described in Section V represents one solution to this problem.

III. Reading-Writing Heads

Fig. 1, though not drawn to scale, gives a sufficient idea of the design of the head. The head consists of a laminated permalloy structure having a pair of sharply pointed pole tips with an air gap between. Laminations only 0.001 inch thick are used, in order to obtain good hf response. The three sides of the triangles are formed of separate pileups of laminations, prepared by a manufacturing process which eliminates the necessity of handling individual laminations. The triangular shape, chosen to permit this process, also serves to confine the magnetic influence of the head to a small area of the drum surface, so that the cells can be closely spaced.

The head as originally developed had three separate windings as shown in Fig. 1. For use in the DIAD system the head was modified to have a single winding. Single-winding operation is made possible by coupling the head to the reading-writing amplifier with a transformer having separate windings for the three functions of write X, write 0, and read. This transformer-coupled arrangement, which is desirable because it permits the use of a simple two-wire connecting cable between head and amplifier, was suggested by H. A. Henning.

The discussion of magnetic recording in section II*B* assumed a unidirectional pulse of current. Obviously such a pulse cannot be passed without distortion through a transformer, since a transformer does not transmit direct current. That magnetic recording of the type under discussion can, nevertheless, be satisfactorily achieved is due to hysteresis and to the duty cycle of the writing current. A pulse of writing current through the head is indeed followed by a reverse-current overshoot. The lf transmission of the transformer can be made good enough, however, so that the reverse current following a single writing pulse is negligible.

When writing pulses of the same polarity are applied in each of a long succession of cells, the reverse current builds up to a value just sufficient to cancel the dc component of the train of pulses. With the parameters used in the DIAD system, the reverse current never gets larger than about 15 per cent of the peak value of the writing current. The reverse current does tend to counteract the magnetization of the drum coating produced by the writing current, but the shape of the hysteresis loop of the coating material is such that the effect of the reverse current on the recorded spots is negligible. Trains of one thousand spots, occupying a whole track on the drum, have been recorded with a transformer-coupled head, and there was no noticeable degradation from the first spot in the train to the last.

IV. Magnetic Drum Coating

Both powdered oxide and electroplated solid metal coatings have been used on magnetic drums. A solid metal coating was chosen for the drum in the DIAD system.

As was pointed out, a spot recorded on the drum spreads out over an area larger than the area directly under the pole tips of the head at the time of writing. The extent of this spreading, which has a direct influence on the feasibility of single-pass operation, depends on the coercivity of the magnetic material. The coercivity, in turn, depends on the composition of the coating and on such details of the electroplating process as the plating current density and the composition of the plating bath.

For the purposes of single-pass operation a low-coercivity coating was used; the material is a nickel-cobalt alloy with a coercivity of the order of 75 oersteds. With this coating a cell density of 30 cells per inch along the track and a cell repetition rate of 60 thousand cells per second have been achieved. Considerably more impressive figures have been reported by other workers in the magnetic drum field; it is felt that further refinements in single-pass technique may eventually permit the operation of data-processing systems with cell densities and cell repetition rates comparable to those used for simple data-storage systems.

V. Amplifier Circuit Design

The very short time intervals encountered in single-pass operation do not permit the use of mechanical switching between amplifiers and heads, and the peak value of the writing current pulse is too high to permit the use of electronic switching. Thus, a reading and a

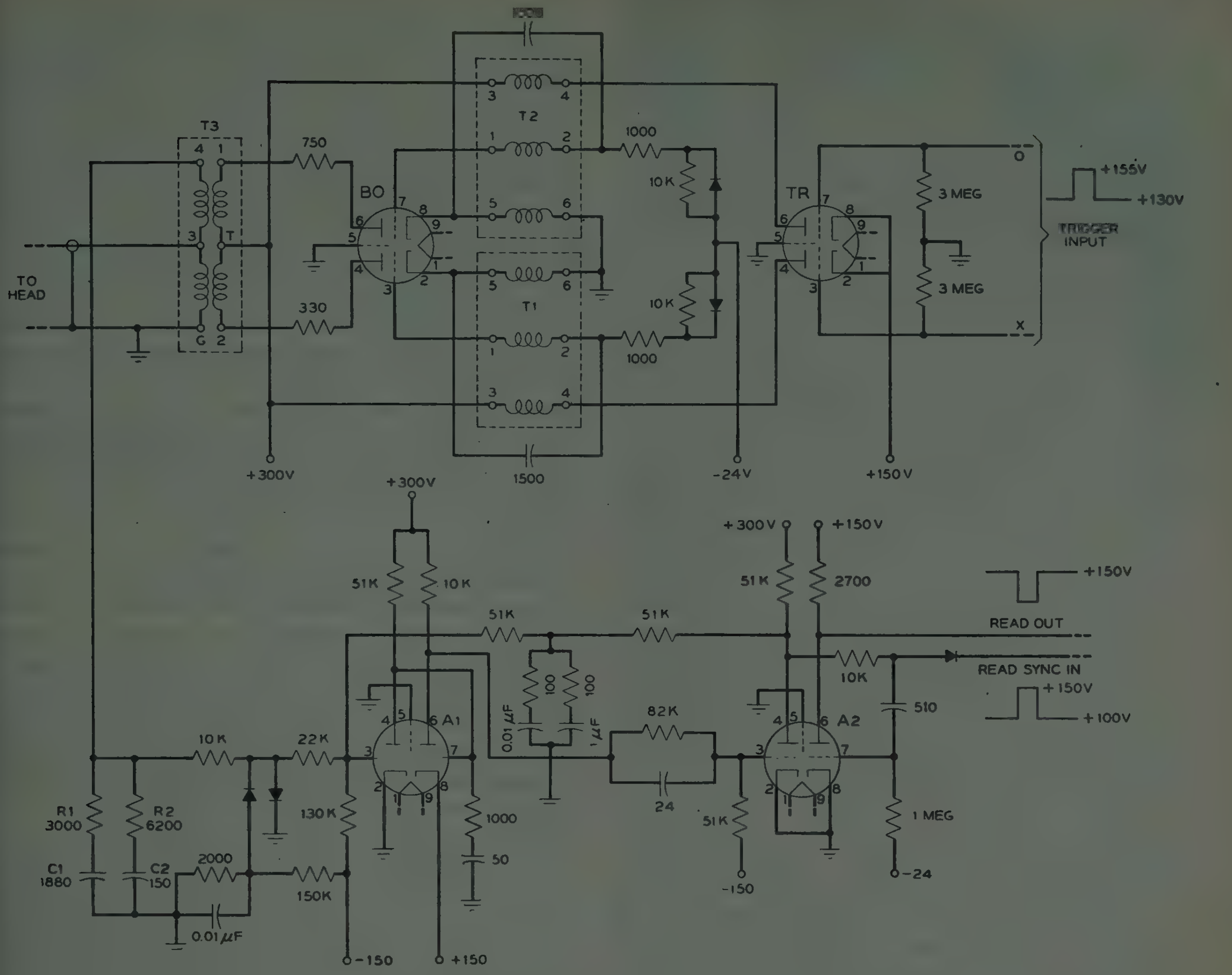

1500
T2
3
4
1
2
5
6
T1
T3
4 1
3 T
G 2
750
330
BO
7 8 9 6 5 4 3 2 1
1000
10 K
10 K
1000
TR
3 MEG
3 MEG
0
X
+155V
+130V
TRIGGER INPUT
TO HEAD
+300V
+300V
1500
-24V
+150V
+300V
+150V
51K
10 K
51K
51K
51 K
2700
+150V
READ OUT
10K
READ SYNC IN
+150V
+100V
510
100
100
0.01 μF
1 μF
82K
24
A1
A2
10 K
22K
130 K
1000
50
R1 3000
R2 6200
C1 1880
C2 150
2000
150K
0.01 μF
51K
1 MEG
-150
-24
-150
+150

Fig. 3—Schematic of combined writing-reading amplifier.

writing amplifier are provided for each head, and both emain connected to the head at all times.

In order to prevent the reading amplifier from delivering an output signal during the time of the writing operation, which might cause false operation of the logical circuits following the amplifiers, gating or synchronizing ulses are provided. A read-sync pulse gates the reading mplifier, so that no output signal appears except during he time of this pulse. A write-sync pulse controls the iming of the writing operation. The two pulses are non-verlapping in time, the trailing edge of the read-sync ulse coinciding with or slightly preceding the leading dge of the write-sync pulse. Since the reading information must be held over through the duration of the write-sync pulse, bistable vacuum tube circuits are provided s a part of the logical circuits. They are tripped by the eading information, and, after controlling the writing peration, reset at the end of the write-sync pulse.

A schematic of the reading-writing amplifier, which was designed by O. J. Murphy, W. A. Cornell and the writer, is given in Fig. 3. All tubes are 2C51 miniature ouble triodes. The complete circuit consists of a writing circuit at the top of the figure and a reading circuit at the bottom. Except for the head-coupling transformer, which acts as an output transformer for the writing circuit and an input transformer for the reading circuit, the two circuits are independent, and their design features can be discussed separately.

A. Writing Circuit

Although spoken of as a writing amplifier, the writing circuit is really a pair of pulse-generating circuits, one for writing X and the other for writing 0. Each consists of a normally quiescent blocking oscillator tube for producing the pulse of writing current and a trigger tube for initiating the action of the blocking oscillator. A description of one circuit will suffice for both, since they are identical except for one small difference which will be noted.

The trigger tube, *TR*, is arranged with its cathode at +150 v and its plate supplied with +300 v through winding 3–4 of the blocking oscillator transformer T_2. These plate and cathode supply voltages are chosen so that the grid of the *TR* tube may be directly connected to the output of a diode-gate logic circuit which, in the DIAD system, operates in the vicinity of +150 v as shown by the waveform near the trigger input terminal. The grid is connected to ground through a three-megohm resistance so that the *TR* tube is biased beyond cutoff if the input lead is disconnected.

An input lead is actually quite likely to be disconnected, since the gates supplying the inputs are separate plug-in units which may be removed for testing and servicing. The three-megohm resistance is so high compared to the source impedance of the gates that it has no appreciable influence on the grid voltage of the trigger tube when the gate is plugged in. One of the inputs to each writing gate is the write-sync pulse, so that the pulses appearing on each trigger lead are coincident with and controlled by the write-sync pulse. Thus the writing action does take place under the control of the write-sync pulse, as stated above, even though the write-sync pulse does not appear explicitly in the schematic.

There are a number of well-known blocking-oscillator circuit configurations in the literature. Many of these were tried and found capable of delivering the desired amplitude (around 180 ma) and duration (about 3 μsec) of current pulse. A current pulse of 180 ma greatly exceeds the rating of a type 2C51 tube, but the duty cycle is low. Experience over a period of three years has shown no greater incidence of tube failure in this circuit than in more conventional applications.

The circuit used here was chosen because it best meets the special requirements imposed by the particular application for which it is intended. These special requirements may be briefly outlined as: Two blocking oscillators must work together through a common coupling device into a common load. When either blocking oscillator fires, it must not cause the other to fire. Each blocking oscillator, after firing, must recover and be ready to fire again within 13 μsec.

Protection against cross-fire is gained by confining the actual blocking-oscillator circuit to the grid and cathode of the tube and using the plate circuit only for output. When either blocking oscillator fires, coupling in the output transformer induces a voltage swing on the plate of the other blocking oscillator of such polarity as to tend to cause it to fire; but this circuit is so insensitive to swings of plate voltage that there is an estimated 30 db margin against false firing.

When the blocking oscillator fires, grid current flows in the loop composed of winding 1–2 of the transformer, grid, cathode, and 1,500 mmf coupling condenser from cathode to terminal 2 of the transformer. This grid current charges the condenser to produce the additional grid bias which causes the blocking oscillator to block after a single pulse. After the blocking oscillator has fired, the condenser discharges through a loop which includes winding 5–6 of the transformer to ground and a network of two resistors and a varistor to a −24 v source of bias.

The condenser influences the duration of the blocking oscillator pulse; the indicated value of 1,500 mmf was found empirically to be the minimum capacitance which would produce the desired pulse duration of 3 μsec. The time constant defined by this condenser and the resistance through which it discharges influences the recovery time of the blocking oscillator, though the condenser does not discharge exponentially because of the transformer winding 5–6 in the discharge loop. A resistance of 1,000 ohms was found empirically to be the largest resistance which would produce the desired recovery time of 13 μsec.

The series combination of the blocking condenser and the discharge resistor is effectively shunted across winding 5–6 of the transformer. If the discharge resistor is limited to the value of 1,000 ohms determined by recovery time considerations, the loading on the transformer is so great that the blocking oscillator is difficult to trigger, although once triggered it delivers a satisfactory pulse.

To improve the triggering sensitivity, a 10,000-ohm resistor shunted by a varistor is added in series with the 1,000-ohm discharge resistor. The varistor is poled so as to present a high impedance to positive-going pulses on terminal 5 of the transformer, so that for purposes of triggering and firing the transformer is effectively loaded with 11,000 ohms. This load is light enough so that the triggering sensitivity of the blocking oscillator is not impaired. For discharging the blocking condenser, however, the varistor presents a low impedance, so that the discharge resistance is effectively 1,000 ohms.

The plates of the two blocking oscillators are fed from +300 v through two windings of the output transformer so connected that the two oscillators deliver pulses of opposite polarity to the head, which is connected to a third winding of the transformer. Between terminals 1 and 2 of the output transformer and the blocking oscillator plates are two resistors whose purpose is to limit the amplitudes of the current pulses delivered to the heads. The different values of these two resistances, which represent the only difference between the otherwise identical blocking oscillators, result from the experimental observation that the current-pulse amplitude required to produce most nearly complete effacement of a spot is slightly different from the amplitude used to write the spot.

B. Reading Circuit

The need to withstand the large voltage swing appearing across the terminals of the head when a blocking oscillator fires constitutes the chief problem in the design of the reading circuit. This large voltage swing, as shown in Fig. 4, is made up of two components. The first is a voltage approximately proportional to the time-derivative of the current pulse. Because of the shape of the current pulse, this component exhibits maxima of opposite polarity near the beginning and end of the current pulse and decays very rapidly to zero after the end of the pulse.

The second component results from the fact that high flux densities are built up in the magnetic structures of the head and the coupling transformer during the pulse. These fluxes cannot decay instantaneously, their rate of decay being limited by eddy currents in the laminations. As a result, the voltage peak at the end of the current pulse is followed by a quasi-exponential decay of voltage back toward the base line. This gradual decay is a serious problem. The tail of the writing voltage tends to mask the reading voltage in the following cell, even without the difficulties caused by amplifier overload.

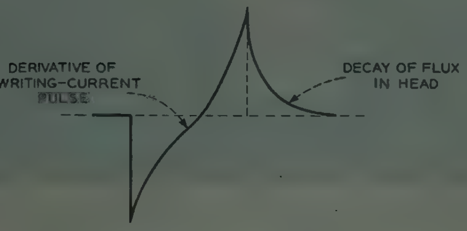


Fig. 4—Writing voltage waveform at head.

The head is connected across winding G-3 of the coupling transformer. The input to the amplifier is taken across winding G-4. Winding G-4 has three times as many turns as winding G-3, to provide about 10 db of voltage gain. Bridged across winding G-4 is a network of two resistors and two condensers, the purpose of which is to accelerate the quasi-exponential decay of the writing voltage. With this network present, the voltage appearing on terminal 4 due to writing is negligible compared to the reading voltage at the time of the read-sync pulse next following the writing.

The network is effective in reducing the problem of the slow-decay component of the writing voltage. It has little effect on the initial large voltage swing. Most of this swing is eliminated by a clipper circuit consisting of a series resistor and two shunt diodes. At the output of the clipper the writing voltage swing is reduced from 90 v peak-to-peak to 2 v peak-to-peak, while the reading voltage of 90 mv peak-to-peak is little attenuated. The ratio of writing voltage to reading voltage is thus much reduced, though the writing voltage is still capable of overloading the amplifier.

In an ac coupled amplifier subjected to large input signals, interstage coupling condensers may become charged through the flow of grid current. The amplifier is then paralyzed, or unable to function normally, until the excess charge is removed from the coupling condensers. The duration of the paralysis depends on the discharge time constant, which is roughly equal to the product of the coupling capacitance and the grid-leak resistance. In a dc coupled amplifier, on the other hand, there are no coupling condensers to become charged, and so recovery from overload is very rapid. For this reason the first three stages of the amplifier are dc coupled, even though uniform gain down to zero frequency is not required for accurate reproduction of the input signals. Since zero-frequency gain is not required, it has been possible to avoid most of the drift which commonly plagues the designer of dc amplifiers.

The first three stages constitute a shunt-feedback amplifier in which the input signal and a portion of the output signal are applied to the first grid through summing resistors. A third summing resistor is connected from the first grid to −150 v to balance out the large dc component in the output signal representing the operating point of the third-stage plate. The portion of the output signal used for feedback is derived from the signal on the third-stage plate by means of a fractionating network which has a transmission ratio varying with frequency.

At zero frequency the fractionating network has a transmission ratio of unity. A large amount of feedback is applied, and the operating points of the three stages are well stabilized. The zero-frequency voltage gain of the amplifier is about 14 db.

At frequencies within the desired pass-band of the amplifier, the fractionating network has a transmission ratio of one five-hundredth; the voltage gain of the amplifier is nearly 60 db, and this gain is stabilized by about 18 db of feedback. Toward the upper edge of the pass-band the feedback is reduced by 6 db in order to maintain the frequency characteristic uniform up to a frequency about an octave above that at which it would otherwise begin to drop off because of parasitic capacitances.

The fourth stage of the amplifier is biased well beyond cutoff to act as a threshold device. The interstage network between the third and fourth stages is a combining circuit for introducing the read-sync pulse. The signal from the third plate, gated by the read-sync pulse, is coupled to the grid of the fourth stage. The output of the amplifier is a negative-going pulse with a +150 v base line, coincident in time with the read-sync pulse. As was pointed out above, applications in which the reading output is used to control writing in the same slot will require some sort of pulse-stretching device following the amplifiers. These devices are not shown because they are considered a part of the logical circuits.

VI. Amplifier Equipment Design

The amplifiers are built as plug-in units to facilitate testing and maintenance. A photograph of the amplifier is shown in Fig. 5. A large portion of the wiring for the amplifier was preformed of metal strips sandwiched between two layers of plastic. The ends of these strips are brought through holes in one of the plastic layers to serve as mounting lugs for the circuit elements. This rather expensive style of construction resulted from a desire to approximate printed-circuit wiring with something which could be produced with local shop facilities. The wiring diagram was laid out with the idea in mind that printed wiring would be used if the amplifier were ever produced in sufficiently large quantities.

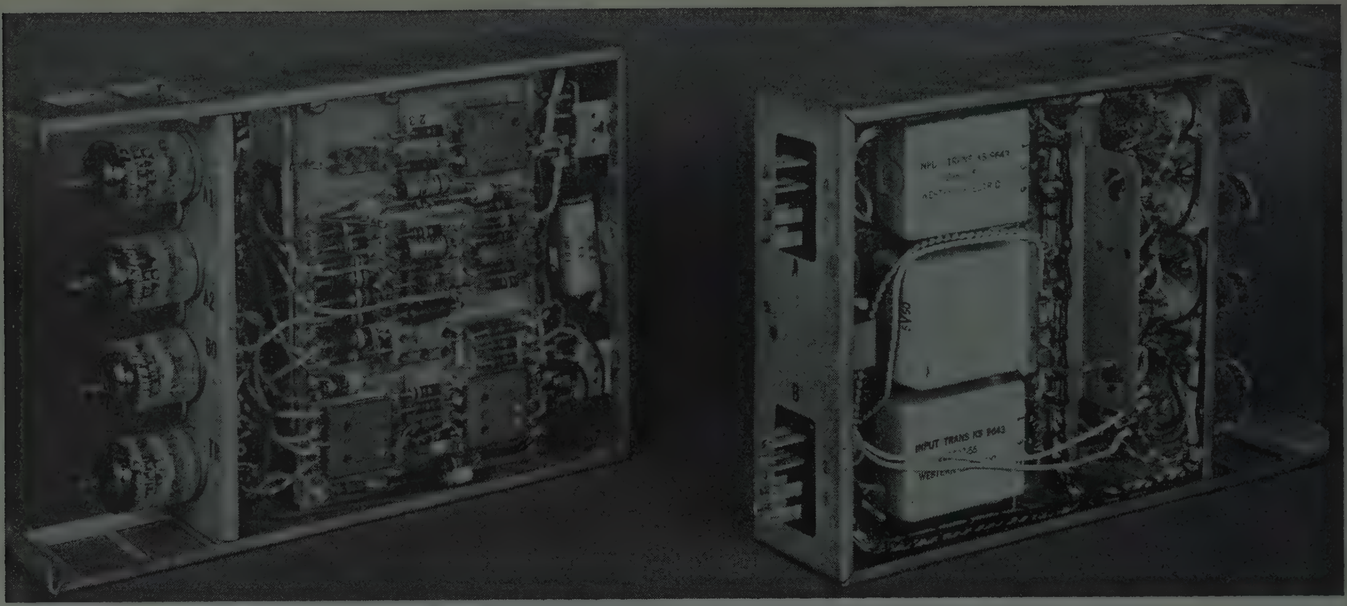


Fig. 5—Combined writing-reading amplifier.

VII. CONCLUSION

This paper has explained single-pass operation of a magnetic drum memory and described some details of the implementation of this process in the DIAD telephone system. This mode of operation offers interesting possibilities of equipment saving in systems using magnetic drums for the processing of large amounts of data. Possible fields of application range from telephone switching to stock control or inventory keeping.

VIII. ACKNOWLEDGMENT

The development of single-pass recording was a project requiring the co-operative effort of a great many individuals, some of whom have been mentioned in foregoing parts of this paper. Grateful appreciation is here expressed by the author to all of the others, too numerous to name, who contributed very substantially to the successful completion of the project, and thus to the writing of this paper.

A Transistor Pulse Amplifier Using External Regeneration*

J. H. VOGELSONG†

Summary—**A pulse-regenerative amplifier using a point-contact transistor has been operated at a basic frequency of 3 megacycles. To produce regenerated pulses with waveshapes which are practically independent of the waveshapes of the input pulses, a germanium diode circuit has been used in conjunction with an external feedback path. This arrangement also provides for the synchronization of the output pulses with a master clock. Transformer coupling has been incorporated into the circuit to provide dc restoration.**

INTRODUCTION

IN SYNCHRONOUS SERIAL computers of even a moderate degree of complexity, regeneration of pulses in amplitude, shape and time must be performed throughout the system. When logical operations are executed in circuits containing active elements such as vacuum tubes or transistors, this regeneration need not be separated from these operations since both can be performed simultaneously by the same circuit. On the other hand, logical operations can be carried out in circuits containing only elements which are essentially passive, such as diodes, to reduce the number of active elements required. In such instances regeneration can be provided by other circuits containing active elements.

Regenerative circuits of this kind, using point-contact transistors as the active elements, have been designed. In the one to be described, the transistor operates as an over-driven amplifier with external pulse feedback used in conjunction with germanium diodes to provide the regeneration. This mode of operation is in contrast to that of bistable circuits which utilize internal feedback supplied by the base resistance of the transistor.

The complete unit, to which a sinusoidal clock voltage is supplied, regenerates 0.17 microsecond pulses at a basic repetition rate of 3 megacycles. One of the desirable features of its operation at this frequency is the fact that its performance is relatively unimpaired by a slow recovery of reverse impedance which is found in many diodes.

---

* Decimal classification: R363×621.375.2×R282.12.

† Bell Telephone Laboratories, Inc., Murray Hill, N. J.

GENERAL

Block diagrams of two possible logical configurations for the regenerative amplifier are shown in Fig. 1. Both arrangements are well known in the computer field, the principle of external feedback being used in Seac,[1] for instance. In either circuit a coincidence between an input signal and the proper portion of the clock wave is necessary to initiate an output pulse. Therefore, if the leading edge of the input signal is arranged to arrive slightly prior to this portion of the clock wave, the clock determines the timing of the start of the output pulse. To assure that the clock also determines the duration of the output pulse, a feedback path returns the output pulse in such a manner as to make it equivalent to the original input signal. In this fashion, the output pulse can be sustained until terminated by the clock, even if the original input signal is removed.

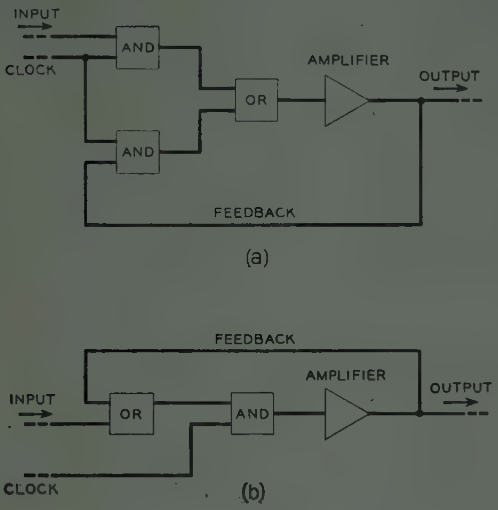


Fig. 1—Logical configurations for a pulse-regenerative amplifier.

DETAILED CIRCUIT OPERATION

Figs. 2 and 3 are circuit schematics of two slightly different implementations of the block diagram of Fig. 1b. The ensuing description is concerned more directly with the circuit of Fig. 2, but since the circuit of Fig. 3 differs only in that a more conventional configuration of the And-Circuit is used, it will not be treated separately. To aid the description, the performance with no input signal applied will be considered first and will be followed by the modification resulting when an input signal is present.

As a starting point, consider the applied clock potential to be at the negative peak of the sine wave. At this time diodes D_1 and D_2 and the transistor emitter are all in a reverse impedance state. If these reverse impedances were infinite, the emitter potential would be equal to the applied clock potential; actually, as a result of finite back impedances the emitter potential will be somewhat less negative at this time. While diode D_2 is essentially nonconducting, the potential (V_2) at the junction of diodes D_2, D_4 and D_6, and resistor R_3 is $E_{\rm clamp}$ minus the series forward voltage drops across diodes D_4 and D_5. (This is based on the assumption that no current flows through D_6 or R_4 toward this junction.)

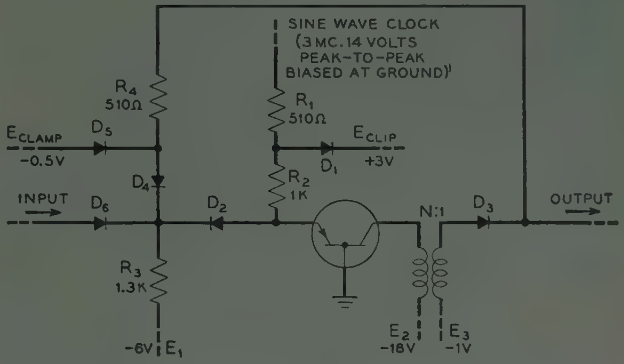


Fig. 2—Regenerative Amplifier I.

As the applied clock potential becomes less negative the emitter potential also rises. Diodes D_1 and D_2 and the transistor emitter remain nonconducting until the emitter reaches the potential, V_2, at which time diode D_2 changes to the low forward impedance state. From this point, as the clock potential becomes still less negative and then positive, current flows through resistors R_1 and R_2 and diode D_2 from the clock source to the diode junction (D_2, D_4, D_6) at which V_2 is measured. This current does not appreciably change the potential, V_2, but rather, replaces a portion of the current which had been flowing through diodes D_4 and D_5 into resistor R_3. Thus the change in V_2 is only the small change in forward voltage drops across these diodes resulting from the decrease in current through them.

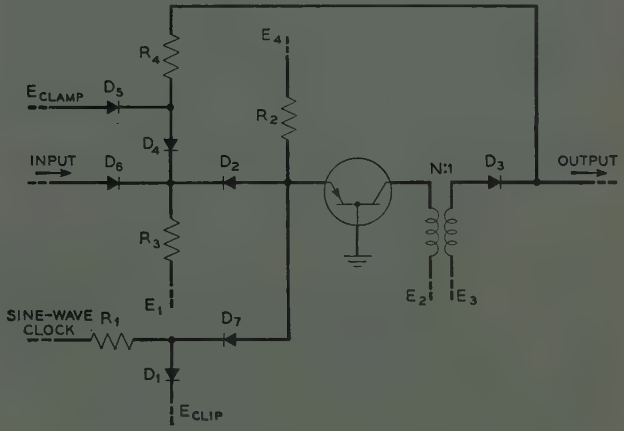


Fig. 3—Regenerative Amplifier II.

When the applied clock voltage becomes sufficiently positive to raise the potential (V_1) at the junction of resistors R_1 and R_2 and diode D_1 to the value $E_{\rm clip}$, diode D_1 begins to conduct. Through this means the clock voltage is clipped, V_1 remaining at E_{clip} (plus the small forward voltage drop across diode D_1) until the positive peak of the clock voltage sine wave has passed and the clock voltage is no longer sufficiently positive to maintain V_1 at E_{clip}. During this clipping interval both V_2 and the emitter potential are essentially constant and the emitter remains slightly below cutoff. As V_1 becomes less positive than E_{clip}, diode D_1 again becomes nonconducting.

---

[1] R. D. Elbourn and R. P. Witt, "Dynamic circuit techniques used in Seac and Dyseac," TRANSACTIONS OF THE I.R.E., vol. EC-2, pp. 2–9; March, 1953.

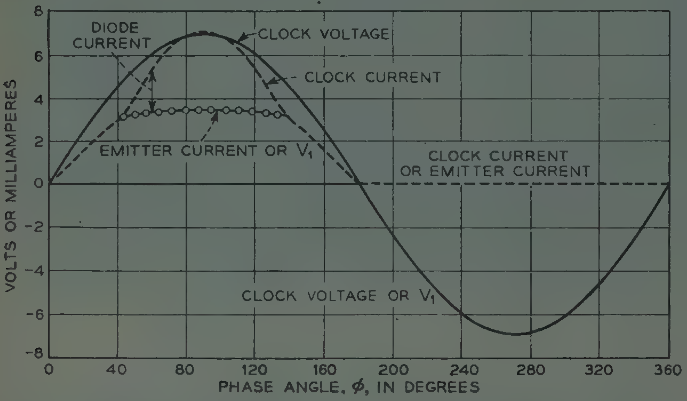


Fig. 4—Voltage and current waveshapes for Regenerative Amplifier I.

The cycle of input circuit operation, with no input signal present, is completed as the clock voltage swings toward the negative peak of the sine wave. Diode D_2 becomes nonconducting as the emitter potential drops below the potential, V_2, which is again clamped by diodes D_4 and D_5 as at the beginning of the cycle. In Fig. 4, waveshapes of some of the input circuit voltages and currents are plotted. The values of the constants which were used for the calculations are those indicated in Fig. 2, with the exception that the emitter is assumed to run at ground potential while the clock potential is positive and at the clock potential when this is negative. These assumptions are reasonably valid whether or not an input signal is present. When no input signal is present, as has been assumed to this point, the curve in Fig. 4 labeled, "V_1 or emitter current," should be interpreted as, "V_1 or current through diode D_2."

Application of positive pulses to the input modifies the performance of the input circuit during the intervals when the clock voltage is positive. For proper operation, which implies that the clock completely determines the timing of the output pulses, the input pulse must be applied prior to the time when the clock voltage swings positive through zero. When this is the case, diode D_2 does not begin to conduct as it does when no input pulse is present since V_2 is more positive as a result of the presence of the input pulse. (The input pulse causes diodes D_4 and D_5 to become nonconducting.) For diode D_2 to conduct, the emitter potential would have to be driven as positive as potential V_2 by the clock voltage. Before this occurs, however, the emitter potential reaches the value[2] at which the transistor emerges from the cutoff region.

After this point has been reached, the transistor emitter characteristic is such that for most external collector impedances a large increase in emitter current can occur with only a slight change in emitter potential. Moreover, this slight change may be either positive or negative, depending on the particular transistor. Thus, essentially the current which flows through diode D_2 when no input signal is present is diverted into the transistor emitter when such a signal is applied.

Voltage-current characteristics for both emitter and collector for a typical unit have been included in Fig. 5. To illustrate the action of the transistor a linear load line has been plotted on the collector characteristic and has then been transferred to the emitter characteristic

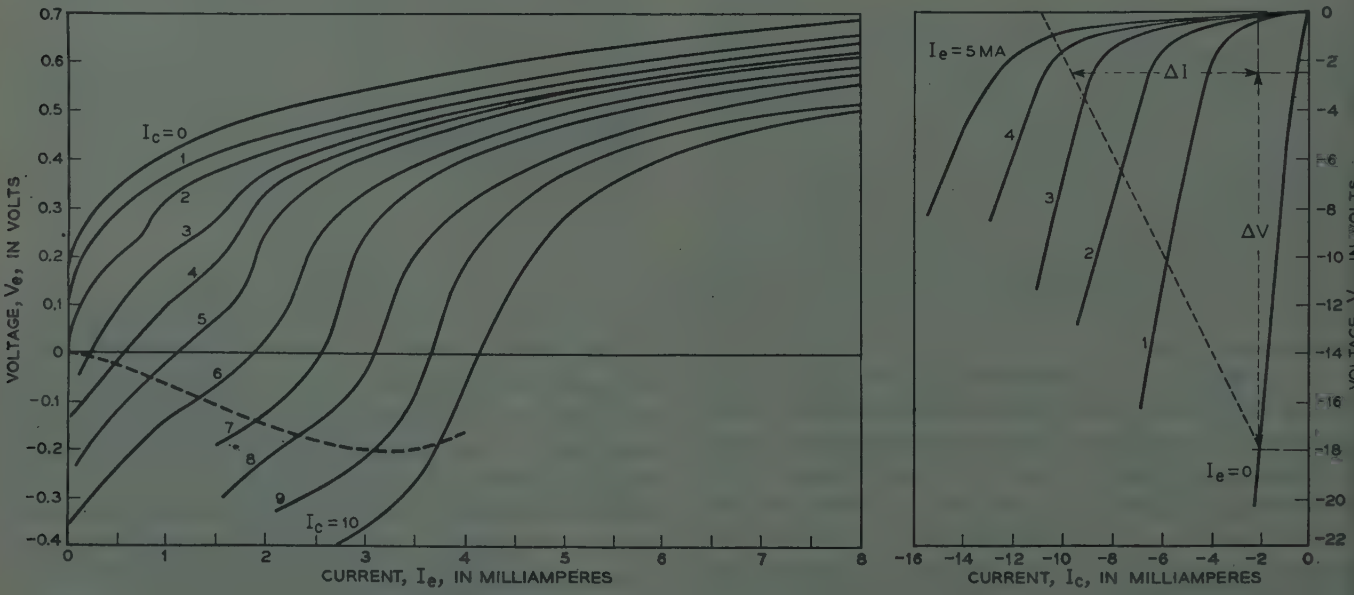


Fig. 5—Transistor characteristics to illustrate development of a pulse.

---

[2] This potential is referred to as the "break point," a term coined by B. G. Farley.

where it is no longer linear. The line, as plotted on the collector characteristic, has a 2000 ohm slope and passes through the point ($I_e=0$, $V_c=-18$). With the particular transistor that was used to obtain the characteristics, a slight negative resistance is evident at the emitter in the region to the right of the break point; another transistor might have displayed a zero, or even positive, resistance in this region.

If the voltages and circuit constants indicated in Fig. 2 are assumed, the presence of an input pulse results in a change in emitter current from a very slightly negative value to a positive value of approximately 3.5 milliamperes. The excursions over the emitter and collector characteristics are indicated by the load lines between these extremities. In Fig. 5 the pulse voltage and current developed at the collector have been indicated as ΔV and ΔI. Since the collector is not driven too deeply into saturation, the unpredictable pulse broadening which results from "hole-storage" is avoided.

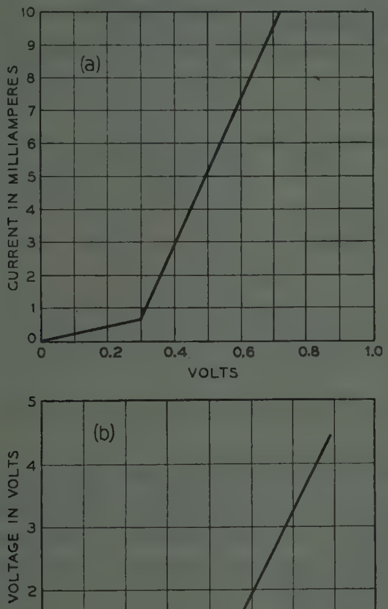


Fig. 6—Straight line approximations to: (a) diode characteristic, (b) regenerative amplifier input characteristic.

In general, the load lines corresponding to circuits which the amplifier will be called upon to drive will not be simple straight lines. In fact, if reactances are disregarded, they are apt to be similar to the characteristic plotted in Fig. 6b, which is a plot of the input resistance of this amplifier when diode D_2 is cut off. To facilitate the calculations for this plot, the 2-straight line approximation to a diode characteristic, shown in Fig. 6a, has been assumed for all diodes. The sharp corner in this assumed characteristic is responsible for the sharp corners in the input resistance characteristic.

As shown in Figs. 2 and 3, the transistor collector is coupled to the load through a transformer and diode D_3. The purpose of the transformer is two-fold. First, it matches impedances (to the extent that non-linear impedances can be matched). Second, it makes possible more satisfactory dc restoration than can be obtained if a condenser is used for coupling. For transistor circuits of this type, capacitive coupling results in a considerable reduction in useful pulse amplitude for a train of pulses as compared to the amplitude of a single isolated pulse. If a properly designed transformer is used, however, the useful amplitude of the pulses can be maintained essentially constant regardless of the number of consecutive pulses.

To obtain complete[3] dc restoration, the total energy stored in the transformer mutual inductance and the shunt capacitance of both the transformer and the transistor output during the pulse should be completely removed prior to the start of the next pulse interval. This cannot be done, however, so it must be approximated as closely as possible. The optimum condition involves a ringing by the transformer (following a pulse) at a frequency of slightly less than 3 megacycles with damping slightly less than critical. To this end, diode D_3 is arranged to effectively disconnect the load from the transformer as the transformer polarity reverses at the termination of a pulse. The transformer ringing frequency and the damping are then determined by parallel combination of transformer mutual inductance, shunt capacity and effective shunt resistance, and the transistor output resistance and capacity.

It should be noted that dc restoration is not obtained without cost. The price paid is the energy stored in the reactive elements during the signal pulse—a greater amount of energy than would have to be stored if no dc restoration were desired.

As indicated previously, an external feedback path is provided for temporary lock-up to assure proper retiming of the pulse. From Fig. 2 it can be seen that diodes D_4 and D_6 constitute an Or-Circuit. Therefore, in returning to the input via diode D_4 and current limiting resistor R_4, the feedback pulse becomes equivalent to the input pulse. Diode D_5 is a low impedance source of current for clamping the potential at the junction of diodes D_2, D_4 and D_6 whenever the clock voltage swings negative. With this current source available, the current need not be supplied through the transformer and a source of 3 megacycle "noise" at the amplifier output is thereby avoided.

The clamping action of diode D_5 would undoubtedly be more effective if its cathode were brought to the junction of diodes D_2, D_4 and D_6. To the present time it has been connected as shown, however, to decrease the possibility of its providing a low impedance shunt across resistor R_3, as a result of poor diode reverse recovery, when an input pulse is present.

---

[3] Complete is used here to indicate a maintenance of the over-all waveform, not merely amplitude.

Photographs of waveshapes at various points in the amplifier of Fig. 2 are included as Figs. 7 and 8. To obtain Fig. 7, a 500 ohm resistive load and a 3:1 transformer turns ratio were employed, whereas, Fig. 8 was obtained with a load consisting of four amplifiers in parallel while the transformer turns ratio was 4:1.

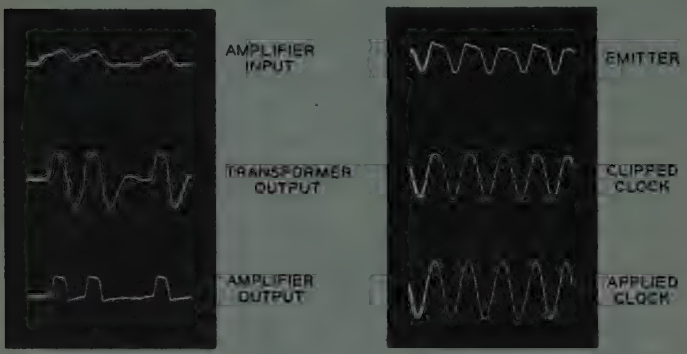


Fig. 7—Photographs of voltage waveshapes at various points of Regenerative Amplifier I. A 500 ohm resistive load and a 3:1 transformer turns ratio were used.

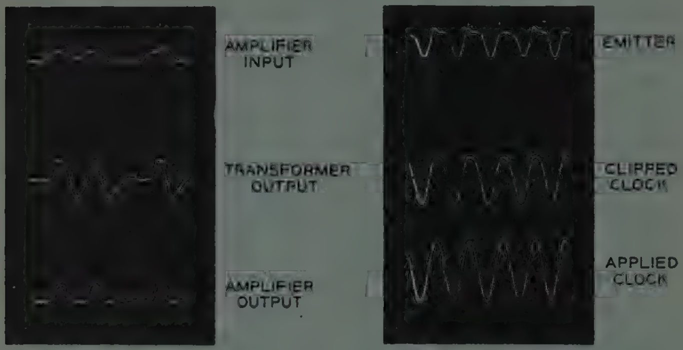


Fig. 8—Photographs of voltage waveshapes at various points of Regenerative Amplifier I. A load consisting of four similar regenerative amplifiers in parallel and a transformer turns ratio of 4:1 were used.

POWER DISSIPATION

For the voltages and circuit constants indicated in Fig. 2, the average 3 megacycle clock power dissipation is approximately 12 milliwatts per amplifier. This figure is substantially the same whether or not the amplifier is being pulsed. On the other hand, the dc dissipation within the transistor is very nearly equal to the product of E_2 and $I_c(0, E_2)$.[4] The exact value, therefore, is directly dependent upon the particular transistor, but is usually less than 50 milliwatts. An additional 25 milliwatts of dc power are dissipated external to the transistor.

COMPARISON OF INPUT CIRCUITS

Two different implementations of the And-Circuit in the input have been indicated in Figs. 2 and 3, respectively. The arrangement of Fig. 2 seems to be superior to that of Fig. 3 in that a slow recovery of reverse impedance in diode D_7 in Fig. 3 is detrimental to the performance of the circuit. If the sine wave clock were applied directly to this diode, the transistor emitter potential could be carried over the break point by each of the positive voltage swings of the clock regardless of the presence or absence of an input signal. A clipping circuit consisting of R_1 and D_1 can be used to alleviate this condition, however, by clipping the positive peaks of the clock voltage at a value slightly more positive than the transistor break point. The normal running potential at the emitter could, of course, be made more negative, but this would necessitate larger input pulses to operate the amplifier.

As might be expected, the analytical expressions defining output pulse rise times are different for the two circuit versions. Specifically, these differences reflect the fact that, for the circuit of Fig. 2, the emitter current is supplied from a sinusoidal clock generator, whereas, for that of Fig. 3, it is supplied from a source of constant potential. A representation, which disregards the transformer and is suitable for either circuit during the rise time interval, is shown in Fig. 9. To differentiate the cases, the applied voltage is a suddenly applied sine wave in one instance and a step function in the other. The only frequency-dependent element introduced into the *tee*-equivalent for the transistor is the mutual impedance, Z_m, which is postulated to have the form:

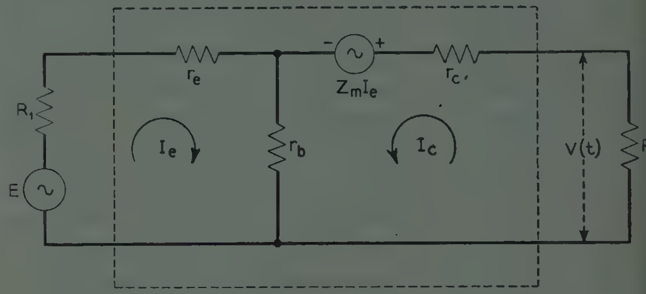


Fig. 9—Equivalent circuit for rise-time analysis.

$$\frac{R_m}{1 + j\dfrac{\omega}{\omega_c}}.$$

In this expression, ω is the angular frequency variable $2\pi f$, and ω_c is the particular angular frequency for which the magnitude of Z_m is down to 0.707 times the d value. The unit step function is represented by th notation, $u(t)$, in the following material.

For the circuit of Fig. 9 the following loop equation can be written in terms of the complex frequency variable, p:

$$[R_1 + r_e + r_b]I_e(p) + r_bI_c(p) = E(p) \qquad \text{(1}$$

and

$$[r_b + Z_m(p)]I_e(p) + [r_b + r_c + R_2]I_c(p) = 0. \qquad \text{(2}$$

From a simultaneous solution of these equations fo

---

[4] $I_c(O, E_2)$ is the collector current corresponding to an emitter current of zero and a collector voltage of E_2.

$I_c(p)$, the expression for $V(p)$ can be readily obtained, since:

$$V(p) = -I_c(p)R_2 = \frac{R_2[r_b + Z_m(p)]E(p)}{[R_1+r_e+r_b][R_2+r_b+r_c]-r_b[r_b+Z_m(p)]}. \qquad (3)$$

Laplace transforms can now be used to obtain the time response, $V(t)$, when the appropriate representations for $E(p)$ are inserted.

Based on these conditions, the equations for the output voltage response are:

For a suddenly applied sine wave described here as $E(t) = E_0 \sin \omega_0(t)\, u(t)$

$$V(t) = \gamma E_0 \left[\frac{(\lambda - \beta)\dfrac{\omega_c}{\omega_0}}{\left(\beta \dfrac{\omega_c}{\omega_0}\right)^2 + 1} \epsilon^{-\beta\omega_c t} + \sqrt{\frac{\left(\lambda \dfrac{\omega_c}{\omega_0}\right)^2 + 1}{\left(\beta \dfrac{\omega_c}{\omega_0}\right)^2 + 1}} \sin(\omega_0 t + \psi) \right] \qquad (4)$$

(applies to the circuit as shown in Fig. 2), and for the step function where $E(t) = E_1 u(t)$

$$V(t) = \gamma E_1 \left[\frac{\lambda}{\beta} - \left(\frac{\lambda}{\beta} - 1 \right) \epsilon^{-\beta\omega_c t} \right] \qquad (5)$$

(applies to the circuit of Fig. 3) where:

$$\beta = \frac{[(R_1 + r_e + r_b)(R_2 + r_c + r_b) - (r_b + R_m)]}{(R_1 + r_e + r_b)(R_2 + r_c + r_b) - r_b^2}$$

$$\gamma = \frac{R_2 r_b}{(R_1 + r_e + r_b)(R_2 + r_c + r_b) - r_b^2}$$

$$\lambda = 1 + \frac{R_m}{r_b}$$

$$\psi = \phi_1 - \phi_2$$

$$\phi_1 = \tan^{-1} \frac{\omega_0}{\lambda\omega_c}$$

$$\phi_2 = \tan^{-1} \frac{\omega_0}{\beta\omega_c}.$$

Generally λ is much larger and β slightly smaller than unity. In addition, ω_c/ω_0 will be considered only for values of unity or greater, so the following approximations are usually satisfactory:

$$\lambda - \beta \sim \lambda$$

$$\lambda/\beta - 1 \sim \lambda/\beta$$

$$\sqrt{\left(\lambda \frac{\omega_c}{\omega_0}\right)^2 + 1} \sim \lambda \frac{\omega_c}{\omega_0}$$

$$\tan^{-1} \frac{\omega_0}{\lambda\omega_c} \sim 0.$$

With these approximations, (4) can be reduced to:

$$V(t) \sim \gamma\lambda E_0 \frac{\omega_c}{\omega_0} \left[\frac{1}{\left(\beta \dfrac{\omega_c}{\omega_0}\right)^2 + 1} \epsilon^{-\beta\omega_c t} + \frac{1}{\sqrt{\left(\beta \dfrac{\omega_c}{\omega_0}\right)^2 + 1}} \sin(\omega_0 t - \phi_2) \right] \qquad (6)$$

and (5) can be reduced to:

$$V(t) \sim \frac{\gamma\lambda E_1}{\beta}(1 - \epsilon^{-\beta\omega_c t}). \qquad (7)$$

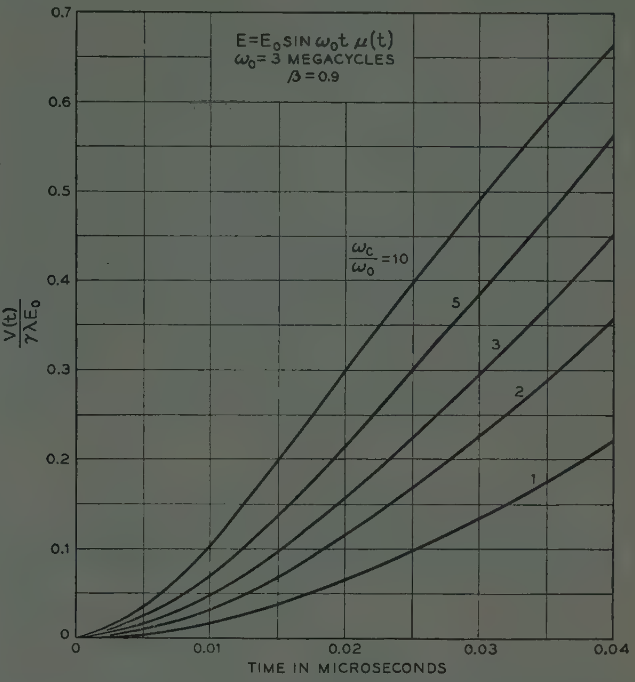


Fig. 10—Graphical illustration of the influence of transistor cutoff frequency in determining pulse rise time of Regenerative Amplifier I.

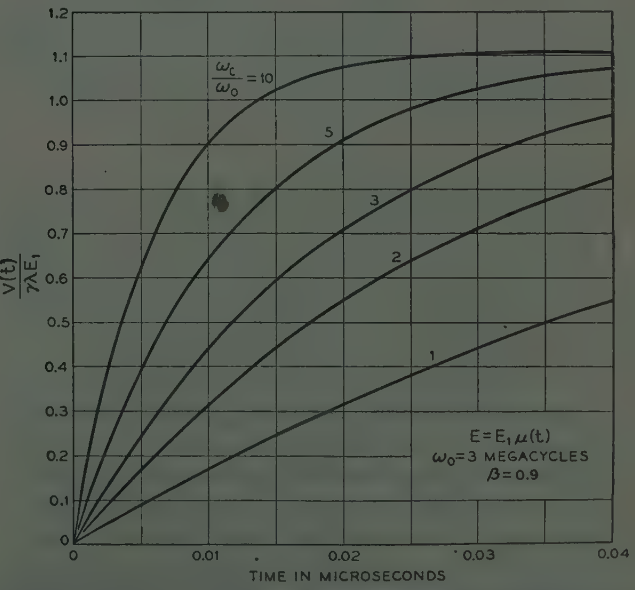


Fig. 11—Graphical illustration of the influence of transistor cutoff frequency in determining pulse rise time of Regenerative Amplifier II.

(4) and (6) are, of course, valid only prior to the time when the clipping of the clock commences.

It is evident that the circuit of Fig. 3 is superior to that of Fig. 2 with regard to rise time. This follows from the fact that the limiting best response obtainable by (6) is sinusoidal, whereas, (7) indicates a limiting best response which is a step function. Use of a square-wave clock with the circuit of Fig. 2 can nullify this difference, however, if a satisfactory clock source of this type is available. As a substitute, a sinusoidal clock voltage with excessive amplitude could be used with the clipping level unchanged, but this is wasteful of clock power.

Other rise time information is conveyed by the equations. For instance, increasing the load resistance, R_2, can shorten rise times if the transistor is driven to saturation. Increasing R_2 has the effect of increasing the multiplying factor, γ, and thereby causes $V(t)$ to rise toward a greater ultimate value. When the transistor collector reaches the saturation region, where further increases in emitter current produce little change in collector current, $V(t)$ is arrested at a maximum value which is less than the ultimate value indicated by the equations. Since either a sinusoidal or an exponential rise in being halted short of a goal, a reduction in rise time is effected.

Also useful for providing shorter rise times are transistors for which λ is large, in that they can more rea ily be driven to saturation. To a certain extent, λ is measure of transistor gain and it can be seen that is a multiplying factor in both response expressions. should be pointed out again, though, that pulse broa ening is apt to result from "hole-storage" if the unit driven too deeply into saturation.

Figs. 10 and 11 are included to indicate the extent which transistor cutoff frequency influences rise tim They have been plotted from (6) and (7), respectivel for the single case of an assumed β of 0.9. In either figu the higher cutoff frequencies produce the shorter ris times, as expected, but a point of diminishing returns reached. It is interesting to note than when transisto are driven into the saturation region, gain can traded for cutoff frequency and vice versa. Still, be over-all performance is obtained with transistors havin both a high cutoff frequency and large current gain.

ACKNOWLEDGMENTS

This work on the regenerative amplifier has been don under contract with the Bureau of Ordnance of th U. S. Navy.

The author wishes to acknowledge the many usefu discussions with W. A. Cornell and Q. W. Simkins, an test work done by W. Kaminski and M. F. Wazowic

---

Coded Decimal Number Systems for Digital Computers[*]

GARLAND S. WHITE[†], STUDENT MEMBER, IRE

Summary—In this paper, basic properties of coded decimal number systems are presented, extending the discussion of "Synthesis of Electronic Computing and Control Circuits."[1] From the very large numbers of possible ways of coding the ten decimal digits into sets of binary elements, a restricted group of number systems is presented as being particularly adaptable for representing the decimal digits in digital computers. As an example, one number system of this group is presented which permits the construction of a very simple addition circuit.

I. INTRODUCTION

THE PROBLEM TO BE considered here is that of representing decimal digits with binary elements in digital computers. The choice of coded decimal number system effects the number of circuit elements required in a computer and the proper choice can minimize the number of circuit elements required.

Decimal digits are represented in electronic computers by binary elements such as the Eccles-Jordan Trigger Circuit. This is because circuits of this type are easily constructed, they function fast, and they are reliable.

Since by definition a binary element has two stable states, n binary elements have 2^n stable states. Thus, for the representation of the ten decimal digits at least fou binary elements must be used with 16 possible ways t represent a digit. The extra six may, however, be utilized for automatic checking purposes, thus partly compensating for this loss of efficiency.

The proper choice of ten of the sixteen possible ways to represent each digit can greatly simplify the construction of the arithmetic elements of computers. The main elements that are affected are those which perform the following functions:

1. Addition, either instantaneous or sequential.
2. Counting, up or down.
3. Complementing.
4. Conversion from decimal digits to coded digits (input) or from coded digits to decimal digits (output).
5. Automatic checking.

Before appropriate coding schemes can be chosen, a knowledge of their basic properties is needed.

II. BASIC PROPERTIES OF CODING SCHEMES

The sixteen possible combinations of four binary elements are listed in Table I on page 1451. The four binary elements are represented by X_1, X_2, X_3, and X_4, their states are represented by zeros and ones, and the binary sequence is listed as zero through fifteen.

---

[*] Decimal classification: 621.375.2. Original manuscript received by the Institute, May 27, 1953.

[†] Computer Laboratory, University of California at Berkeley.

[1] Staff of the Computation Laboratory, Harvard University Press, Cambridge, Mass., pp. 145–156; 1951.

TABLE I

All possible combinations of the states of four binary elements

Binary Sequence	X_1	X_2	X_3	X_4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

The values given for X_1 to X_4 in any of the above rows could be used to represent any one of the ten decimal digits. There are therefore, $16!/6!$ or 2.9×10^{10} possible coding systems. However, not all of these are essentially different because of properties of Table I. Interchanges of columns, or of zeros and ones,[1] reduce the total number of essentially different schemes to $16!/6!$ (384) or 7.6×10^7 basic coding schemes. There are still an enormous number of codes from which to choose.

One method of choosing a coding scheme assigns a "weight" to each column in Table I; for example, if $X_1=1$, $X_2=2$, $X_3=4$ and $X_4=8$ then the significance of each row is given by the arabic number at the left in Table I, and the first ten rows provide a coded-decimal scheme. This scheme is commonly referred to as the 1, 2, 4, 8 system.

Another method of choosing a coded decimal number system is to choose the first five and the last five rows of Table I. This is the number system chosen by Prof. Aiken at Harvard for use in the Mark III Calculator. With this number system the binary elements may be assigned the weights 1, 2, 4, 2; it is referred to as the 1, 2, 4, 2^+ system.

Still another method of coding the decimal digits is by use of the middle ten rows of Table I. This is the well known "excess 3" system and is used in the "Univac" of the Remington Rand Corp.

The 1, 2, 4, 8 and the 1, 2, 4, 2^+ systems are members of a restricted group of coding systems that allows constant positive weights to be assigned to the binary elements. The groups of positive weights that may be assigned to the binary elements may be listed by noting that one of the weights must be one, another either one or two and the sum of the weights must be not less than nine nor greater than fifteen. These groups are listed in Table II.

TABLE II

Groups of positive weights that may be assigned to the binary elements

V_1	V_2	V_3	V_4
1	2	3	3
1	2	2	4
1	1	3	4
1	1	2	5
1	2	3	4
1	2	4	4
1	2	2	5
1	1	3	5
1	2	3	5
1	2	4	5
1	2	2	6
1	1	3	6
1	2	3	6
1	2	4	6
1	2	3	7
1	2	4	7
1	2	4	8

The number of systems that are contained in each group may be determined by noting the number of ways each digit could be coded in a particular group of positive constant weights. For example, in the 1, 2, 2, 4 systems the 2, 3, 4, 5, 6, and 7 can each be coded in two different ways. In this case one-half the product of all the numbers of ways each digit can be formed gives the total number of basic systems. In this group the total is 32. The reduction by one-half is necessary because of the equality of two weights in this group of systems. The groups of weights are reproduced in Table III with the number of basically different schemes of coding the decimal digits for each group. In all these schemes the rows of Table I are used in order, that is, each scheme uses the first row for 0 and chooses for 1, one of the next rows, then for 2, one of the rows below that for 1, and so on.

TABLE III

Number of basically different ways of coding the decimal digits for each group of positive constant weights

Groups of Constant Positive Weights				Number of basically different ways of coding the Decimal Digits
X_1	X_2	X_3	X_4	
1	2	3	3	18
1	2	2	4	32
1	1	3	4	18
1	1	2	5	32
1	2	3	4	32
1	2	4	4	8
1	2	2	5	16
1	1	3	5	16
1	2	3	5	16
1	2	4	5	8
1	2	2	6	8
1	1	3	6	4
1	2	3	6	8
1	2	4	6	4
1	2	3	7	2
1	2	4	7	2
1	2	4	8	1
				Total 225

The constant weight systems have distinct advantages over the variable weight systems, such as ease of interpretation and the possibility of operating with a part of a digit. For example, in sequential addition the addition of two digits is accomplished by adding to one digit, appropriate weights of the binary elements of the second digit in succession. The remainder of this paper is devoted to the constant positive weight systems.

Of the 225 systems indicated in Table III, 14 have the useful property that the replacement of zeros by ones and ones by zeros of the representation of any digit will produce the "nines" complement. This feature exists when each digit and its complement have been chosen symmetrically about the center of Table I. Column (e) of Table IV is so chosen, column (a), (b), (c) and (d) are not.

TABLE IV

Five examples of ways to code the ten decimal digits using the weights 1, 1, 2, and 5

Digit	(a)	(b)	(c)	(d)	(e)
	1125	1125	1125	1125	1125
0	0000	0000	0000	0000	0000
1	1000	1000	1000	1000	1000
2	1100	1100	0010	0010	1100
3	1010	0110	1010	0110	0110
4	1110	1110	1110	1110	1110
5	0001	0001	0001	0001	0001
6	1001	1001	1001	1001	1001
7	1101	1101	0011	0011	0011
8	1011	0111	1011	0111	0111
9	1111	1111	1111	1111	1111

The properties of the systems listed in Table IV are quite different, for example, the number of grids or crystal diodes required for a sequential adder in the system of column (a) is 8; column (b) 14; column (c) 14; column (d) 18; and column (e) 43. A sequential adder is the simplest type of adder possible in a computer employing a decimal coded system, and its use is possible only when the binary elements are assigned constant weights.

The groups of constant positive weights that include coding schemes that can be complemented by the direct inversion of the states of the binary elements are shown in Table V.

TABLE V

The number of constant positive weight systems that can be complemented by direct inversion of the states of the binary elements

Groups of Constant Positive Weights				Number of Systems that Can be Complemented by Direct Inversion
1	1	2	5	4
1	2	2	4	4
1	1	3	4	3
1	2	3	3	3

Use of one of these systems would simplify a complementing computer element, but complicate the adder.

III. A PREFERRED GROUP OF NUMBER SYSTEMS

The properties of the coded decimal number system of column (a), Table IV, make it a particularly good choice for computer applications in that the number of circuit elements required for the functions indicated earlier are less than the number required by the popular systems in use at the present time. This coded decimal number system was found in a search for a number system that would allow the use of a minimum number of crystal diodes in a sequential adder.

In order to show some of the features of this number system as compared with those of the 1, 2, 4, 8 system and the 1, 2, 4, 2^+ system mentioned, the number of grids or crystal diodes needed to perform the indicated functions are shown in Table VI.

TABLE VI

Comparisons of features of system proposed by author with those of the 1, 2, 4, 8 system and the 1242^+ system

Function	Number of Grids or Crystal Diodes Required to Perform Function		
	1242^+ system	1248 system	System of Table IV
1. One Word Time Addition	90(approx.)	80 (approx)	20
2. Sequential Addition	47	19	8
3. Counting up	12	8	2
4. Complementing	0	2	4
5. Conversion from Decimal Digits to Coded Digits or from Coded Digits to Decimal Digits	28	30	25
6. Forbidden-digit Check	12	4	4
Total	189	143	63

Table VI shows that not only are more economical arithmetic elements possible with the proposed system but that more reliable computing systems should result from the use of this system.

The proposed system is one of a group of eleven systems that have the property that one binary element has a weight of five and the states of the other three binary elements from the decimal digits zero through four are reproduced from five through nine. The groups of constant positive weights that include the systems of this restricted group are shown in Table VII.

TABLE VII

Groups of constant positive weights that include systems of the restricted group

Groups of Constant Positive Weights				Number of Systems Included in the Restricted Group
1	1	2	5	4
1	1	3	5	2
1	2	2	5	2
1	2	3	5	2
1	2	4	5	1
				Total 11

All of the systems of this restricted group are comparable in equipment requirements to the proposed system shown in column (a), Table IV.

IV. CONCLUSIONS

Although this article has been almost entirely concerned with constant positive weight number systems, the possibility that variable-weight systems may be better in some cases is not excluded. There are no universal criteria for the choice of an optimum coded decimal system. The choice should, obviously, depend upon what arithmetic elements are to be built into a given computer. Simple formulas for choosing, and answers to many other questions concerning number systems will have to wait on advancements of the theory of switching functions.

ACKNOWLEDGMENTS

The author gratefully acknowledges the suggestions of Professors Paul L. Morton and Torben H. Meisling, Division of Electrical Engineering, University of California at Berkeley.

An Electromagnetic Clutch for High Accelerations*

S. M. OSTER† AND L. D. WILSON†, MEMBER, IRE

***Summary*—Certain of the design considerations, construction detail and performance data are presented on a low-inertia electromagnetic clutch used to satisfy high-acceleration requirements. The clutch has many possible applications in the digital computer field. Unidirectional and bidirectional models are discussed.**

INTRODUCTION

ONE OF THE REQUIREMENTS frequently imposed on high-speed magnetic tape devices used as auxiliaries to a digital computer is short starting and stopping time. There are several reasons why it is desirable to minimize the time consumed in starting and stopping the tape. First of all, where a magnetic tape performs the functions of a computer memory, access time must be reduced to a minimum in order to increase the versatility of the memory. More important, the time during which the processing circuits are interrupted for read-in and read-out must be minimized. Furthermore, since both the recording and reading processes require uniform tape velocity to achieve uniform signal, the tape must be accelerated rapidly to recording-reading speed to save tape.

Low-inertia motor-and-capstan systems require high-performance servo-mechanisms and cannot produce sufficiently low start-stop times because the entire system must be accelerated from the halt. Some constant-speed capstan systems have incorporated the tape as a part of a clutching arrangement: a jam-roller or pressure shoe engages the tape for accelerations. This system, although it provides extremely short acceleration times, is destructive to the tape because of the friction resulting from the sudden engaging of the pressure shoe or roller. The electromagnetic clutch described in this paper was developed as a component of a high-speed tape transport system in an attempt to compromise between ideally short-start stop times on the one hand, and system and tape life on the other.

The principle of the design takes into account the fact that time is consumed when a clutch is engaged by the travel of a drive member to the clutch facing. This delay can be reduced by maintaining constant contact between drive member and facing at a low pressure insufficient to permit power transfer, and increasing this pressure to engage the clutch. Such a design requires a precise alignment between drive members, facings, and clutch pressure disc, so that the constant contact will not cause local wear on any of the components (as would result if opposed faces were not parallel). If the facing material possesses a slight compliance, the tolerances in the construction of the clutch are not as severe in this respect.

A second requirement is that the driven members possess a very low inertia. Excluding the heavy iron components of the magnetic circuit from the driven elements of the clutch helps meet this requirement.

In the clutch discussed here the constant-velocity elements of the system possess a combined inertia much greater than that of the driven elements; the travel of the clutching components is small; and the actuating magnets are rapidly driven to saturation.

A unidirectional model of the clutch assembly is illustrated in Fig. 1(a) and (b). The driving motor of the system (not shown) is a 1/15 hp induction motor, fixed to the clutch-side flexible coupling. The three pieces of the flexible coupling cannot turn with relation to each other, but the output side of the coupling is permitted a certain free axial travel with respect to the driving side. The output coupling is fixed to a drive armature-and-thimble.

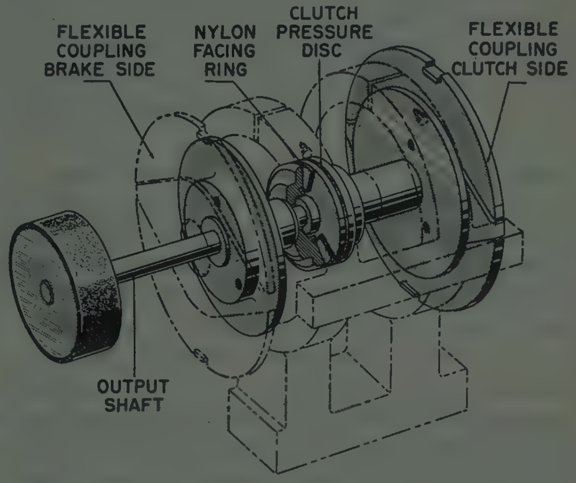


Fig. 1(a)—Cutaway view, unidirectional clutch.

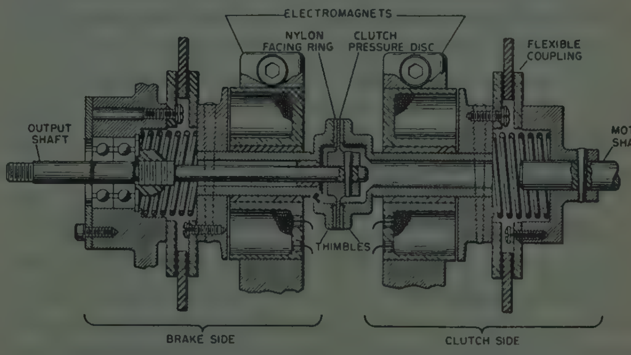


Fig. 1(b)—Orthographic view, unidirectional clutch.

Inside the flexible coupling is a light spring, which loads the armature so that its thimble impinges on one surface of an annular nylon facing. The facing material

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, June 24, 1953.

† Eckert-Mauchly Div., Remington Rand, Inc., Philadelphia, Pa.

has a compliance to compression which, although slight, is approximately one hundred times greater than, for example, that of steel. It is 0.062 inch thick, with scavenging grooves, and rides against the clutch pressure disc, which is 1 3/16 inches in diameter and made from hardened, ground steel.

On the other side of the pressure disc a similar facing, thimble, armature, and flexible coupling act as a braking mechanism. The brake coupling is fixed to the assembly housing.

Since both armatures are spring-loaded, either could take effect if no power was applied and the system were perfectly balanced. However, the tape transport system in which such a clutch assembly is incorporated contains a provision for actuating the brake side automatically when the power is turned on.

The coils of the actuating electromagnets are multiple-layer solenoids, mounted around the shafts of their respective thimbles. The armature at the other end of the shaft forms a part of the magnetic return path of the solenoid. The fixed positions of the electromagnets makes slip-rings unnecessary; the power leads are brought in directly to the coils. Furthermore, no part of the magnetic circuit is on the driven side of the clutch. The inertia of the clutch output is thereby reduced.

Various sizes of wire in different numbers of turns were tried, with equal success. All coils were wound with the same inner diameter and the same length of magnetic path. With a 0.004 inch gap between the side of the solenoid and the face of the armature, the coils saturated at approximately 600 ampere-turns. The saturation torque measured in a static torque test was 210 oz-in.

A square-current wave form with a short pulse superimposed on its leading edge is applied to the coil. This type of waveform is used in order to compensate for the eddy currents set up in the magnet-core, and to drive the coil rapidly to saturation. Actually, the value of the peak power overshoots the requirements of the electromagnet, but is used in overcoming the eddy currents. To further suppress the eddy effect, the magnet is slotted, so that the outer shell of the core, which would act like a shorted turn around the coil, is to some degree interrupted. The rise time for the initial surge current is between 0.15 and 0.2 ms, and the flux is established in approximately 0.4 ms, the additional time being that required to overcome the eddy currents. The rated maximum peak-voltage across the coil is 1,000 volts. At present, the peak-power input to the magnets is 600 va. The use of certain alloys possessing higher values of resistivity but substantially the same saturation flux density promises to reduce this figure considerably.

The flexible coupling which drives the armature permits a small axial travel, as was mentioned earlier. When the magnetic flux is built up, the armature tends to close to the electromagnet, pressing the thimble hard against the nylon facing. Since the thimble and facing normally just touch, the distance traveled by the armature in response to the magnetic pull is extremely small, on the order of 0.0001 inch or less. The facing turns the pressure disc and the output shift.

The inertia of the output shaft and the pressure disc is 11.2 gm-cm^2, which produces a torque-to-inertia ratio (using the static-torque test figure) of 1.32×10^6 rad/sec^2. With the addition of a 20 gm-cm^2 load, the ratio becomes 4.75×10^5 rad/sec^2. At the designed input speed of 2,000 rpm, the allowable combined radial and thrust load on the output shaft is four pounds.

Performance measurements have shown that the actual time required to accelerate a 20 gm-cm^2 external load to and from 1,755 rpm (the speed at which one tape system performs) is 1.2–1.4 ms, which includes the 0.4 ms necessary for establishing the flux in the magnet. Although the clutch was designed to operate at these speeds, they are not necessary in most tape transport systems. For tape transport purposes, therefore, the system is operated with reduced power input, and the acceleration time is permitted to increase to 2–2.5 ms.

The braking process is accomplished in the same way as clutching. The angular relationship of the thimble, armature, and flexible coupling is fixed, and the coupling is bolted to the assembly housing. The electromagnet causes the brake thimble to engage the second facing, and the other side of the pressure disc. The disc is, of course, released from the effect of the clutch, and deceleration to zero velocity takes place in the same length of time as full acceleration.

The thrust of the output shaft in either direction is taken up by the ball bearings on which the shaft rides at its output end.

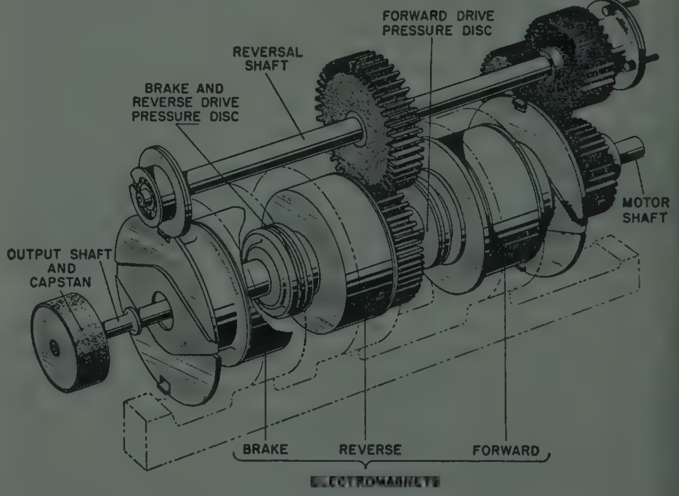


Fig. 2—Bidirectional clutch.

A somewhat more complex design problem is presented by the necessity for movement in two directions. The basic principle just described can be expanded to accommodate rotations at more than one speed and in either or both directions. The use of a clutch obviates the necessity of reversing large-inertia motors, or using two or more motors.

Fig. 2 shows a one-speed bidirectional system, driven, as before, by a constant-speed motor. The change in direction is accomplished by means of a gear train with a 1:1 ratio. Various speeds could be achieved through the use of different ratios, while alternate directions of rotation require only the inclusion or omission of idlers.

In the illustrated system the basic components are the same as those for the unidirectional system. The output shaft is longer, and another pressure disc has been added to accommodate the reverse drive. The motor shaft rotates continuously, driving the gear train and the flexible coupling. Because of the idler in the primary train, the upper power shaft rotates in the same direction as the motor shaft; in the secondary gear train at the center of the drawing, this is reversed so that the second armature turns opposite to the first. The brake armature and coupling are bolted to the housing. The reverse and brake thimbles operate on the center pressure disc, while the forward drive thimble closes on the pressure disc at the upper right.

The inertia of the pressure discs and output shaft is 19.2 gm-cm², and the torque-to-inertia ratio resulting is 7.70×10^5 rad/sec². Adding a 20 gm-cm² load, the ratio becomes 3.78×10^5 rad/sec². The increase in acceleration time due to the added disc and the longer shaft is 0.3 ms.

The electromagnets are energized by the same type of pulsed waveform used in the one-speed clutch, and respond in the same fashion. The three inputs must be synchronized so that no more than one electromagnet is energized at a time. Normally the activating signals are so synchronized that the brake is engaged and all clutches are disengaged during the "no signal" condition.

ACKNOWLEDGMENT

The authors wish to express their appreciation to the members of the Remington Rand organization for contributing to the work reported in this paper and to F. J. Leary for his assistance in preparing it.

A Survey of Analog-to-Digital Converters*

HARRY E. BURKE, JR.†, SENIOR MEMBER, IRE

Summary—This paper discusses many of the techniques now in use for converting analog information into digital form. Some of the more important reasons for this conversion are outlined and pertinent characteristics of conversion are indicated. Simplified sketches are used to illustrate seventeen basic principles of conversion. The description of an automatic data processing system is used to demonstrate the advantages that can result from instrumentation designed around an analog-to-digital converter.

INTRODUCTION

A GOOD MANY YEARS AGO Aesop told a story about a grain miser whose horde was raided by ants that silently crept through cracks, into his warehouse, to extract his store kernel by kernel. It is easy to picture the frustration of this wretched man, opening his granary doors one day to find his treasure gone. Today, engineers and scientists are frustrated by a reverse situation—they want to empty their storehouses of raw information, but succeed in doing it only "kernel by kernel," or point by point. Raw data continue to pile up at such a rate that research laboratories and test facilities are overflowing with unreduced information. Manometer tube photographs, theodolite records, frequency-modulated carriers on magnetic tape, galvanometer deflections from recording oscillographs, strip-charted pen gyrations, are gathering dust despite a frantic effort to reduce them to useful engineering conclusions.

There is now available a technique to help break this bottleneck, and to accelerate the tedious data-reduction process to a point where it at least approaches the speed at which raw data can be generated by modern instrumentation. This technique is that of analog-to-digital conversion, and it is already far beyond mere engineering curiosity. A wide variety of instruments has already been designed and used to prove the value of this approach.

The term "analog" is used here to describe a dependent parameter that varies by some ratio in the same manner as does some independent parameter. For instance, the voltage generated by a thermocouple is analogous to the temperature differential experienced by the couple, and is hence an analog voltage. In the same manner the deflection of a galvanometer, the shift of a carrier frequency, or the rotation of a shaft can be continuously proportional to some other varying physical quantity, to become analog functions. Fig. 1(d) is a curve describing some such function, and is essentially an analog plot. Analog functions are characterized by being continuous in nature, with an infinite number of values.

The term "digit" implies discontinuity, for instance, the presence or absence of some finite symbolism describing the phenomena. Fig. 1 illustrates a typical function by means of an analog plot and by certain digital presentations. Fig. 1(a) describes the function of (d) by means of familiar Arabic symbols, while (b) and (c) are typical binary records of the same information. Roman numerals or Egyptian pictures could have been shown with equal significance. The term "binary" (or two-state) here means the presence or absence of one type of symbol in a geometric location coded to some special significance. For instance, a hole may be punched in a card. This hole is a binary mark, in that

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, April 27, 1953. Presented at the AIEE-IRE-ACM Computer Conference, New York, N. Y., Dec. 12, 1952.

† Consolidated Engineering Corp., Pasadena, Calif.

either there *is* a hole or there *isn't* a hole. This hole can then be made to take on a decimal-digital form by its location on the card. If datum points are to be assimilated by the human brain with the minimum of effort the presentation should be in a tabular Arabic form, as this best matches the brain's previous training. On the other hand, machines do not have the versatility of the brain, and they work best on a binary signal. So, machine assimilation of data is usually carried out through some binary-coded data-handling system.

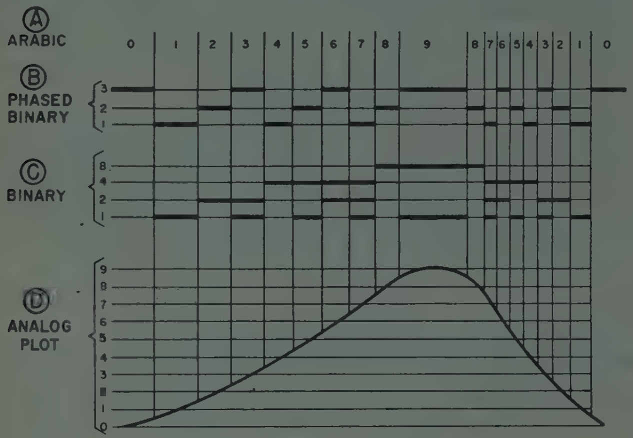


Fig. 1—Typical digital presentations.

The analog-to-digital converter is a device interposed somewhere between the analog input information and the tabular, or binary-stored, output information. Digits result in uniform, rapid, and accurate data processing. In the past, engineering data has often been considered to be accurate only to plus or minus one per cent of the full-scale capabilities of the data-handling system. A good part of this feeling has arisen from the knowledge that an analog system tends to shed some accuracy each time the data is processed, or each time it passes from one instrument in the system to another. One-per cent system accuracy is then about all that can be economically attained in an extensive analog system. Digital information, however, can be processed and reprocessed with no loss in accuracy, and systems capable of handling data accurately to plus or minus one-tenth of one per cent of full scale can be economically assembled. The accuracy of a digital system is almost entirely a function of the accuracy of the creation of the original digits, and, once the digits are available, the problem of processing is a relatively minor one. Digital information is now being transmitted over radio links, through computers, into recording devices and the like, with excellent reliability. The key to such a system is the analog-to-digital converter.

CHARACTERISTICS

A survey of analog-to-digital converters shows that many exceedingly ingenious ideas have been developed into useful instruments. A casual examination of these instruments might lead to the impression that they share few features in common, but there are certain characteristics that apply to all of the converters discussed here.

The measurement of an unknown quantity generally establishes its relationship to some known, standard reference quantity. The process of analog-to-digital conversion is essentially a measurement, so somewhere in every converter there must be a standard. Of necessity, this standard will have the same physical characteristics as has the quantity to be digitized. Precision components such as resistors or condensors, precise units of distance or rotation, and standard voltages are all used as references where appropriate. Some functions are more readily standardized than are others, so they are probably easier to digitize. No converter will perform with more accuracy or stability than is demonstrated by its standard.

The output signal of all of these converters falls into one of three categories. The first of these is mechanical "coded-contact-closures." This is exemplified by the type of signals produced by relays or commutators. The advantage of such a signal form lies in its universality, as there is generally no problem of synchronization, impedance matching, or signal-level matching between the converter and the device accepting the digits. For higher speed applications, one disadvantage is that it takes more time to operate a mechanism than it does to energize a purely electronic device. The second category is "coded-buses." Here a vacuum tube can control the presence or absence of a signal on a bus wire. This sort of system has speed advantages, but requires careful matching of the output signal into the receiving instrument. The third category is a "pulse-code," such as is used by telegraphers to transmit information of all kinds. Here, simplicity of transmission equipment is important but the transmitted signals must be stored somehow before they can be decoded. The first two coding techniques might be considered to be "space" codes, while the third is a "time" code.

All of the converters described here operate from some form of "binary" signal, i.e., a contact *is closed*, or it *is not;* a bus line *is energized*, or it *is not;* a specific period of time *is occupied* by some event, or it *is not.* The presence or absence of a particular binary condition in space, time, or space and time is then arranged to have the intended significance. If Arabic decimal information is desired, it can be accomplished by binary-coding ten bus wires in such a way that only one of the ten is ever designated at one time. These bus wires are then used to energize the proper Arabic symbol in some manner. This action is typified by the operation of a typewriter keyboard, where the binary pressure—there is either pressure or there isn't—on a key produces the number engraved on the type bar. Fig. 1 includes two examples of the many possible binary codes. Fig. 1(b), labeled "phased binary," is coded to indicate incremental steps in either the plus or minus direction. This is a space-time code where the change of signal from line 1 to line 2 (also 2 to 3, and 3 to 1) indicates a plus step, while the change from line 3 to line 2 (also 1 to 3, and 2 to 1) indicates a minus step. The important information of such a system lies in the sum of the number of plus and minus steps that transpire in describing the analog equivalent. Fig. 1(c) is a fairly common system often called "binary," where the code spaces are allocated significance in the order 1, 2, 4, 8, 16, 32, and so forth. In this system combination codes fill in the numbers between the designators. Fig. 1 is intended to illustrate the term "digit" and certainly does not give every possible example of a digit. The number of possible codes seems to be limited only by the total imagination of the instrument designers.

The term "digit" is inextricably coupled with the term "toggle." It has already been pointed out that a digital system is a discontinuous one, and it is usual that some kind of toggle action provides the required discontinuity, or the rapid change from one state to another. Relays, vacuum tubes, detents, can be used to furnish this required toggle action. If the analog input signal changes in value over one full unit, the digital output signal should flip, or toggle, from one digit to the next at some point during this change. This toggle action is one of the factors that prevents ambiguity in the number read from the converter, as only one number should be readable at any one instant. Toggle action is required for each digit-to-digit step, but in a decimal-digital system it is also required at a carry point, such as one experiences in changing from a count of 99 to 100, or from 30 to 29. Here the toggle action becomes more complicated, as several digits must correctly toggle if correct readout information is to be available. In a decimal system, carry-toggle action of this kind is accomplished by an interchange of information between the decimal digits.

A description of an analog data-processing device usually includes some discussion as to its frequency-response characteristics. This method of comparing similar devices is so useful that attempts are often made to couple the terms "frequency-response" and "digit" together. In defining the frequency response of such a system, the number of samples required per cycle to describe the input signal must first be determined. It has been shown that only two samples-per-cycle, at the highest frequency of interest, are actually needed, but there is a general feeling that more than these are usually desired. It is suggested that the term "samples-per-second" be used in reference to devices of this type, instead of applying a cyclic caption to a sampling process. Some analog-to-digital converters are constructed so that they can actually follow an input signal through its various changes with time if these changes are not too rapid. Under these conditions it is possible to sample the signal each time it changes by one digit, or to sample in equal time intervals which are short enough to give the information desired. Another type of converter searches the entire range of possible values for the correct answer, and requires the same period of time for any sample of the analog signal, regardless of its value. If comparisons are made between converters as to their maximum sample rates, it should be noted whether this is a rate based on the digit-to-digit speed or on the zero-to-full-scale speed.

Accuracy, stability, linearity, and resolution are all subjects that apply to the process of analog-to-digital conversion in much the same way that they apply to an analog process. For this reason it is felt that they need not be discussed in detail here, except for two special cases. Assuming a converter has been constructed so that the input and output signals are reasonably compatible, the stability and resolution of the conversion process will be about one-half of one digital step. This ambiguous half-step, combined with the toggle action which occurs between steps, usually means that the output reading of an analog-to-digital converter is accurate to no better than plus or minus one digit in the number of digits read out. For maximum accuracy it is then desirable to digitize the analog input signals as near to the system full scale as is possible. If noise is present in the analog input signal, the problem of conversion may be extremely difficult. Some converters are completely useless in the presence of cyclic noise because of their inability to stabilize on any single reading. Others will read out the sum of the signal and the instantaneous noise, while still others will read the peak or the average noise plus the signal. In any case, for maximum accuracy, frequency components in the analog input signal which exceed the maximum frequency that can be digitized must be damped to the point where they do not interfere with the digital conversion.

EXAMPLES

At the present time developmental effort in the field of analog-to-digital conversion is quite intense and fluid. It is probable over one hundred different devices have been demonstrated in breadboard form in the last three years, although few of these have actually reached the stage where they can be purchased commercially. This survey covers about fifty of these devices in particular, and it is believed that the ideas expressed here would also describe the majority of those not included. Seventeen techniques have been chosen as illustrations. Although these are grouped together as nine different figures for convenience mostly, it is felt this is not necessarily the best classification. Perhaps devices competing for the same application would have been a more interesting grouping, but the problems of explanation would have been much more complex. The reason for this is that many specific analog-to-digital converters are, or could be, combined with an analog-to-analog converter in such a way that all techniques would be essentially competitive.

Two direct-counting techniques are shown in Fig. 2. For this application the converters are arranged to generate some kind of repetitive event which can be counted. The revolution angle of a shaft can be broken into finite segments by slotting a disk attached to the shaft. With reasonable machining care one revolution can be digitized to an accuracy of plus or minus one count in several thousand. The slots can be sensed magnetically or photoelectrically, and counted in an electronic counter. Special arrangements of the sensing device can be used to detect the phase of the count, and the counter can be made to count up or down depending on the direction of the rotation. The instantaneous count in the counter is then the digital measurement of the shaft position in relation to its position at a zero count. In much the same way, the relative motion of the two conductor grids generates nulls and peaks in the detector circuit which can be counted. This technique tends to average the dimensional location errors and may be potentially the more accurate of the two. The output signal from both of these converters is a "time" code.

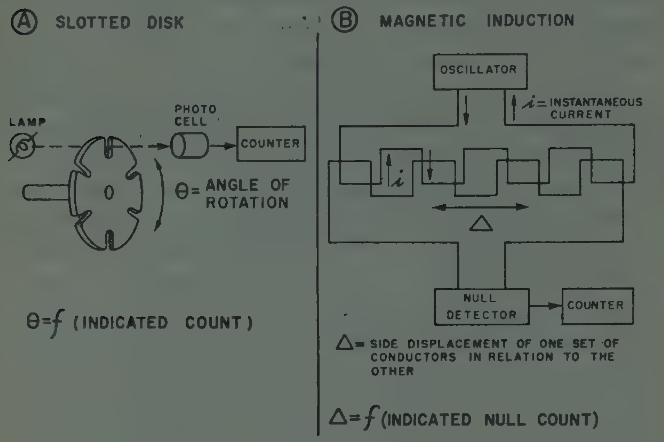

Ⓐ SLOTTED DISK
LAMP
PHOTO CELL
COUNTER
0
θ= ANGLE OF ROTATION
θ=f (INDICATED COUNT)
Ⓑ MAGNETIC INDUCTION
OSCILLATOR
i= INSTANTANEOUS CURRENT
i
Δ
NULL DETECTOR
COUNTER
Δ= SIDE DISPLACEMENT OF ONE SET OF CONDUCTORS IN RELATION TO THE OTHER
Δ=f (INDICATED NULL COUNT)

Fig. 2—Direct-counting techniques.

Fig. 3 describes two incremental-step techniques. The step-matrix voltage indicator is essentially the electrical equivalent of the multi-contact displacement indicator. In this device a crystal is biased at each of the desired voltage increments. When the input voltage is equal to one of the bias voltages, the current through that circuit will suddenly change, and can be used to actuate an indicator. It is probable this technique can have the highest possible speed of response, as the speed limitation is primarily a function of circuit capacitance. Each of these converters produces a "space" code.

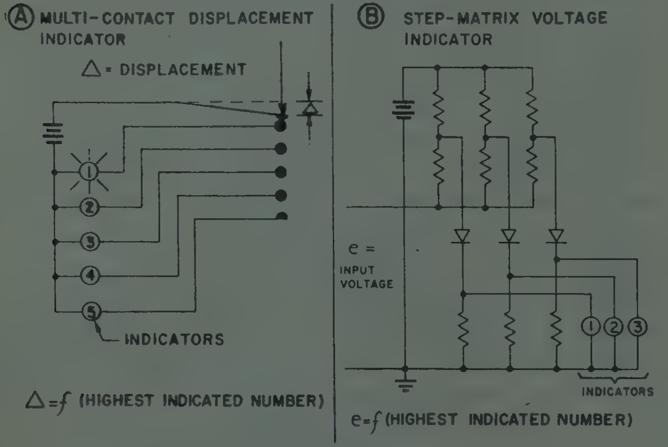

Ⓐ MULTI-CONTACT DISPLACEMENT INDICATOR
Δ = DISPLACEMENT
②
③
④
⑤
INDICATORS
Δ=f (HIGHEST INDICATED NUMBER)
Ⓑ STEP-MATRIX VOLTAGE INDICATOR
e = INPUT VOLTAGE
① ② ③
INDICATORS
e=f (HIGHEST INDICATED NUMBER)

Fig. 3—Incremental step techniques.

Fig. 4 demonstrates some of the things that can be done with a commutator and a brush. The phased-binary presentation of Fig. 1(b) is producible by bussing every third commutator bar to actuate three indicators in a "space-time" code. It is not even necessary that the brush span the distance between two bars, as the absence of a signal can carry significance in this case. An ambiguous "space" code can be prevented if the commutator bars are spaced close together and the brush is equal to one-half the width of one bar. In this case a relay matrix can unscramble the code into decimal significance, as is shown. One other commutator-brush converter has an exceedingly clever method of actually toggling the brush itself so that it jumps from bar to bar, and never stops on or between two bars.

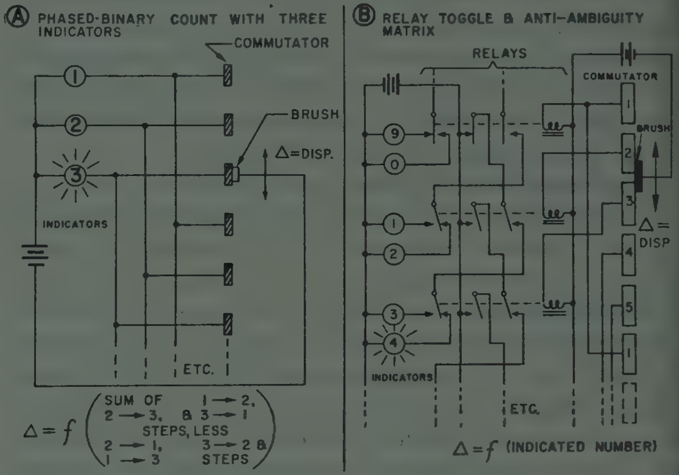

Ⓐ PHASED-BINARY COUNT WITH THREE INDICATORS
COMMUTATOR
①
②
③
BRUSH
Δ=DISP.
INDICATORS
ETC.
Δ = f (SUM OF 1 → 2, 2 → 3, & 3 → 1 STEPS, LESS 2 → 1, 1 → 3 3 → 2 & STEPS)
Ⓑ RELAY TOGGLE & ANTI-AMBIGUITY MATRIX
RELAYS
COMMUTATOR
BRUSH
⑨
⓪
①
②
③
④
1
2
3
4
5
1
Δ= DISP
INDICATORS
ETC.
Δ=f (INDICATED NUMBER)

Fig. 4—Commutator and brush techniques.

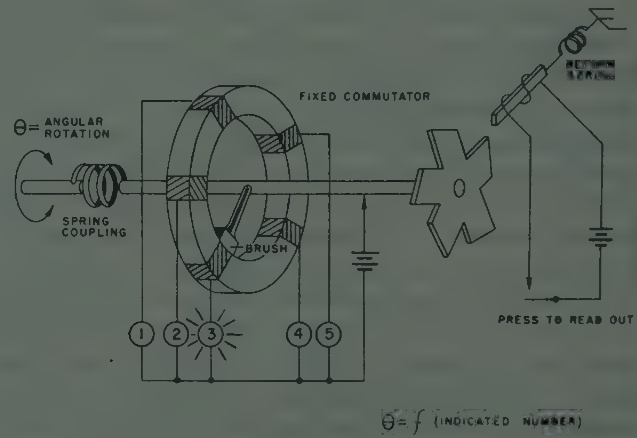

θ= ANGULAR ROTATION
SPRING COUPLING
FIXED COMMUTATOR
BRUSH
RETURN SPRING
0
① ② ③ ④ ⑤
PRESS TO READ OUT
θ=f (INDICATED NUMBER)

Fig. 5—Forced nonambiguous techniques: star wheel.

The principle illustrated by Fig. 5 is a relatively simple one, but it requires a rather complex drawing. Only one example is shown. In this case the analog input information is in the form of a shaft angle. A star-wheel-and-commutator combination is elastically coupled to the shaft, so that its position duplicates the shaft angle until readout is desired. Just before readout a solenoid-operated plunger forces the star wheel to align the brush directly onto the nearest commutator bar, which then provides the desired digital signal.

If the oscillations of a frequency-modulated signal are counted for a fixed period of time, the count can be made to describe the modulating function. Fig. 6 shows two well-known methods for changing the frequency of an oscillating system. The vibrations of a wire under tension can be sustained at the natural frequency, or some harmonic, by magnetic-electronic means, and the frequency can be varied by changing the tension. In much the same way changes of resistance, capacitance, inductance, or voltage can be made to change an electronic oscillator's frequency. These methods are generally nonlinear, and require some technique of zero suppression, but can be made to give useful results.

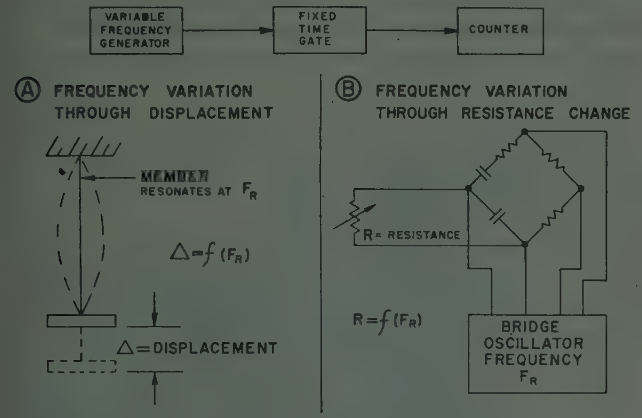

VARIABLE FREQUENCY GENERATOR
FIXED TIME GATE
COUNTER
Ⓐ FREQUENCY VARIATION THROUGH DISPLACEMENT
MEMBER RESONATES AT F_R
$\Delta=f(F_R)$
Δ=DISPLACEMENT
Ⓑ FREQUENCY VARIATION THROUGH RESISTANCE CHANGE
R= RESISTANCE
$R=f(F_R)$
BRIDGE OSCILLATOR FREQUENCY F_R

Fig. 6—Fixed-interval techniques.

Fig. 7 describes the converse of Fig. 6. Here chronometric pulses are generated, and gated into a counter by one event, and the counter is stopped by another event. The resulting count in the counter is a measurement of the elapsed time between the two events. A linear sawtooth voltage, coinciding with a zero signal and an input voltage, can be made to digitize the input voltage. The phase relationship between two alternating signals can be measured similarly. This is an old approach and has been used in ballistic studies and timing races.

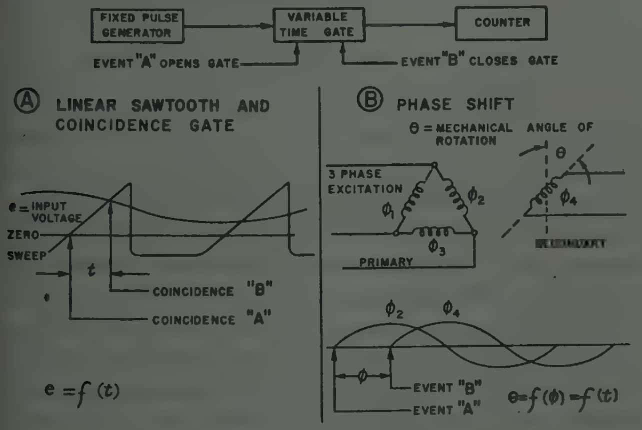

FIXED PULSE GENERATOR
VARIABLE TIME GATE
COUNTER
EVENT "A" OPENS GATE
EVENT "B" CLOSES GATE
Ⓐ LINEAR SAWTOOTH AND COINCIDENCE GATE
e = INPUT VOLTAGE
ZERO
SWEEP
t
COINCIDENCE "B"
COINCIDENCE "A"
$e=f(t)$
Ⓑ PHASE SHIFT
θ = MECHANICAL ANGLE OF ROTATION
3 PHASE EXCITATION
ϕ_1
ϕ_2
ϕ_3
ϕ_4
θ
PRIMARY
SECONDARY
ϕ
EVENT "B"
EVENT "A"
$\theta=f(\phi)=f(t)$

Fig. 7—Chronometric techniques.

Fig. 8 shows two ways in which a raster can be used to provide the digital signals. Example "A" makes use of holes in a disk to control the passage of light from a source to a group of photocells. The holes and photocells are then mutually coded to give a "space" binary code. This device actually would not work well as shown because the particular code used has a tendency to become ambiguous if there is any instability in the system. Other codes have been used that will accurately divide one shaft revolution into several thousand parts. The same raster is capable of producing a "time" code if the so-called "flying spot" is used to develop a time axis. Example "B" makes use of the beam in a cathode-ray tube driven by a saw tooth voltage on the horizontal axis. The vertical voltage is then digitized by the interruptions of the beam caused by that part of the raster over which the flying spot passes. A galvanometer driven with a saw-tooth current and a single photocell could accomplish the same effect with the coded disk of Example "A."

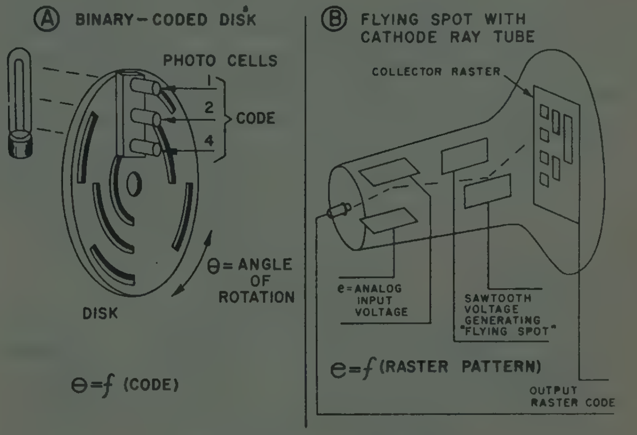

Ⓐ BINARY-CODED DISK
PHOTO CELLS
1
2
4
CODE
θ= ANGLE OF ROTATION
DISK
$\theta=f$ (CODE)
Ⓑ FLYING SPOT WITH CATHODE RAY TUBE
COLLECTOR RASTER
e=ANALOG INPUT VOLTAGE
SAWTOOTH VOLTAGE GENERATING "FLYING SPOT"
$e=f$ (RASTER PATTERN)
OUTPUT RASTER CODE

Fig. 8—Raster techniques.

Two methods using continuously rotating drums are pictured in Fig. 9. In both of these cases there are two information areas on the drum that are mutually synchronized by their physical locations. Example "A" requires a hollow drum whose cylindrical surface is perforated by two types of symbols. Inside the drum, in back of some small slits, is a photocell, while in back of the appropriate Arabic numbers is a flash tube. The photocell and flash tube do not rotate with the drum. If light ever impinges on the photocell the flash tube will be illuminated. The slits are then arranged around the circumference of the drum in such a way as to synchronize with the proper symbol, and along the axis of the drum to break up a linear distance into incremental steps. If the spot of light from a galvanometer's mirror is then reflected onto the area of the drum which includes the slits, it will fall on only one of the slits per drum revolution and only one number will be illuminated, indicating the galvanometer's deflection. Example "B" makes use of a magnetic drum on the periphery of which are recorded two pulse tracks. The first of these has a duplicity of pulses which break up the circumference of the drum into the desired number of digits. The second pulse track has only one pulse recorded on it. There is a fixed head reading each of the two tracks and a movable head reading the single-pulse track. An electronic counter can then be used to count the number of pulses on the drum between the fixed head and the movable head in such a way that the angular distance between the two heads is indicated.

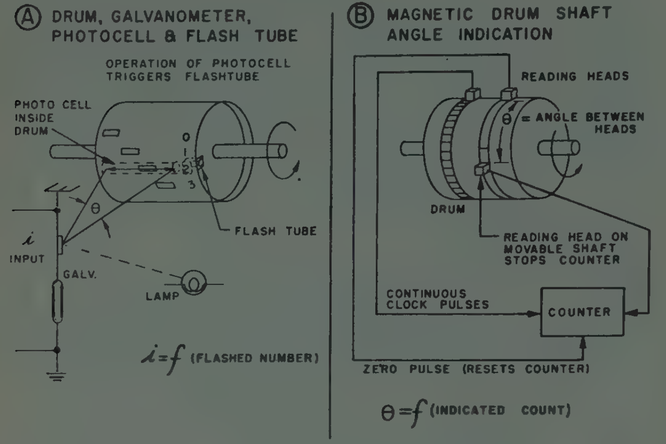

Ⓐ DRUM, GALVANOMETER, PHOTOCELL & FLASH TUBE
OPERATION OF PHOTOCELL TRIGGERS FLASHTUBE
PHOTO CELL INSIDE DRUM
0
1
2
3
θ
FLASH TUBE
i
INPUT
GALV.
LAMP
i=f (FLASHED NUMBER)
Ⓑ MAGNETIC DRUM SHAFT ANGLE INDICATION
READING HEADS
θ = ANGLE BETWEEN HEADS
DRUM
READING HEAD ON MOVABLE SHAFT STOPS COUNTER
CONTINUOUS CLOCK PULSES
COUNTER
ZERO PULSE (RESETS COUNTER)
θ=f (INDICATED COUNT)

Fig. 9—Synchronous drum techniques.

Fig. 10 includes two self-balancing or null-detecting techniques. The first of these is nothing more or less than a standard, self-balancing potentiometer with the slide wire replaced by a Thompson-Varley decade. In this particular example individual plus-minus stepping switches operate on each decimal-digit to achieve the maximum speed of balance. The second example might be considered to be an electronic equivalent of a self-balancing potentiometer. A phase-sensitive detector, working from the difference between the input voltage and the voltage generated by an adder circuit controls the flow of pulses to a toggle counter, which in turn controls the voltage of the adder circuit. The circuitry of such a device becomes rather complex, consequently symbols are used here, but it should be understood that all of the indicated functions can be done electronically for maximum speed of response. The Thompson-Varley output signal consists of coded-contact-closures from the stepping switches, while the electronic counter circuit produces a bus-code from one side of each toggle.

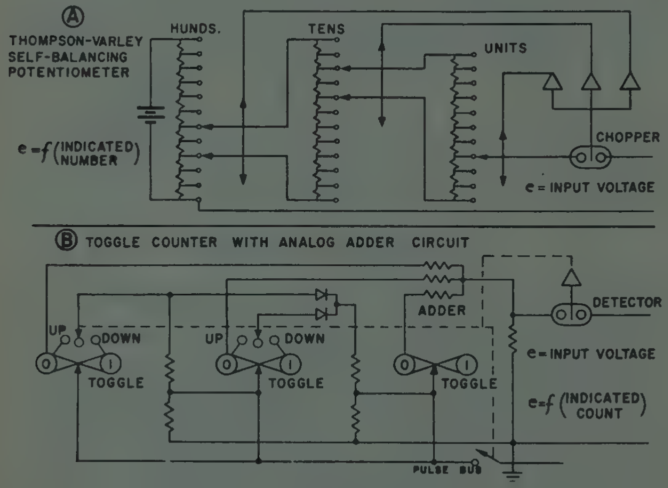

Ⓐ THOMPSON-VARLEY SELF-BALANCING POTENTIOMETER
HUNDS.
TENS
UNITS
CHOPPER
e=f (INDICATED NUMBER)
e = INPUT VOLTAGE
Ⓑ TOGGLE COUNTER WITH ANALOG ADDER CIRCUIT
ADDER
DETECTOR
UP
DOWN
TOGGLE
0
1
e = INPUT VOLTAGE
e=f (INDICATED COUNT)
PULSE BUS

Fig. 10—Null detector techniques.

All the analog-to-digital converters described have been reduced to bare, essential features for the purpose of discussion. Most of the successful instruments are a considerable elaboration on one of the basic ideas.

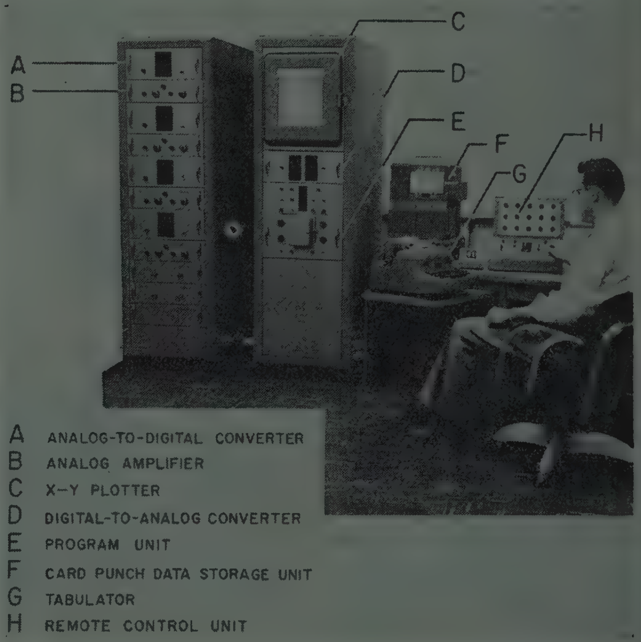

A
B
C
D
E
F
G
H
A ANALOG-TO-DIGITAL CONVERTER
B ANALOG AMPLIFIER
C X-Y PLOTTER
D DIGITAL-TO-ANALOG CONVERTER
E PROGRAM UNIT
F CARD PUNCH DATA STORAGE UNIT
G TABULATOR
H REMOTE CONTROL UNIT

Fig. 11—Analog-to-digital conversion.

SYSTEMS

Analog-to-digital converters are useful devices in themselves, but they demonstrate their greatest worth when they are incorporated into a system. Fig. 11 is a typical digital data-processing system. For the sake of identification, this might be called a multi-channel "quasi-static" system, where quasi-static means that the input signals change only at the discretion of the operator. For example, in the collection of data from a wind tunnel, the operator initiates the data-handling cycle when he is satisfied that the model is adjusted properly and conditions in the tunnel are stabilized to the point where data of some significance can be taken. After the data have been collected, the conditions in the tunnel are changed and the cycle repeated. This particular system is chosen as an example because it contains all of the essential features of a "complete" system.

The system illustrated consists of four channels of analog-to-digital conversion equipment, a remote control unit, a plotting unit, a tabulating unit, a storage unit, and a program unit. After this system is set up, adjusted, and calibrated, an operator at the remote control point can examine the input channels, decide on their reasonableness, freeze these data, and initiate the readout cycle. Data collected by the system are then automatically tabulated, plotted, and punched into cards.

For the sake of this illustration, it might be assumed that this system is operating from the output signals of four strain-gage bridges attached to a model in a wind tunnel. The analog voltages generated by the strain gages are amplified and converted to their equivalent digits by the action of individual, digital self-balancing potentiometers. The coded-contact-closure signals from these potentiometers indicate the balance points accurate to three decimal places, the polarity of the balance points, the attenuator settings, and whether or not there is an actual balanced condition in each channel. The calibration of this system will include simple analog computations in the input amplifiers, which change the significance of the digits to some desired linear function. Zero suppression (addition or subtraction) and scale factor adjustment (multiplication or division) controls are available on the front panel of each amplifier.

The remote control unit includes fifteen rotary switches which allow the introduction of arbitrary fixed constants into the tabulator and card format. These constants can be used to indicate dates, model configuration, test numbers, and other information that does not change as a result of the test. The program unit controls the flow of information from the converters and the fixed constants on the control board into the tabulator, card punch, and from the digital-to-analog converter in the $X-Y$ plotter. A plug board is provided to allow flexibility in the program and information format. A "run" number, generated each time the program completes a cycle, is recorded along with the other digits. A possible tabulated format might be as follows:

Test	Date	Run	X	Y	Z	No. 1		No. 2		No. 3		No. 4	
21	1-21-52	01	0 10	0 15	1 00	1	−251	2	354	1	791	4	−697
21	1-21-52	02	0 10	0 15	2 00	1	−264	2	300	1	988	4	−501
21	1-21-52	03	0 10	0 15	3 00	1	−281	2	265	2	525	4	−275

The same information would also be punched into the cards, with one card for each tabulated row. These cards can then be used to control a computer for complete data reduction.

The digital-to-analog converter can receive two, three-digit numbers, and pass equivalent analog signals to the plotter unit for control of the X and Y plotting axes. These digits can be programmed automatically, introduced by hand at the remote control point, or read from the punched cards, as the circumstances dictate.

If the operator has control of only the start of the test and must take data at fixed intervals of time thereafter, the required system might be called a "dynamic" data-processing system. An application example would be that required for processing data during a rocket's flight. Here, high-speed conversion and control equipment is required, with perhaps a recording oscillograph replacing the electro-mechanical plotter and a magnetic-tape recorder replacing the card-punch unit. Tabulation and computation could be done at the end of the test by playing back the magnetic tape at a reduced speed. "Dynamic" data-processing systems usually generate a great deal of unwanted data in order to assure the collection of the desired data, so that some method must be available for separating out the useful information at the end of the test; otherwise, the system philosophy is not much different from that of the "quasi-static" example.

Conclusion

It has been shown that an analog-to-digital converter can be an important part of an automatic data-reduction system. Of course, such instruments are not the complete answer to all of the data-reduction problems as they furnish but one step in the process. Plotters, tabulators, storage devices, matching equipment, and computers must all be considered as a part of such a system and the characteristics of the analog-to-digital converter must be compatible with their characteristics as well as those of the analog signal. At present, an analog-to-digital converter may be considered somewhat of a novelty, but in the future their use will become commonplace. Applications seen for the near future include wind tunnels, engine and rocket test stands, telemetry, static structural tests, industrial process control, computer inputs, and so forth. Even at this stage of the technique, data processing is being greatly accelerated.

Bibliography

Barney, "Binary quantizer," *Elec. Eng.;* Nov., 1949.
Best, N. R., "Matrix telemetering system," *Electronics;* Aug., 1950.
Bowersox, R. B., and Hylkema, C. G., "High-Speed Recordiug Potentiometer," Jet Propulsion Laboratory Memorandum No. 20–69, California Institute of Technology, Pasadena, Calif.; Jan. 16, 1953.
Burke, H. E., "Some Techniques of Analog-to-Digital Conversion", Translations of IRE 7th Section Professional Group on Electronic Computers, April, 1952.
Davis, F. H., Navord Report 1219, Naval Ordnance Test Station, Inyokern, Calif.; Nov. 16, 1949.
Donath, E., "Automatic Data Reduction," present at the 27th meeting of the Bumblebee Guidance Panel, Appl. Sci. Corp. of Princeton, Princeton, N. J.
Goldberg, E. A., "Step multiplier." *Electronics;* Aug., 1951.
Harrington, J. V., Spencer, G. R., and Wulfsberg, K. N., "A Five-Digit Parallel Coder Tube," Massachusetts Institute of Technology, Cambridge, Mass.
Klein, D. A. L., and Gow, K. P., "A Dial-Reading Translator for Digital Machine Inputs," Southern California Cooperative Wind Tunnel, Pasadena, Calif. April, 1952.
Kuder, M. L., "Anodige, and Electronic Analog-to-Digital Converter," National Bureau of Standards Report No., 1117, Washington, D. C.
Lippel, B., "A High Precision Analog-to-Digital Converter," Signal Corps Eng. Labs., Fort Monmouth, N. J.
Sears, R. W., "Electron beam deflecting tube for pulse code modulation," *Bell Sys. Tech. Jour.;* Jan., 1948.

Sink and Slocomb, "The SADIC, A Precision Analog-Digital Converter," Consolidated Engineering Corp. Presented at the IRE Data Handling Symposium, Long Beach, Calif.; Aug., 1951.

Smith, B. D., "Telemetering by Pulse Code Modulation," Melpar, Inc., Alexandria, Va.

Company Brochures

Arthur D. Little, Inc.
Atomic Instruments Company
Beckman Instruments, Inc.
Benson-Lehner Corporation
Berkeley Scientific Company
Clary Multiplier Corporation
Consolidated Engineering Corporation
Electronic Engineering Company of California
Engineering Research Associates; Inc.
Institute of Inventive Research
Melpar, Inc.
Metrotype Corporation
Potter Instrument Company
Streeter-Amet Company
Taller and Cooper, Inc.
Telecomputing Corporation
Westinghouse Electric Corporation
Wright Engineering

Unpublished Projects

Benson-Lehner Corporation
Consolidated Engineering Corporation
Cornel Wind Tunnel Instrumentation Group
Electro Circuits Company
Massachusetts Institute of Technology by Sisson and Susskind
National Advisory Committee of Aeronautics, Lewis Laboratory
National Bureau of Standards Survey, by G. G. Bower
Naval Research Laboratory by A. M. Rothrock
Office of Naval Research Survey by N. M. Blachman
Tally Register Company
Telecomputing Corporation
Wallind-Pierce Corporation
Wright Field Wind Tunnel Instrumentation Group

An Analog-to-Digital Converter for Serial Computing Machines*

H. J. GRAY, JR., P. V. LEVONIAN, AND M. RUBINOFF†, ASSOCIATES, IRE

Summary—**An analog-to-digital converter is described whose output can be read synchronously into a high-speed digital computer. The converter uses new types of cyclic-to-binary translators capable of converting a cyclic number into its binary form serially with least significant digit first. The underlying theorems are proved.**

INTRODUCTION

THERE HAVE ARISEN numerous instances where the magnitude of an analog quantity is required in digital form in a serial computing machine. The devices described in this paper accomplish the conversion of the analog number from its voltage-analog representation to its binary-digital representation as a time sequence with least significant digit first. Moreover, if desired, the conversion is sufficiently fast to allow N numbers to be converted in $(N+1)$ number-times (minor cycles), even for the fastest existing serial computing machines.

The process of conversion employed occurs in two steps, as shown in Fig. 1. The number is first converted from its voltage representation to "reflected binary" or "cyclic" code with least significant digit first. Next, the resultant cyclic number is transformed to its binary representation. It is important to note that this cyclic-to-binary transformation is carried out least significant digit first. Methods used to date for this type of transformation worked only with the most significant digit first, hence a reversing process was necessary before the number could be read into a serial computing machine.

The details of the system are described below.

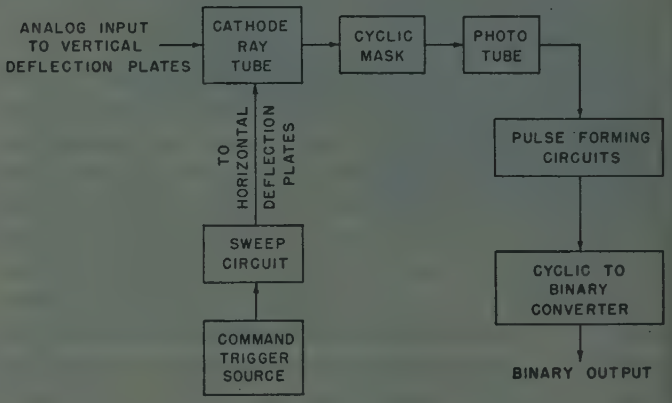


Fig. 1—Block diagram of analog to digital converter.

THEORETICAL CONSIDERATIONS

The cyclic code is derived from the binary notation by a single column shift followed by a logical addition, i.e., addition without carry. Thus the binary number:[1]

$$A_2 = \sum_{j=0}^{n-1} a_j 2^j = a_{n-1}a_{n-2} \cdots a_1 a_o$$

becomes the cyclic number:

$$A_c = \alpha_{n-1}\alpha_{n-2} \cdots \alpha_1 \alpha_o;$$

where

$$\alpha_{n-1} = a_{n-1} \tag{1}$$

and

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, May 6, 1953.

† Moore School of Electrical Engineering, University of Pennsylvania.

[1] For any number A the binary representation will be written as A_2 and the cyclic representation as A_c. The arabic letters a_j and b_j will be used to designate digits of the binary numbers, and the Greek letters α_j and β_j will be used to designate digits of the cyclic numbers.

$\alpha_j \equiv (a_j + a_{j+1}) \pmod 2, \quad j = 0, 1 \cdots n-2,$

where mod 2 addition of two binary *digits* is of course addition without carry.

Note that $\alpha_j = 0, 1$ according as $a_j = a_{j+1}$ or $a_j \neq a_{j+1}$, respectively. The process is illustrated for the number "thirteen":

$$\begin{array}{lrcccc} & A_2 = & 1 & 1 & 0 & 1 \\ \text{shifted} & A_2 = & & 1 & 1 & 0 \ (1) \\ \hline & A_c = & 1 & 0 & 1 & 1. \end{array}$$

Theorem I: The cyclic representations of any pair of successive numbers, A and $A+1$ $(=B)$, differ in only one column.

Proof: Let $A_2 = a_{n-1}a_{n-2} \cdots a_1a_o$, $B_2 = b_{n-1}b_{n-2} \cdots b_1b_o$.

(1) Suppose $a_o = 0$. Then $b_o = 1$ and $a_j = b_j$ for $j \neq 0$. Hence $\beta_o \equiv b_o + b_1 \equiv 1 + a_1$; $\alpha_o \equiv a_o + a_1 = a_1$; $\beta_j \equiv b_j + b_{j+1} = a_j + a_{j+1} \equiv \alpha_j$; $j \neq 0$.

$\therefore$ In this case, A_c differs from B_c only in column $j = 0$.

(2) Let $a_o = 1$, the only other possible case. Then,

$$b_o = 0, \qquad b_1 \equiv 1 + a_1.$$

Consider column $j = 0$:

$$\beta_o = b_o + b_1 = 1 + a_1; \qquad \alpha_o = a_o + a_1 = 1 + a_1.$$

Hence $\beta_o = \alpha_o$.

Consider next column $j = 1$. We note in this case that $b_1 = 1 + a_1$. If $a_1 = 0$ the argument of part (1) applies, $\beta_1 \neq \alpha_1$, $\beta_j = \alpha_j$ for $j \neq 1$ and the theorem holds; if $a_1 = 1$, then $b_2 \equiv 1 + a_2$, the argument of part (2) holds, $\beta_1 = \alpha_1$, but column $j = 2$ must be inspected.

The process may be continued until (a) it terminates at column $k \neq (n-1)$ with $\beta_k \neq \alpha_k$, $\beta_j = \alpha_j$ for $j \neq k$, in which case the theorem holds, or (b) $\beta_j = \alpha_j$ for $j < (n-1)$ and $b_{n-1} \equiv a_{n-1} + 1$. In the latter case, since there is no column n, $\beta_{n-1} \neq \alpha_{n-1}$ whether $a_{n-1} = 0$ or 1. This completes the proof of the theorem.

Theorem II: The parity of A_c is even or odd according as $a_o = 0$ or 1.

Proof: The parity of A_c is by definition the sum of the digits α_j of A_c, to modulus 2. But from equation (1) it is seen that

$$\begin{aligned} &\alpha_{n-1} + \alpha_{n-2} + \cdots + \alpha_1 + \alpha_o \\ &\equiv a_{n-1} + (a_{n-1} + a_{n-2}) + \cdots + (a_2 + a_1) + (a_1 + a_o) \\ &\equiv 2(a_{n-1} + a_{n-2} + \cdots + a_2 + a_1) + a_o \\ &\equiv a_o \pmod 2, \quad \text{since } 2x \equiv 0 \pmod 2 \text{ for all } x. \end{aligned}$$

$$\therefore \quad \text{Parity of } A_c = a_o.$$

Theorem III: If $x + y \equiv z \pmod 2$, then $x + z \equiv y \pmod 2$.

Proof:

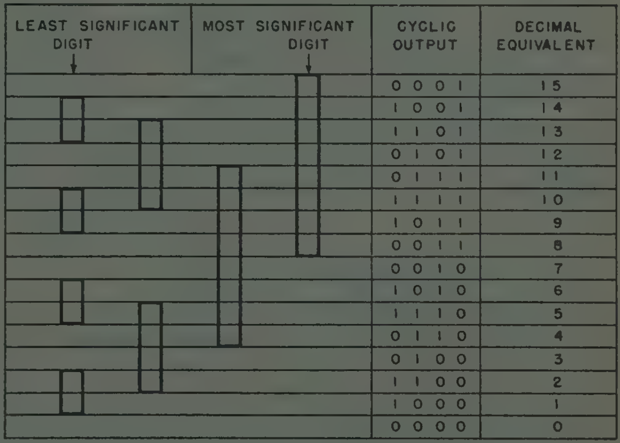
$$\begin{aligned} x + z &\equiv x + (x + y) \\ &\equiv 2x + y \\ &\equiv y \pmod 2. \end{aligned}$$

These theorems will be used in the discussion below.

Analog-to-Cyclic Conversion

The device for generating the cyclic representation from the voltage analog is similar to devices described elsewhere.[2–4] Referring to Fig. 1, the basic principles of the system are as follows.

The analog (voltage) input is placed on the vertical deflection plates of a cathode-ray tube. Through a command trigger pulse, the electron beam is made to sweep horizontally across the face of the tube with constant velocity. A mask, quantized into distinct vertical levels, is placed in front of the tube. It is constructed in such a way that at the vertical level corresponding to the number A, holes have been provided which represent A in cyclic notation. The mask for a four-digit output is shown in Fig. 2; the slots have been placed in such a manner that at a given level the digits of the number appear in increasing order of significance from left to right. This is the reverse of the order in which the numbers are normally written. They are placed this way so as to obtain the least significant digit of the cyclic output first with the electron beam sweeping from left to right. The numbers corresponding to the sixteen vertical levels are indicated in both decimal and cyclic form.



CYCLIC OUTPUT	DECIMAL EQUIVALENT
0 0 0 1	15
1 0 0 1	14
1 1 0 1	13
0 1 0 1	12
0 1 1 1	11
1 1 1 1	10
1 0 1 1	9
0 0 1 1	8
0 0 1 0	7
1 0 1 0	6
1 1 1 0	5
0 1 1 0	4
0 1 0 0	3
1 1 0 0	2
1 0 0 0	1
0 0 0 0	0

Fig. 2—Cyclic mask.

As the beam sweeps across the face of the tube from left to right, the light which passes through the holes in the mask is picked up by the photo-tube and converted by additional circuits into serial voltage pulses which represent, least significant digit first, the cyclic equivalent of the analog voltage input.

The advantage of using a cyclic mask is demonstrated by *Theorem I.*[5] If the electron beam sweeps between the

---

[2] L. A. Meacham and E. Peterson, "An experimental multichannel pulse code modulation system of toll quality," *Bell Sys. Tech. Jour.*, vol. 27, p. 30; January, 1948.

[3] R. W. Sears, "Electron beam deflection tube for pulse code modulation," *Bell Sys. Tech. Jour.*, vol. 27, p. 44; January, 1948.

[4] Raymond P. Mork, "Coders," (Symposium on digital computers in control systems), *IRE Convention:* March 5, 1952.

[5] W. M. Goodall, "Television by pulse code modulation," *Bell Sys. Tech. Jour.*, vol. 30, p. 38; January, 1951.

levels representing two successive numbers there is an ambiguity in one column only and either one of these two successive numbers will be the resultant output. Using a binary mask, however, it is possible for an ambiguity to occur in several or all columns. Consider for example the beam lying between the levels representing binary seven (0111) and binary eight (1000). Using a binary mask, any number between zero and fifteen, inclusive, might be obtained.

Cyclic to Binary Transformation

From *Theorem II* it follows that, in converting from cyclic code back to binary notation with least significant digit first, the first digit a_o may be obtained by counting the number of "1"s mod (2) in A_c, using a binary counter initially reset to zero. The final state of the counter determines a_o. Moreover, since $a_o+a_1\equiv\alpha_o$ (mod 2), it follows from *Theorem III* that $a_o+\alpha_o\equiv a_1$ (mod 2), and a_1 may be obtained by adding α_o to a_o in the binary counter. Similarly, a_{j+1} for all j can be found by addition in the counter since $a_{j+1}\equiv a_j+\alpha_j$ (mod 2). Hence, the entire binary representation, A_2, may be obtained by reading the cyclic number into the binary counter twice.

The following methods described below are based on this result.

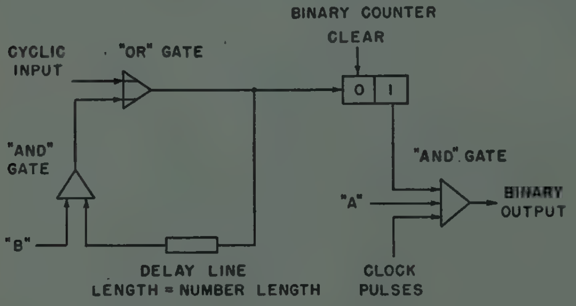

BINARY COUNTER
CLEAR
CYCLIC INPUT
"OR" GATE
0
1
"AND" GATE
"AND" GATE
"A"
BINARY OUTPUT
"B"
DELAY LINE LENGTH = NUMBER LENGTH
CLOCK PULSES

Fig. 3—Cyclic to binary converter; method (1).

(1) (See Fig. 3.) The binary counter is initially cleared to the "0" stage. The output is obtained by gating clock pulses with the "1" stage of the counter. The cyclic input is read to the counter twice; once to determine the least significant digit of the binary output and a second time to produce the entire output. The second reading is obtained by circulating the cyclic number through a delay line back to the input of the counter. The "B" input prevents the cyclic number from circulating more than once, and the "A" input gates the correct portion of the output.

(2) This is based on the observation that there are only two possibilities for a_o: zero or one. Application of *Theorem III* in finding A for the two cases leads to the result that the two resulting binary representations are 1's complements of each other. For example for A_c $=1011$ if it is correctly assumed that $a_o=1$ then the correct binary counterpart 1101 is obtained. However, if it is incorrectly assumed that $a_o=0$ then the incorrect binary number 0010 is obtained.

Referring to Fig. 4, it is seen that when the cyclic number is read to counter both of these possibilities are generated by gating clock pulses with the opposing stages of the counter. These two binary outputs are delayed one number length until the cyclic input has been completely read to the counter. The correct output is then selected by the stage of the counter which is positive, i.e. by the parity of the cyclic input. It should be noted that the initial setting of the counter is immaterial as the correct output is obtained in both cases. The "A" input is added to gate the correct portion of the output.

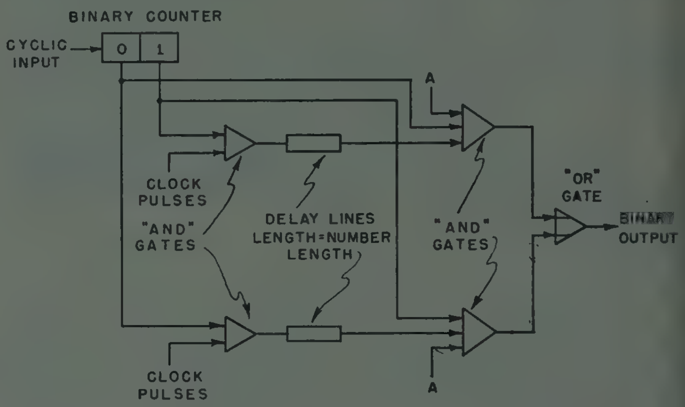

BINARY COUNTER
CYCLIC INPUT
0
1
A
CLOCK PULSES
"AND" GATES
DELAY LINES LENGTH=NUMBER LENGTH
"AND" GATES
"OR" GATE
BINARY OUTPUT
CLOCK PULSES
A

Fig. 4—Cyclic to binary converter; method (2).

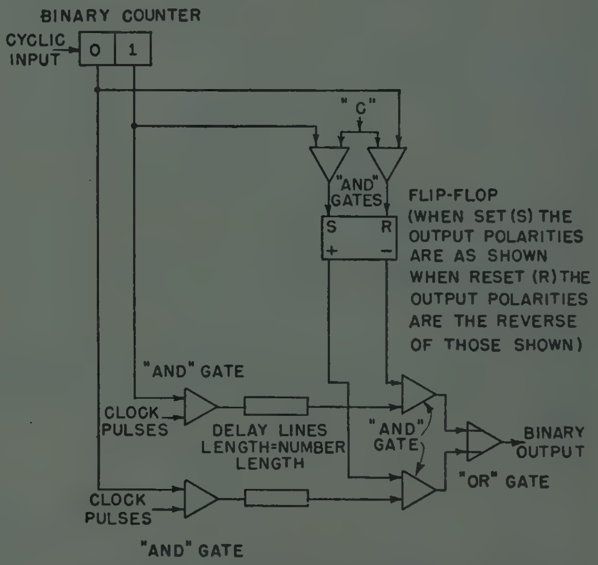

BINARY COUNTER
CYCLIC INPUT
0
1
"C"
"AND" GATES
S
R
+
−
FLIP-FLOP (WHEN SET (S) THE OUTPUT POLARITIES ARE AS SHOWN WHEN RESET (R) THE OUTPUT POLARITIES ARE THE REVERSE OF THOSE SHOWN)
"AND" GATE
CLOCK PULSES
DELAY LINES LENGTH=NUMBER LENGTH
"AND" GATE
BINARY OUTPUT
"OR" GATE
CLOCK PULSES
"AND" GATE

Fig. 5—Cyclic to binary converter; method (3).

(3) (See Fig. 5.) This is a modification of method 2 which allows several cyclic numbers to be converted in sequence. The state of the counter after the first cyclic number is read in is remembered by the flip-flop. This releases the counter from the duty of selecting one of the two possible outputs, and it can thus be used immediately by the second cyclic number to be converted. "C"

is the trigger input to the flip-flop. It occurs immediately after each cyclic number is read completely to the counter.

With this system N cyclic numbers can be converted in $N+1$ number times.

Experimental Results

A four-digit cyclic mask was prepared by hand. The size was such that a 5 inch cathode-ray tube could accommodate 256 lines (an 8 digit mask), i.e., the line-separation was 0.5 mm. The horizontal separation was approximately $\frac{1}{2}$ inch overall. Using experimental equipment, successful resolution of vertical lines was obtained, and the entire system operated correctly at 1 megacycle pulse rate. Pulse resolution remained adequate up to at least four megacycles.

Acknowledgement

This work was done as part of a project sponsored by the Special Devices Center, ONR.

Effectiveness of Two-Step Smoothing in Digital Control Computers*

ROBERT E. SPERO†

***Summary*—An analysis is made of the effect, in smoothing observational data with a digital computer, of using two smoothing steps, the first having a high data handling rate and a short smoothing time, the second a low data handling rate and a long smoothing time. The analysis shows that for the most commonly used types of smoothing, the effect of the two smoothing operations in series is essentially equivalent to that of a single operation combining the most desirable features of each of the two, i.e., the high data handling rate of the first operation and the long smoothing time of the second. This fact is important in certain control applications where the combination of both these features in one smoother is not possible.**

I. Introduction

A DIGITAL computer which is an element in a control system will often have as one of its functions the smoothing of observational data containing random noise. The effectiveness of the smoothing will depend directly on the number of observations over which the smoothing takes place, i.e., on the product of the smoothing time, T, and the data handling rate, n, in observations per second. Thus, both a high data rate and a long smoothing time are desirable.

Sometimes, however, the incoming information is in such a form that while it can be sampled at a high rate, its smoothing time must be kept low to avoid intolerable errors due to rate or acceleration lags. If, to avoid these lags, the data are converted before smoothing to a form in which long smoothing times can be used without introducing appreciable errors, the additional computing steps required before smoothing may make it impossible to handle the data at a high rate. Thus with a single smoother either n or T can be large, but not both, and the effectiveness of the smoothing is severely limited.

A possible solution to this dilemma is presented here. It consists of using two smoothers in cascade. The first smoother accepts the data at a high rate, n_1, and smoothes over a short time, T_1. The data are then converted to a form permitting a long smoothing time, T_2, and are smoothed over this time in a unit handling only a small number, n_2, of observations per second. It is shown in this paper that for the most commonly used classes of smoother transfer functions, this process results, under the proper conditions, in an effective smoothing which is very nearly directly dependent on n_1T_2. In other words, the cascaded smoothers are effectively equivalent to a single smoother having the high data handling rate of the first smoother and the long smoothing time of the second. The conditions under which this holds are $n_1 \gg n_2$ and n_1T_1 of the same order of magnitude as n_2T_2.

II. Single-Step Smoothing

In a digital computer, smoothing of noisy data is accomplished by taking a weighted average of the past input data. The weight assigned to any observation depends only on its age, i.e., on the number of succeeding observations. Let W_η be the weight assigned to the observation of age η ($\eta=0, 1, 2, \cdots$), with weight W_0 applying to the current observation. Let N be the total number of observations which have been made. Then the smoothed output, y_0, is related to the inputs, X_η ($\eta=0, 1, 2, \cdots$) by

$$y_0 = \sum_{\eta=0}^{N} W_\eta X_\eta. \tag{1}$$

The cases of interest here are those in which steady state conditions prevail, i.e., N is very large. Under these conditions, (1) may be modified to the form

$$y_0 = \sum_{\eta=0}^{\infty} W_\eta X_\eta. \tag{2}$$

The autocorrelation of the output, $\psi_y(\tau)$, is the ensemble average of y_0y_τ, where y_τ was the ouput τ observations ago. Thus, using overscoring to denote an average,

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, April 23, 1953.

† Sperry Gyroscope Company, Great Neck, L. I., N. Y.

$$\psi_y(r) = \overline{y_0 y_r} = \overline{\sum_{\eta=0}^{\infty} W_\eta X_\eta \sum_{\rho=0}^{\infty} W_\rho X_{\rho+r}}$$

$$= \sum_{\eta=0}^{\infty} \sum_{\rho=0}^{\infty} W_\eta W_\rho \overline{X_\eta X_{\rho+r}}. \tag{3}$$

It will be assumed that data consist only of random noise with standard deviation σ_I, mean zero, and no autocorrelation. (The assumption of zero signal is a matter of convenience. The use of another nonrandom signal would not change the basic arguments, since the purpose of this analysis is to show the effect of the smoothing on the noise.) These assumptions imply that

$$\begin{aligned} \overline{X_i X_j} &= \sigma_I^2 \quad \text{for} \quad i = j \\ &= 0 \quad \text{for} \quad i \neq j. \end{aligned} \tag{4}$$

Applying (4) to (3)

$$\psi_y(r) = \sigma_I^2 \sum_{\eta=0}^{\infty} W_\eta W_{\eta+r}. \tag{5}$$

The variance of the output, σ_0^2, is merely $\psi_y(0)$. Thus, the ratio of the variances of the output and input noise is

$$\frac{\sigma_0^2}{\sigma_I^2} = \sum_{\eta=0}^{\infty} W_\eta^2. \tag{6}$$

The value of (6) depends, of course, on the nature of the weighting factors. Three sets of factors will be considered. The first results in the taking of a straight average over a finite number of observations:

$$\begin{aligned} W_\eta &= \frac{1}{M} \quad \text{for} \quad 0 \leqq \eta < M \\ &= 0 \quad \text{for} \quad \eta \geqq M. \end{aligned} \tag{7}$$

The second set is the geometric series:

$$W_\eta = A e^{-\alpha\eta}. \tag{8}$$

The third set of weighting factors gives the digital equivalent of second order smoothing:

$$W_\eta = A_1 e^{-\alpha_1 \eta} + A_2 e^{-\alpha_2 \eta}, \tag{9}$$

where A_1 and A_2 form a complex conjugate pair and α_1 and α_2 form another such pair.

Now let the smoother's input (and output) rate be n observations per second. The definition of smoothing time, T, is somewhat arbitrary and must be fitted to the type of weighting factor under consideration. For the straight average (7), it is logical to define T as the time required to make the M observations entering into the average, that is

$$T = \frac{M}{n}. \tag{10}$$

Thus in this case

$$\frac{\sigma_0^2}{\sigma_I^2} = \sum_{\eta=0}^{M-1} \frac{1}{M^2} = \frac{1}{M} = \frac{1}{nT}. \tag{11}$$

For a smoother described by (8), T can be defined as the time required to reduce the weighting factor to $1/e$. Then α is given by

$$\alpha = \frac{1}{nT}. \tag{12}$$

The sum of the weighting factors must be 1 in any case. Thus A can be found from

$$A \sum_{\eta=0}^{\infty} e^{-\eta/nT} = 1. \tag{13}$$

Using the well known formula for the sum of a geometric series,

$$A = 1 - e^{-1/nT}. \tag{14}$$

Using (12) and (14) in (8) and then applying (6),

$$\begin{aligned} \frac{\sigma_0^2}{\sigma_I^2} &= (1 - e^{-1/nT})^2 \sum_{\eta=0}^{\infty} e^{(2/nT)\eta} \\ &= \frac{(1 - e^{-1/nT})^2}{1 - e^{-2/nT}} = \frac{1 - e^{-1/nT}}{1 + e^{-1/nT}} = \tanh \frac{1}{2nT}. \end{aligned} \tag{15}$$

For x small, $\tanh x$ is very nearly equal to x. (If x is 0.1 the error will be less than 0.35 per cent.) In any practical applications, the total number of observations in the smoothing time, nT, will be quite large (certainly greater than 5), so that $1/2nT$ will be small and the approximation will be applicable to (15). Thus

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1}{2nT}. \tag{16}$$

When the weighting factors are of the form (9), the smoothing time can conveniently be defined as the time required for the envelope of W_η to decrease from its value at time zero by a factor of $1/e$. This means that the real parts of α_1 and α_2 must equal $1/nT$. The imaginary parts will be arbitrary. It is convenient to write

$$\begin{aligned} \alpha_1 &= \frac{1}{nT}(1 - jb), \\ \alpha_2 &= \frac{1}{nT}(1 + jb). \end{aligned} \tag{17}$$

The values of A_1 and A_2 are subject only to the limitations that they be conjugate and that the sum of the weights be zero. An infinite number of combinations are possible, but two are of particular interest. They are

$$\begin{aligned} A_1 &= \frac{1}{nT}\left(1 + j\,\frac{1 - b^2}{2b}\right), \\ A_2 &= \frac{1}{nT}\left(1 - j\,\frac{1 - b^2}{2b}\right), \end{aligned} \tag{18}$$

and

$$A_1 = j\frac{1}{nT}\,\frac{1+b^2}{2b}, \qquad A_2 = -j\frac{1}{nT}\,\frac{1+b^2}{2b}. \tag{19}$$

The first set of values corresponds to a smoother transfer function which is the digital counterpart of the often encountered continuous smoothing function,

$$\frac{Y_{\text{out}}(S)}{Y_{\text{in}}(S)} = \frac{AS+B}{S^2+AS+B}, \tag{20}$$

while the second set corresponds to

$$\frac{Y_{\text{out}}(S)}{Y_{\text{in}}(S)} = \frac{B}{S^2+AS+B}. \tag{21}$$

Now using (9) in (6), and noting that the summed expression can be broken into two conjugate terms, the ratio of the output and input variances in the general second-order case is

$$\frac{\sigma_0^2}{\sigma_I^2} = 2Re\left(\frac{A_1^2}{1-e^{-2\alpha_1}} + \frac{A_1A_2}{1-e^{-(\alpha_1+\alpha_2)}}\right). \tag{22}$$

Assuming that nT is large, this can be approximated by

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq 2Re\left(\frac{A_1^2}{2\alpha_1} + \frac{A_1A_2}{\alpha_1+\alpha_2}\right). \tag{23}$$

Using (17) and (18) in (23) gives

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{5+b^2}{4nT}. \tag{24}$$

For A_1 and A_2 given by (19) the ratio is

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1+b^2}{4nT}. \tag{25}$$

Equations (11), (16), (24), and (25) show that in all the cases considered, the ratio of the variances of the output and input errors is inversely proportional to nT. This establishes the desirability of having both n and T large. However, as was mentioned in the introduction, it is not always possible to combine a high data handling rate and a long smoothing time in the same smoother. It will be shown in the next section, however, that this desirable combination of qualities can be effectively obtained by using two smoothers in series.

III. Two-step Smoothing

When two smoothers are used in series, the output of the first, as given by (2), is applied as the input to the second. Thus if W_ν' is the weighting factor for the second smoother, the variance of its output is

$$\sigma_0^2 = \left[\sum_{\nu=0}^{\infty} W_\nu' y_\nu\right]^2 = \sum_{\mu=0}^{\infty}\sum_{\nu=0}^{\infty} W_\mu' W_\nu' \overline{y_\mu y_\nu}. \tag{26}$$

Let the data handling rate of the first smoother be n_1 observations per second, that of the second smoother n_2 observations per second, with $n_1 \gg n_2$. Then two pieces of data which are m observations apart going into the second smoother were $(n_1/n_2)m$ observations apart coming out of the first smoother. Thus in (26),

$$\overline{y_\mu y_\nu} = \psi_y\left(\frac{n_1}{n_2}|\mu-\nu|\right), \tag{27}$$

where ψ_y is the auto-correlation of the first smoother output, defined by (3), and the absolute value is used to cover the cases $\nu > \mu$. Using (5) in (27) and then substituting the result into (26) gives for the ratio of the output and input variances,

$$\frac{\sigma_0^2}{\sigma_I^2} = \sum_{\mu=0}^{\infty} W_\mu' \left\{ \sum_{\nu=0}^{\mu-1} W_\nu' \sum_{\mu=0}^{\infty} W_\eta W_{\eta+n_1/n_1(\mu-\nu)} + \sum_{\nu=\mu}^{\infty} W_\nu' \sum_{\eta=0}^{\infty} W_\eta W_{\eta+n_1/n_2(\nu-\mu)} \right\}. \tag{28}$$

It will be noted that the absolute value has been handled by breaking the terms up into two sets, those for which $\mu > \nu$ and those for which $\mu \leqq \nu$.

In evaluating (28), it will be assumed first that both smoothers are of straight averaging type, with weighting factors, as derived from (7) and (10),

$$\begin{aligned} W_\eta &= \frac{1}{n_1T_1} && \text{for} \quad 0 \leqq \eta < n_1T_1 \\ &= 0 && \text{for} \quad \eta \geqq n_1T_1 \\ W_\eta' &= \frac{1}{n_2T_2} && \text{for} \quad 0 \leqq \eta < n_2T_2, \\ &= 0 && \text{for} \quad \eta \geqq n_2T_2 \end{aligned} \tag{29}$$

where T_1 and T_2 are the smoothing times of the first and second units respectively, $T_2 \gg T_1$. Using (49) in (28) and performing the indicated summations, first on η, then on ν, and finally on μ, the ratio of the variances for $(T_2/T_1) \geqq 2$ is given by

$$\frac{\sigma_0^2}{\sigma_I^2} = \frac{1+n_2T_1}{n_1n_2T_2^2}\left(\frac{T_2}{T_1} - 1 + \frac{2n_2T_1+1}{3n_2T_1}\right), \tag{30}$$

or, since T_2/T_1 is a large number

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1+n_2T_1}{n_1n_2T_2^2}. \tag{31}$$

If n_2T_1 is large compared to 1, this can be further approximated by

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1}{n_1T_2}. \tag{32}$$

Comparing (32) with (11), it can be seen that the two averaging smoothers in series are approximately equivalent to a single smoother having the high data handling rate of the first smoother, n_1, and the long smoothing time of the second, T_2. In other words, the series combination acts like a single smoother combining the best qualities of each of the individual smoothers.

The same type of analysis can be applied to pairs of smoothers of the other types considered in section II. For example, suppose the two sets of weighting factors are exponential:

$$W_\eta = Ae^{-\alpha\eta}$$
$$W_\eta' = Be^{-\beta\eta},$$

where

$$\alpha = \frac{1}{n_1T_1}, \qquad \beta = \frac{1}{n_2T_2} \tag{33}$$
$$A = 1 - e^{-1/n_1T_1}, \qquad B = 1 - e^{-1/n_2T_2}.$$

Performing the summations of (28),

$$\frac{\sigma_0^2}{\sigma_I^2} = \frac{A^2B^2}{(1-e^{-2\alpha})(1-e^{-2\beta})}\coth\frac{\frac{n_1}{n_2}\alpha+\beta}{2}, \tag{34}$$

Making use of (34), this becomes

$$\frac{\sigma_0^2}{\sigma_I^2} = \frac{\tanh\frac{1}{2n_1T_1}\tanh\frac{1}{2n_2T_2}}{\tanh\left(\frac{1}{2n_2T_1}+\frac{1}{2n_2T_2}\right)}, \tag{35}$$

and approximating tanh x by x

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1}{2n_1(T_1+T_2)}, \tag{36}$$

which for $T_2 \gg T_1$ can be further approximated by

$$\frac{\sigma_0^2}{\sigma_I^2} = \frac{1}{2n_1T_2}. \tag{37}$$

Comparison of (38) with (16) shows that in this case too, the series combination is approximately equivalent to a single smoother having data handling rate n_1 and smoothing time T_2.

Finally, consider the case of two second order smoothers, with weighting factors given by (9). For the first smoother the quantities A_1, A_2, α_1, and α_2 will be as given in (17) and (18) or (19), with $n = n_1$ and $T = T_1$. For the second smoother the parameters will be designated B_1, B_2, β_1, β_2. The same equations will hold for these as for the corresponding A's and α's except that n_2 will replace n_1 and T_2 will replace T_1. Carrying out the summations and noting that the final result can be written as the sum of two conjugate terms,

$$\frac{\sigma_0^2}{\sigma_I^2} = 2Re\left\{\left(\frac{A_1^2}{e^{-2\alpha_1}}+\frac{A_1A_2}{e^{-(\alpha_1+\alpha_2)}}\right)\right.$$

$$\left.\cdot\left[\left(\frac{B_1^2}{e^{-2\beta_1}}+\frac{B_1B_2}{e^{-(\beta_1+\beta_2)}}\right)\coth\frac{\frac{n_1}{n_2}\alpha_1+\beta_1}{-2} = +\left(\frac{B_2^2}{e^{-2\beta_1}}+\frac{B_1B_2}{e^{-(\beta_1+\beta_2)}}\right)\coth\frac{\frac{n_1}{n_2}\alpha_1+\beta_2}{-2}\right]\right\}. \tag{38}$$

Approximating e^{-x} by x and coth x by $1/x$ and using (18) for the A's and B's, the expression for the ratio of the variances is found to be

$$\frac{\sigma_o^2}{\sigma_I^2} \cong \frac{3b^4+10b^2-9+\frac{(T_1+T_2)^2}{(T_1+T_2)^2+b^2(T_1-T_2)^2}(b^2+1)^2(b^2+9)}{16b^2n_1(T_2+T_2)}. \tag{39}$$

If (19) is used for the constants,

$$\frac{\sigma_0^2}{\sigma^2} \simeq \frac{3b^2-1+\frac{(T_1+T_2)^2}{(T_1+T_2)^2+b^2(T_1-T_2)^2}(b^2+1)^2}{16b^2n_1(T_1+T_2)}. \tag{40}$$

If $T_2 \gg T_1$ (39) and (40) respectively reduce to

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{5+b^2}{4n_1T_2}, \tag{41}$$

and

$$\frac{\sigma_0^2}{\sigma_I^2} \simeq \frac{1+b^2}{4n_1T_2}. \tag{42}$$

Comparing (41) and (42) with (24) and (25) it can be seen that effective smoothing in each case is approximately equal to that which could be obtained with a single smoother having data handling rate n_1 and smoothing time T_2.

Various other types and combinations of smoothers could be considered. It is not necessary, in general, that the two smoothers be of the same type. For example, if the two smoothers are both of the second order type with the first having the coefficients given in (19) and the second those of (18), the resultant value of σ_0^2/σ_I^2 can be approximated by (41). That is, the change in the type of the first smoother does not, in this case, affect the final result.

The principle considered here extends generally to smoothers which operate by taking weighted averages of discrete data. Essentially, the first smoother functions as a correlator, so that each of its outputs contains information regarding a number of inputs. The second smoother, then, can obtain from a small fraction of the outputs of the first smoother almost as much information as it could obtain by looking at all of the original data. It can therefore produce smoothing which is approximately equivalent to that which would result if it operated at the input data rate.

TABLE I

Type	Weighting Factors	Approximate σ_0^2/σ_I^2 for Single Smoothing	Approximate σ_0^2/σ_I^2 for Double Smoothing	Improvement factors $T_1 = 1$ sec $n_1 = 400$ obs/sec, $T_2 = 20$ sec $n_2 = 4$ obs/sec, $b = \frac{1}{2}$			
				1st only	2nd only	Series	Single with n_1, T_2
Straight Average	$\frac{1}{nT}$ *for* $0 \leqq \eta < nT$ 0 *for* $\eta \geqq nT$	$\frac{1}{nT}$	$\frac{1+n_2T_1}{n_1n_2T_1T_2}$	20.0	8.9	80.0	89.4
Exponential	$(1-e^{-1/nT})e^{-\eta/nT}$	$\frac{1}{2nT}$	$\frac{1}{2n_1(T_1+T_2)}$	28.3	12.6	129.6	126.5
Second Order (a)	$\frac{1}{nT}\left(1+j\ \frac{1-b^2}{2b}\right)e^{-[(1-jb)/\eta T]\eta}$ $\frac{1}{nT}\left(1-j\ \frac{1-b^2}{2b}\right)e^{-[(1+jb)/nT]\eta}$	$\frac{5+b^2}{4nT}$	$\frac{3b^4+10b^2-9+\frac{(T_1+T_2)^2}{(T_1+T_2)^2+b^2(T_1-T_2)^2}(b^2+1)^2(b^2+9)}{16b^2n_1(T_1+T_2)}$	17.0	7.6	75.4	76.2
Second Order (b)	$j\,\frac{1+b^2}{2bnT}\left[e^{-[(1-jb)/nT]\eta} + e^{-[(1+jb)/nT]\eta}\right]$	$\frac{1+b^2}{4nT}$	$\frac{3b^2-1+\frac{(T_1+T_2)^2}{(T_1+T_2)^2+b^2(T_1-T_2)^2}(b^2+1)^2}{16b^2n_1(T_1+T_2)}$	32.7	14.6	180.0	146.0

IV. CONCLUSIONS

The results of this study are summarized in Table I. The last four columns present the results of a specific numerical example. The numbers in these columns are the improvement factors, σ_I/σ_0, found by taking the reciprocals of the square roots of the appropriate variance ratios. These are the factors by which the rms noise level is reduced by the smoothing. These show clearly that the effect of double smoothing is always very close to that of a single n_1, T_2 smoother, with the double smoother sometimes giving slightly greater improvement, sometimes slightly less. Comparisons should be made only between single and double smoothing for a given type of smoother; comparisons between types are not valid, owing to the variation in the definition of smoothing time.

* * *

An AM-FM Electronic Analog Multiplier*

WILLIAM A. McCOOL†, ASSOCIATE, IRE

Summary—**This paper describes an electronic multiplier wherein the input voltages are made proportional to the respective indices of amplitude and frequency modulations of a radio frequency carrier with the aid of feedback stabilization. The desired product of the input voltage is obtained from a Foster-Seeley discriminator whose output is independently proportional to each modulation index after the carrier component is subtracted out.**

Performance of the AM-FM multiplier is essentially independent of vacuum tube characteristics by virtue of the feedback stabilization and is limited primarily by the stability of the discriminator parameters. Other features of the multiplier are: ease and rapidity of adjustment; conventional AM and FM receiver circuitry; long-time multiplication error of less than 1 per cent of full scale output; usable bandwidth (flat amplitude response and less than 15 degrees phase-shift for highest frequency component) approximately 1 per cent of carrier frequency.

INTRODUCTION

THE UNUSUAL INTEREST and activity in the development of electronic analog multipliers since the last war suggests that some challenging and knotty problems are involved. In surveying the situation, it should be emphasized that feedback principles are the basis for the whole philosophy of analog computation and simulation, both in the mechanization of the mathematical equations as well as in the functioning of the components performing specific mathematical operations. As normally applied in computing components, feedback stabilizes the relation between a single input (which may be a sum of inputs) and a single output, such as in the operations of integration, constant multiplication, voltage regulation, and zero-drift elimination. A fundamental difficulty in applying feedback to a multiplying device arises from the fact that two inputs are required and they cannot be independently stabilized by feedback from the product output. In any multiplier, therefore, the characteristics of the basic product-forming element establish the limits of stability and accuracy. For example, a servomechanism multiplier is no better than its potentiometers.

In all analog computing components, rapid response (large bandwidth) and high computing accuracy inherently tend to be mutually exclusive properties. Where computing accuracy is of first importance the multiplying servo,[1,2] even with its limited speed of response, is the best compromise and, consequently, is universally employed. There is a definite need, nevertheless, for a much faster multiplier to extend the dynamic range of electronic analog computers with only a limited sacrifice in accuracy. A natural solution of this problem is an electronic multiplier such as the one described in this paper, the AM-FM multiplier, where in the Foster-Seeley[3] discriminator is the product-forming element and the modulation processes are stabilized with feedback. The AM-FM multiplier is one of the general type shown functionally in Fig. 1 and described as follows.

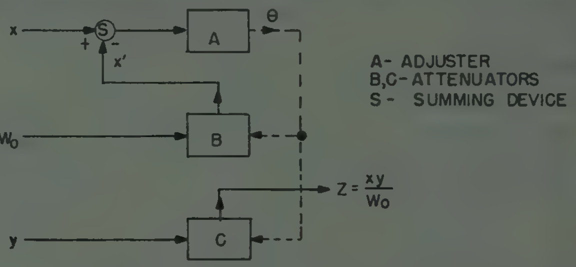


Fig. 1—Adjuster-attenuator multiplier.

If the nomenclature of Lentz and Greenwood[4] is used, A is called an "adjuster," and B and C are called "attenuators." B and C must be identical in every respect. Their gain θ is adjusted by A such that

$$x - x' = \epsilon \approx 0 \tag{1}$$

and

$$x' = \theta w_0 \approx x, \tag{2}$$

where w_0 is a reference quantity. Thus, if the error ϵ indicated in (1) is negligible, then according to (2), θ *is established by two externally controlled quantities.* The output of C is independently proportional to both its gain θ and its input y, i.e.,

$$z = \theta y. \tag{3}$$

Eliminating θ between (2) and (3) shows that the multiplier output is the xy product divided by the reference quantity w_0, or

$$z = \frac{xy}{w_0}, \tag{4}$$

in which the error ϵ is neglected. Equation (4), incidentally, suggests that the multiplier becomes a divider if it is possible to make w_0 a variable input quantity. Moreover, additional attenuators permit the multiplication of other y-quantities by the common factor x/w_0.

It is interesting to note that in every type of attenuator the nature of the input quantities (e.g., w_0 and θ in the B attenuator of Fig. 1) must be essentially different so that the information contained in either input can be recovered and separated from the other. It will be

---

* Decimal classification: 621.385.2. Original manuscript received by the Institute, June 6, 1953; Revised manuscript received, July 23, 1953.

† Naval Research Laboratory, Washington, D. C.

[1] S. Frost, "A compact analog computer," *Electronics*, pp. 116–122; July, 1948.

[2] Project Typhoon Summary Progress Reports; September/November/December, 1947.

[3] S. W. Seeley, "Balanced Phase-Shift Discriminators," RCS Lab. Report LB666; March, 1946.

[4] I. A. Greenwood, Jr., J. V. Holdam, Jr. and D. MacRae, Jr., "Electronic Instruments," M.I.T. Radiation Lab. Series, vol. XXI, McGraw-Hill Book Co., New York, N. Y.; 1948.

convenient to call this the "discrimination" property of the attenuator. The property is clearly illustrated in the servomechanism multiplier wherein the amplifier and servomotor comprise the adjuster *A*, the follow-up potentiometer comprises the attenuator *B*, and the multiplying potentiometer comprises the attenuator *C*. In the follow-up potentiometer, shaft position information θ is recovered as proportional voltage x when the excitation is a fixed quantity w_0.

A satisfactory multiplier must afford four-quadrant operation, i.e., polarity as well as magnitude of both input quantities must be preserved. If the physical mechanisms employed do not preserve the sense of either or both of the inputs, it is a simple matter to extend the multiplication to four-quadrant operation (Appendix I).

FUNCTIONAL DESCRIPTION OF THE AM-FM MULTIPLIER

The electronic multiplier described in this paper employs the adjuster-attenuator principle. Feedback circuits are extensively applied to make the over-all stability depend primarily on "passive" components (inductors, resistors, capacitors), i.e., variations in the vacuum-tube characteristics enter only as second order effects. Since frequency and voltage are essentially different quantities, they are suitable inputs for simultaneous modulation of the frequency and amplitude of a radio-frequency carrier with the respective input quantities, which are slowly varying (low frequency compared to the carrier frequency) direct current voltages. Demodulation is effected with a frequency modulation discriminator-detector.

In the basic scheme, the actual quantities whose product is formed are frequency modulation "deviation" and carrier amplitude. If the conventional demodulation process is employed (Figs. 4 and 5) the polarity of the frequency modulation information is preserved, while the information in the carrier amplitude is devoid of polarity unless the latter quantity is made proportional to the amplitude modulation index rather than to the amplitude of the carrier itself. This expedient effectively extends the operation of a two-quadrant multiplying device to four quadrants (Appendix I) since, as shown in the following paragraph, a demodulator output component proportional to the frequency modulation variable must be subtracted out. Four-quadrant operation can be attained also with suppressed carrier modulation techniques.

The functional diagram of the AM-FM multiplier is shown in Fig. 2, and the descriptive equations are:

$$x = \theta w_0 \tag{5}$$

$$z' = \theta(y + w_0) = \frac{x}{w_0}(y + w_0) = \frac{xy}{w_0} + x, \tag{6}$$

and

$$z = z' - x = \frac{xy}{w_0}, \tag{7}$$

in which the error ϵ is again neglected. From the correspondence between the diagrams of Figs. 1 and 2 it is easily seen that the adjuster *A* consists of a high-gain dc amplifier and a frequency-modulated oscillator whose frequency deviation is "adjusted." The attenuators *B* and *C* each consist of a current summing network, a

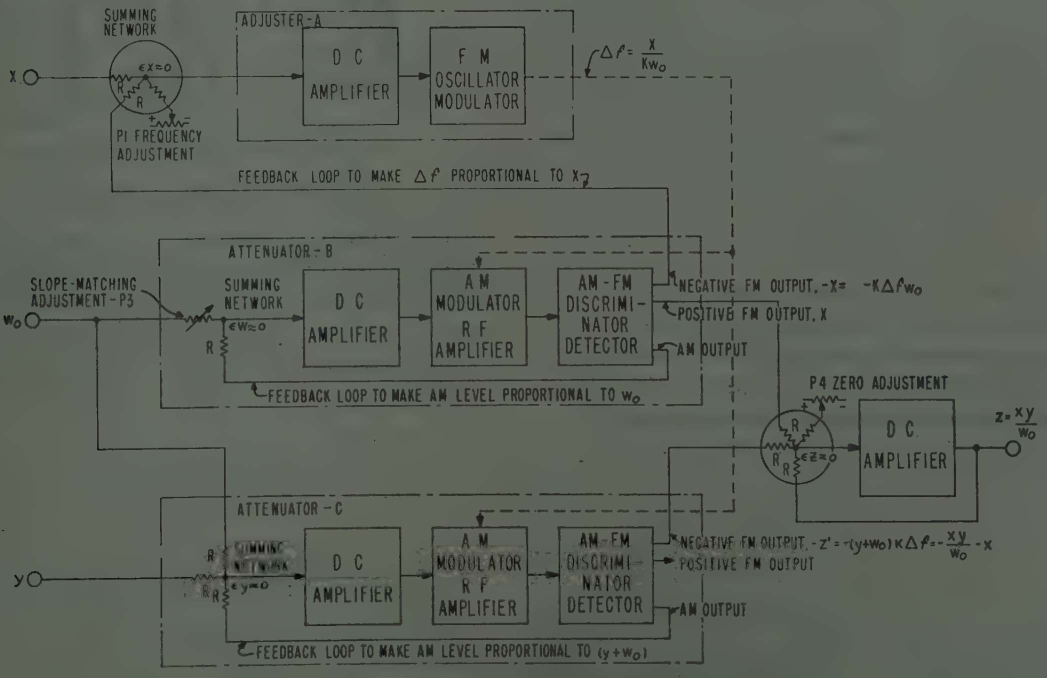

SUMMING NETWORK
ADJUSTER-A
D C AMPLIFIER
F M OSCILLATOR MODULATOR
$\Delta f = \frac{X}{Kw_0}$
X
$\epsilon x \approx 0$
R
R
R
PI FREQUENCY ADJUSTMENT
FEEDBACK LOOP TO MAKE Δf PROPORTIONAL TO X
ATTENUATOR - B
SLOPE-MATCHING ADJUSTMENT - P3
w_0
SUMMING NETWORK
$\epsilon w \approx 0$
R
D C AMPLIFIER
A M MODULATOR R F AMPLIFIER
AM - FM DISCRIMI-NATOR DETECTOR
NEGATIVE FM OUTPUT, $-X = -K\Delta f w_0$
POSITIVE FM OUTPUT, X
AM OUTPUT
FEEDBACK LOOP TO MAKE AM LEVEL PROPORTIONAL TO w_0
P4 ZERO ADJUSTMENT
R
R
R
R
$\epsilon z \approx 0$
D C. AMPLIFIER
$z = \frac{xy}{w_0}$
ATTENUATOR - C
y
R
R
R
SUMMING NETWORK
$\epsilon y \approx 0$
D C AMPLIFIER
A M MODULATOR R F AMPLIFIER
AM-FM DISCRIMI-NATOR DETECTOR
NEGATIVE FM OUTPUT, $-z' = -(y+w_0)K\Delta f = -\frac{xy}{w_0} - x$
POSITIVE FM OUTPUT
AM OUTPUT
FEEDBACK LOOP TO MAKE AM LEVEL PROPORTIONAL TO $(y+w_0)$

Fig. 2—Simplified block diagram of AM-FM multiplier.

high-gain dc amplifier, and an FM discriminator-detector whose AM gain is proportional to the frequency deviation. The gain θ corresponds to the frequency deviation.

The feedback loop containing the adjuster A and the attenuator B is a familiar automatic frequency control system.[5,6] The high loop gain provided by the dc amplifier forces the demodulated FM output of the detector (the difference between two rectified voltages, a and b, the development of which is explained later), via a current summing network, to match the x-input voltage within a negligible error, thus satisfying (1). The feedback loop within each attenuator is a familiar amplified automatic gain control system.[7] The high loop gain provided by the dc amplifier in each attenuator forces the AM output of the detector (the sum of the two rectified voltages, a and b) to match an input voltage via a current summing network. Thus, once the w_0-reference voltage is held fixed, the frequency deviation for a given x-input voltage is forced to depend only on the circuit constants of the discriminator (including all reflected impedances) and on the resistors of the associated current summing networks. This establishes the gain θ according to (2).

According to (6) the FM output of attenuator C, z', is proportional to both the established frequency deviation and the sum of the y-input and the w_0-reference voltages. Equation (7) indicates that, if the x-input voltage is subtracted from the C attenuator FM output, the desired product z is obtained. As shown in Fig. 2, the subtraction operation is effected by summing the positive FM output (x) of the B attenuator with the negative FM output ($-z'$) of the C-attenuator by means of the usual resistor network and high-gain dc amplifier.

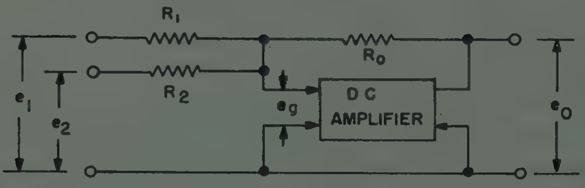


Fig. 3—Summing amplifier.

Each of the four current summing networks is similar to that found in conventional summing amplifiers.[1] In the simple example of such an amplifier shown in Fig. 3, the sum of the currents at the resistor junction connected to the high-gain amplifier input must be zero if there is no input grid current. Therefore,

$$\frac{e_1 - e_g}{R_1} + \frac{e_2 - e_g}{R_2} + \frac{e_0 - e_g}{R_0} = 0. \qquad (8)$$

When the amplifier gain is so high that e_g is negligibly small compared to e_1, e_2, and e_0, then (8) is reduced to:

$$\frac{e_1}{R_1} + \frac{e_2}{R_2} + \frac{e_0}{R_0} \approx 0, \qquad (9)$$

and the amplifier output voltage is:

$$e_0 = -\frac{R_0}{R_1} e_1 - \frac{R_0}{R_2} e_2. \qquad (10)$$

Thus for all practical purposes the gain-with-feedback for any input is determined by the output-input resistance ratio and, therefore, is just as stable as the resistors themselves. With this "current-summation" type of feedback the demodulated attenuator outputs are currents which are proportional to the rectified voltages of interest.

In order to simplify the description of the AM-FM multiplier, all the resistors have been assumed to have the same value, thus entirely eliminating resistance ratios from all the equations. In a practical multiplier, this will not be the case because the various voltage levels, which are controlled by the resistance ratios, will be dictated by design considerations.

In the above example, it should be noted that the only specification of the amplifier was high gain. Except for frequency response and transient response considerations, therefore, the amplifier could contain physical-quantity conversions and inversions such as voltage-shaft rotation or voltage-frequency deviation.

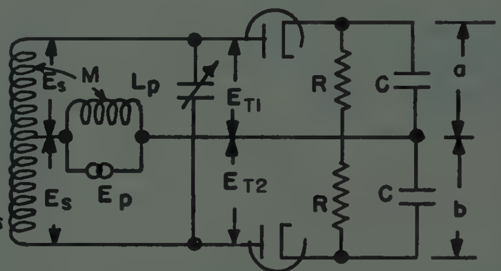


Fig. 4—Foster-Seeley phase discriminator.

THE DISCRIMINATOR DETECTOR

The circuit of a simple Foster-Seeley phase discriminator[3] is illustrated in Fig. 4 wherein $2E_S$ is the complex amplitude of the RF voltage developed across the secondary winding. The RF voltages presented to the respective series diode detectors are $\overrightarrow{E_{T_1}}$ and $\overrightarrow{E_{T_2}}$ which are the vector sums,

$$\overrightarrow{E_{T_1}} = \overrightarrow{E_P} + \overrightarrow{E_S} \qquad (11)$$

and

$$\overrightarrow{E_{T_2}} = \overrightarrow{E_P} - \overrightarrow{E_S}. \qquad (12)$$

The corresponding rectified voltages are:

$$a = \left|\overrightarrow{E_{T_1}}\right| = \left|\overrightarrow{E_P} + \overrightarrow{E_S}\right| \qquad (13)$$

---

[5] H. Roder, "Theory of the discriminatory circuit for automatic frequency control," Proc. IRE: vol. 26, pp. 590–611; May, 1938.

[6] W. L. Mraz, "Automatic Frequency Control as a Feedback Problem," Bell Lab. Internal Memo., Case 26500.

[7] B. M. Oliver, "AVC as a feedback problem," Proc. IRE, vol. 36, pp. 466–473; April, 1948.

nd

$$b = |\overrightarrow{E_{T_2}}| \doteq |\overrightarrow{E_P} - \overrightarrow{E_S}|, \qquad (14)$$

here the rectification efficiency of the diodes is as-umed to be perfect.

The voltage $a-b$ is the normal FM output of the dis-iminator detector, although frequency modulation oes produce some amplitude variation in the voltage $+b$. Since both of these voltages are proportional to e RF excitation voltage E_P, their ratio:

$$R = \frac{a-b}{a+b}, \qquad (15)$$

invariant with amplitude modulation. Thus if the agnitude of $a+b$ can be "clamped" at some constant alue, then the magnitude of $a-b$ will vary only with equency modulation. This, of course, is the well-nown ratio-detector principle[8] and is used to great dvantage in the AM-FM multiplier. In the B attenu-tor, $a+b$ is clamped at the w_0-reference voltage and we an write:

$$w_0 = a_w + b_w. \qquad (16)$$

ut $a-b$ is forced to match the x-input voltage so that:

$$x = a_w - b_w, \qquad (17)$$

here the error ϵ is neglected. Similarly, for the C at-enuator, we can write:

$$w_0 + y = a_y + b_y \qquad (18)$$

nd

$$z' = a_y - b_y. \qquad (19)$$

Substituting (16) and (17) into (5) and solving for he attenuation θ gives:

$$\theta = \frac{x}{w_0} = \frac{a_w - b_w}{a_w + b_w} = K\Delta f, \qquad (20)$$

here Δf is the frequency deviation. Substituting (18) nd (19) into (6) and again solving for θ, we have:

$$\theta = \frac{z'}{w_0 + y} = \frac{a_y - b_y}{a_y + b_y} = K\Delta f. \qquad (21)$$

ince the frequency deviation is identical for both the 3 and C attenuators, the respective gains must be lentical. From (20) and (21), therefore,

$$\theta = \frac{x}{w_0} = \frac{z'}{w_0 + y}, \qquad (22)$$

hich reduces to (6):

$$z' = \frac{xy}{w_0} + x.$$

Vhen the B attenuator voltage is subtracted from the attenuator output voltage z', again the desired result s (7):

$$z = z' - x = \frac{xy}{w_0}.$$

It should be pointed out that the results of the foregoing analysis are approximate since the error voltage in each current summing network has been neglected. However, these errors can easily be made negligible in a practical multiplier.

The schematic diagram of the discriminator-detector circuit in Fig. 5 illustrates one method of controlling the output voltages, $a+b$ and $a-b$. One pair of diodes, D_1 and D_2, is connected so that the sum of their dc load currents becomes the "feedback" current proportional to $a+b$, while the other pair, D_3 and D_4, is connected so that the difference of their dc load currents becomes the feedback current proportional to $a-b$. Thus, each pair of load resistors functions as a feedback resistor (i.e., corresponding to R_0 in Fig. 3) in the corresponding current summing network.

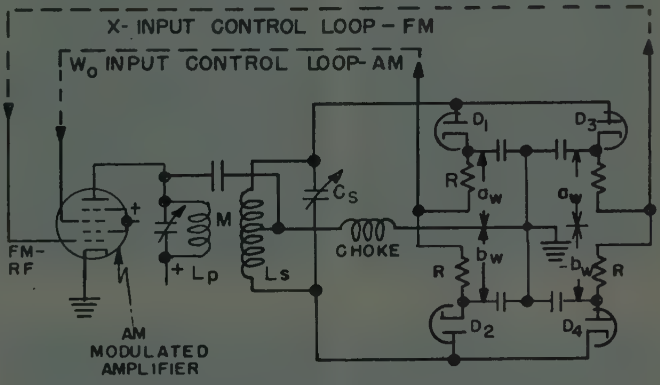


Fig. 5—Discriminator-detector circuit for AM-FM multiplier attenuator.

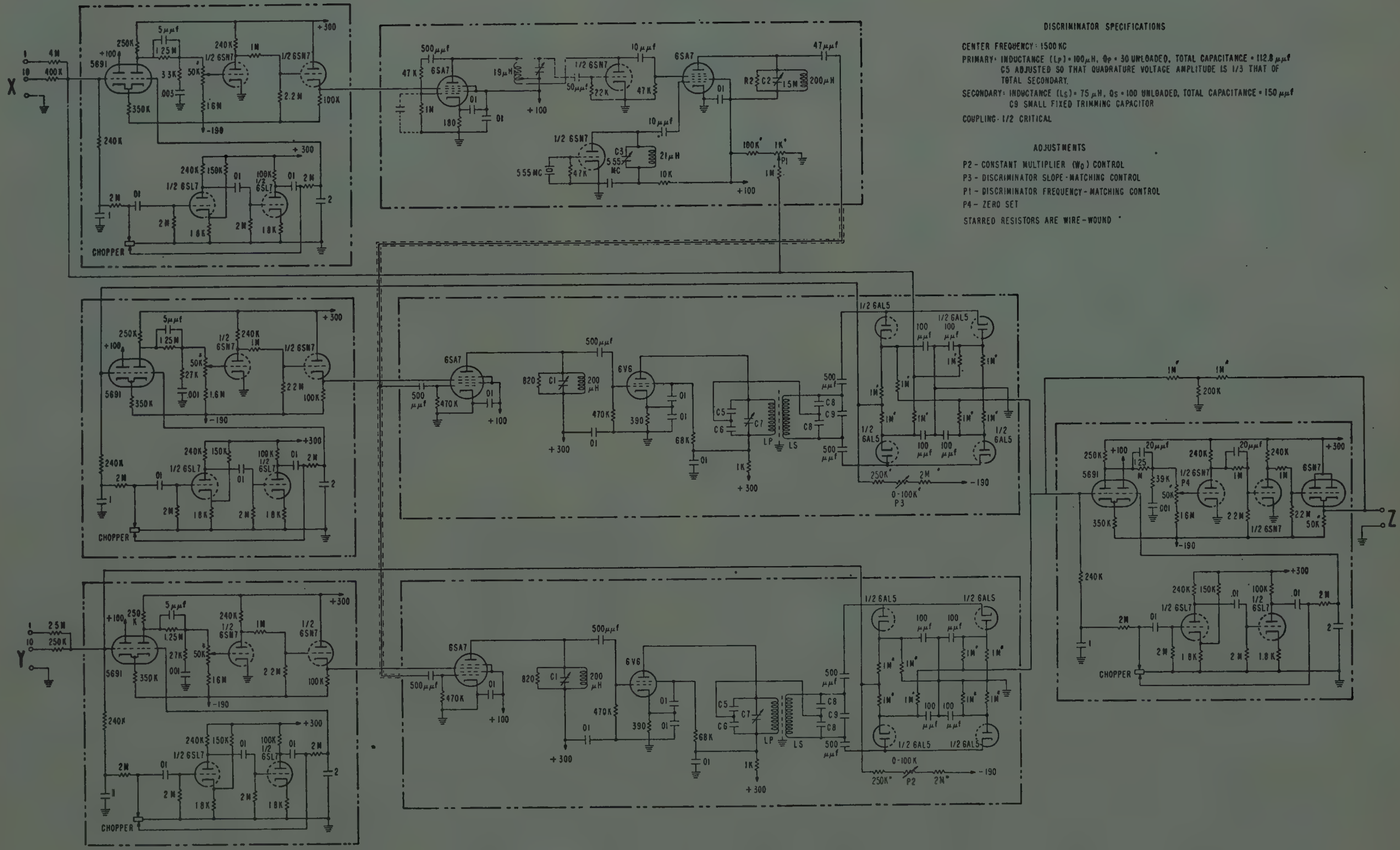
It has already been indicated that for specified values of the voltages $a+b$ and $a-b$, the "automatic frequency control" feedback loop forces the frequency deviation to depend upon the parameters of the discriminator-detector circuit. It is important that the FM modulator and oscillator are actually stages of the "equivalent" high-gain amplifier of the system, and are operating at high level with respect to the input level at the current summing junction. According to feedback theory, therefore, the drift in the center frequency of the oscillator and the drift in the conversion constants of the reactance tube modulator are practically eliminated by the feedback. In contrast, the effects of drift in the input grid-cathode voltage of the dc amplifiers (this input being the lowest signal level) are not altered by feedback and must be eliminated by more devious means (e.g., chopper stabilization[9]).

The success of any adjuster-attenuator type of multiplier depends upon how well attenuator characteristics can be matched and how well this match is maintained

---

[8] J. Avins, "The Radio Detector," RCA Lab. Report LB 710; Iay, 1947.

[9] E. A. Goldberg, "Stabilization of wide-band DC amplifiers for zero and gain," *RCA Review*, pp. 296–300; June, 1950.


X
Y
Z
5691
1/2 6SN7
6SN7
1/2 6SL7
CHOPPER
6SA7
6V6
1/2 6AL5
P1
P2
P3
P4
C1
C2
C3
C5
C6
C7
C8
C9
R2
LP
LS
+300
+100
-190
555 MC

DISCRIMINATOR SPECIFICATIONS

CENTER FREQUENCY: 1500 KC
PRIMARY: INDUCTANCE (Lp) = 100μH, Qp = 30 UNLOADED, TOTAL CAPACITANCE = 112.8 μμf
C5 ADJUSTED SO THAT QUADRATURE VOLTAGE AMPLITUDE IS 1/3 THAT OF
TOTAL SECONDARY.
SECONDARY: INDUCTANCE (Ls) = 75 μH, Qs = 100 UNLOADED, TOTAL CAPACITANCE = 150 μμf
C9 SMALL FIXED TRIMMING CAPACITOR
COUPLING: 1/2 CRITICAL

ADJUSTMENTS

P2 - CONSTANT MULTIPLIER (W_0) CONTROL
P3 - DISCRIMINATOR SLOPE-MATCHING CONTROL
P1 - DISCRIMINATOR FREQUENCY-MATCHING CONTROL
P4 - ZERO SET
STARRED RESISTORS ARE WIRE-WOUND *

Fig. 6—AM-FM multiplier schematic diagram.

over long operating periods. The x-input versus θ characteristic does not have to be specified, except that it should be identical in each attenuator. However, if the characteristic is inherently linear, the process for matching is greatly simplified, since the problem is analogous to curve fitting.

It is not too difficult to design a discriminator-detector whose $a-b$ versus Δf characteristic is linear within several tenths of a per cent of a maximum useful frequency deviation. This being the case in the AM-FM multiplier, matching discriminators is reduced to matching the $a-b$ versus Δf slope which is a function of discriminator parameters when $a+b$ is constrained.

Although some variations in the discriminator-detector characteristics, e.g., temperature coefficient, are unavoidable, remarkable stability can be attained by making the discriminators as much alike as possible so that these variations will "track" and thus cancel errors which alone might be intolerable. Improved stability, however, is always obtained when these variations are minimized in the beginning by proper design.

In any satisfactory multiplier, the alignment procedure must be simple and the adjustment of the controls must be smooth. In the AM-FM multiplier both of these requirements are satisfied. Two controls, which can be made available from the front panel if desired, are necessary in the C attenuator (and additional attenuators) in order to match the $(a-b)$ versus Δf slope and the zero of the B attenuator. The slope can be effectively adjusted by varying the discriminator output level which is controlled by the reference voltage w_0 (20) and the corresponding output-input resistance ratio (10). The zero adjustment simply trims the discriminator secondary capacitance.

EXPERIMENTAL MODEL

An experimental model of the AM-FM multiplier has been developed to show that the basic principles set forth in the preceding paragraphs are practicable and fundamentally sound. Fig. 6 is a schematic diagram of this model, which contains eleven vacuum tube envelopes, exclusive of power supplies and four chopper stabilized dc amplifiers for multiplying two input voltages. Each additional multiplicand requires an attenuator containing four tube envelopes and two dc amplifiers. Except for the discriminator design and construction, conventional AM and FM receiver-type circuitry is employed and the schematic diagram, therefore, is almost self-explanatory. It should be pointed out that the reference voltage proportional to w_0 is the -190 volt supply connection indicated in each AM modulator section.

Tests have shown that tubes do not have to be selected. All tubes can be replaced without any readjustments except for the discriminator diodes, in which slight variations in inter-electrode capacitance detune the discriminator secondary circuit.

Fig. 7 is a group of oscillograms illustrating some of the performance characteristics of the model. Fig. 7(a) is a two-to-one Lissajous pattern comparing a 100-cycle sine wave with its square performed by the multiplier. A phase shift of several degrees is apparent. Similarly, in Fig. 7(b), a 1,000-cycle sine wave is compared with its square in which some distortion is indicated by the pattern dissymmetry, indicating the familiar high-frequency overloading characteristic of feedback systems. The phase shift is approximately 17° at 2,000 cycles, one-third of which is contributed by the Y or AM input and the remainder by the X or FM input. The output product of a constant and a square wave with a 300 per second repetition rate is shown in Fig. 7(c) (square wave applied at the X input) and Fig. 7(d) (square wave applied at the Y input). For both inputs of the multiplier the frequency of the overshoot transient appears to be about 10 kc.

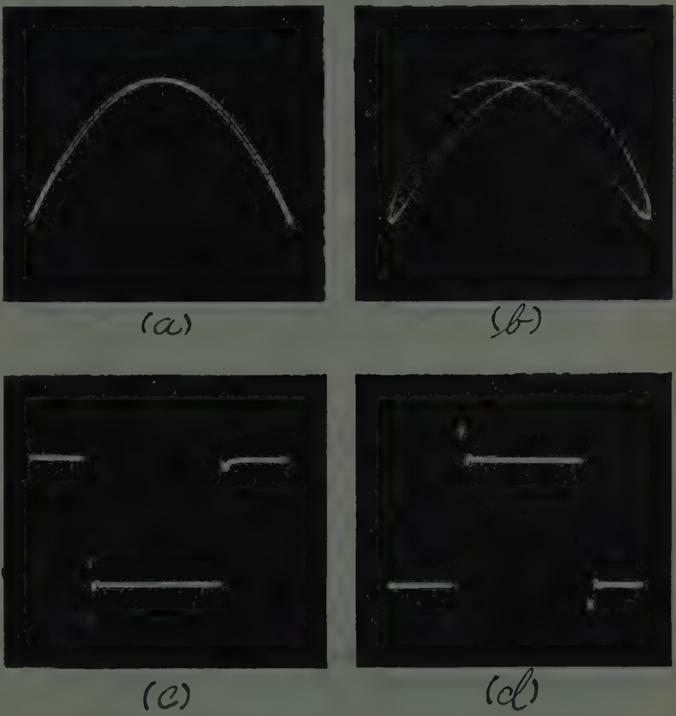


Fig. 7—Dynamic Performance oscillograms.

As a quantitative test of multiplication accuracy, a sine wave input of full-scale amplitude was multiplied by a constant input at various levels. The results listed in Table I indicate a maximum error of ±0.5 per cent full-scale output, not including a residual noise and drift content of 0.5 per cent. From multiplier equation, $Z=KXY$, errors were calculated based on the average K given by each set of Z, X, and Y measurements. This actually turned out within 0.69 per cent of the theoretical value based on the reference voltage, w_0. Estimated measurement errors was ±0.5 per cent.

Zero drift is unquestionably the greatest source of long-time error in the AM-FM multiplier. In the experimental model, zero drift was caused entirely by variations in the discriminator secondary inductance and/or capacitance due to ambient temperature variations. However, the measurements for Table I were made after several hours warm-up and immediately after adjustment of the model. After three hours, these measurements were duplicated within a few tenths of 1 per cent with no further adjustment. The ambient temperature during this period, however, was carefully controlled.

Adjustment of the multiplier consists of three steps: (a) adjust slope potentiometer P3 (just below the discriminator in the upper AM modulator section, Fig. 6) for zero sine wave output with no AM input (Y) and sine wave FM input (X); (b) adjust frequency potentiometer P1 (in the FM modulator section, Fig. 6) for zero sine wave output with no FM input (X) and sine wave AM input (Y); and (c) adjust zero-set potentiometer P4 (in the output summing amplifier, Fig. 6) for zero dc output. Any suitable means can be used for an output indicator. It should be noted that the frequency potentiometer P1 changes the controlled frequency in lieu of the retuning of the secondary circuit in the C discriminator.

TABLE I

ACCURACY EVALUATION OF AM-FM MULTIPLIER

$Y=1 \sin 2\pi\ 100t$		$X=1 \sin 2\pi\ 100t$	
X	error in $Z\%$	Y	error in $Z\%$
.1	.05	.1	−.01
.2	.11	.2	−.03
.3	.21	.3	−.25
.4	.33	.4	−.07
.5	.32	.5	−.21
.6	.44	.6	−.23
.7	.43	.7	−.31
.8	.27	.8	−.27
.9	.25	.9	−.35
1.0	.24	1.0	−.49

CONCLUSIONS

Based on the experimental results obtained with the model of the AM-FM multiplier it is concluded that:

1. The long-time computing error is within ±1.0 per cent of full scale; further development is expected to reduce this by a factor of 2 or 3.
2. The usable bandwidth for both inputs (flat amplitude response, less than 15° phase-shift for highest frequency component) is approximately 1 per cent of the carrier frequency.
3. Performance is independent of normal variations in vacuum tube characteristics.
4. Adjustment and servicing is simple and rapid.
5. Unlike time-division multipliers with their square-wave output, the AM-FM multiplier requires no output filter, the only noise being tube microphonics, power supply ripple, and drift.

ACKNOWLEDGMENT

Although this version of the AM-FM multiplier was originated and developed at the Naval Research Laboratory, the basic modulation scheme was independently developed and reported by engineers[10–12] at the Research Laboratory of Electronics, Massachusetts Institute of Technology, and in Great Britain. Moreover, it has been considered by a number of other workers in the field who, for one reason or another, did not exploit the possibilities. It is interesting to note that there are other types of dual modulation multipliers,[4,13–16] such as the ones now offered by several manufacturers which employ amplitude and pulse-width modulations, i.e., time division multipliers.

The author is greatly indebted to Dr. H. M. Trent, head of the Applied Mathematics Branch, Naval Research Laboratory, for his support and encouragement in this development, and to L. C. Rogers for the expeditious construction of the experimental model.

APPENDIX I

EXTENSION OF OPERATION OF A ONE-QUADRANT MULTIPLIER TO FOUR QUADRANTS

A one-quadrant multiplier senses only the magnitude of the input quantities which, therefore, must be restricted to one polarity in many computing applications where the polarity of the product is significant. The extension may be viewed as a "shift of origin" in the x-y plane with the change of variables:

$$x = \bar{x} - x_0, \qquad \bar{x} > 0 \tag{8}$$

and

$$y = \bar{y} - y_0, \qquad \bar{y} > 0. \tag{9}$$

The basic product, then, is:

$$\bar{z} = \frac{\bar{x}\bar{y}}{w_0}, \tag{10}$$

from which the desired product, given by (4), of the actual input quantities is obtained by substitution of the new variables in (10). Thus,

$$\begin{aligned} \bar{z} &= \frac{\bar{x}\bar{y}}{w_0} = \frac{(x + x_0)(y + y_0)}{w_0} \\ &= \frac{xy}{w_0} + \frac{x_0 y + x y_0 + x_0 y_0}{w_0} \end{aligned} \tag{11}$$

---

[10] R. Price, "An FM-AM Multiplier of High Accuracy and Wide Range," Tech. Report No. 213, Research Lab. of Elec., M.I.T.; Oct. 4, 1951.

[11] M. J. Somerville, "An electronic multiplier," *Elec. Eng.*; Feb., 1952.

[12] B. Chance, V. Hughes, E. F. MacNichol, D. Sayre, F. C. Williams, "Waveforms," M.I.T. Radiation Lab. Series, sec. 12.38, vol. xxi, McGraw Hill Book Co., New York, N. Y.; 1948.

[13] "Six-Channel Electronic Multiplier Model EM-101 MOD-0," Reeves Instrument Corp., Brochure No. R100 10 2M-2-52.

[14] W. R. Thomas and M. Squires, "Electronic Analogue Methods of Multiplication," RAE Tech. Note GW53, Farnborough; Oct., 1949.

[15] D. E. Garrett and F. G. Cole., "A general purpose electronic wattmeter," PROC. IRE, vol. 40, pp. 165–171; Feb., 1952.

[16] F. H. Hammond, "An Electronic Multiplier," TRE Tech. Note No. 114, Gt. Malvern, Worcs.; April, 1951.

or

$$z = \frac{xy}{w_0} = \bar{z} - \frac{x_0y + xy_0 + x_0y_0}{w_0}$$

$$= \frac{\bar{x}\bar{y}}{w_0} - \frac{x_0y + xy_0 + x_0y_0}{w_0}. \tag{12}$$

Fig. 8 is a functional diagram of the four-quadrant multiplier and is derived by augmenting Fig. 1 to include the correction terms indicated in (12) in which x_0, y_0, w_0 are constants.

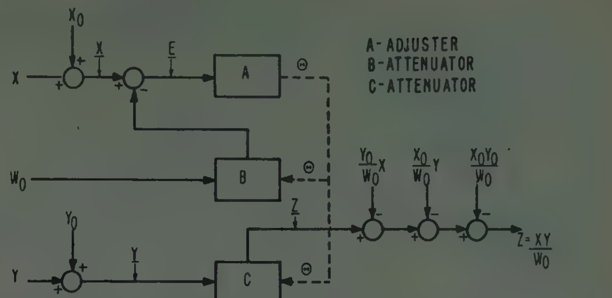


Fig. 8—Method for extending operation of an adjuster-attenuator multiplier from one to four quadrants.

The Magnetic Amplifier as an Analog Computer Component*

LEONARD J. CRAIG†, ASSOCIATE, IRE

Summary—Some of the basic concepts of obtaining desired function characteristics using magnetic amplifiers with idealized core characteristics are presented.

The core-characteristic test procedure is explained along with the results of some tests. The effect of parameter variation is shown and the causes of nonlinearities are discussed.

Some new magnetic amplifier circuitry is shown and their use in the analog computer field is indicated.

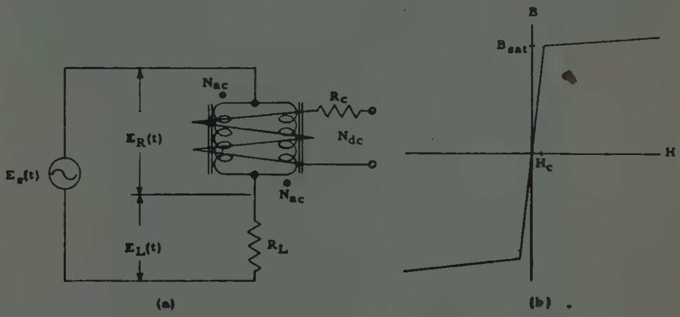
INTRODUCTION

IN RECENT YEARS the practical usage of magnetic materials with rectangular hysteresis loops has become quite evident in industrial control applications where large power-handling capacity is required. More recently these materials have come into the field of industrial electronics as stable circuit components in units where long standing stability is of prime consideration. Some typical examples of their usages are servo-motor amplifiers, bi-stable flip flops, and second harmonic detectors.

The purpose of this article is to present some theory and application for utilizing the rectangular hysteresis characteristics of magnetic amplifiers as analog computer components for function generation. The method of determining the linearity of the core materials and some results obtained are presented. The stability of these components over extreme temperature ranges is examined, and some new magnetic amplifier circuits and their applications are presented.

THEORY

A cursory analysis of the parallel-connected magnetic amplifier, depicted in Fig. 1, will serve as the basis for the fundamental concepts to appear later in this article. There are two general cases of equal importance to be considered that are intimately related in the mechanics of operation but differ greatly in the field of application.



(a) (b)

Fig. 1—(a) Parallel-connected magnetic amplifier with resistive load, and (b) core material transfer characteristics.

Case I: $E_s(t)$ is supplied by a sinusoidal voltage generator, with negligible internal impedance, having a peak amplitude of $E_{s_{\max}}$. The following conditions, for this case, are stipulated to be absolutely true for all periods of time.

1. $$E_{s_{\max}} \leq \frac{2B_{\text{sat}}A\pi N_{ac}}{T_s\,10^8},$$

i.e., the magnetic amplifier is not saturated by the supply voltage.

2. $$I_m R_L \ll E_{s_{\max}},$$

where

$$I_m = \frac{\sqrt{2}\,H_cL}{4\pi N_{ac}},$$

meaning that the coercive force (H_c) of the core materials, such as deltamax, permalloy, or supermalloy, is small, and that the number of ac turns (N_{ac}) is large enough to insure that the reactor impedance is much greater than the load resistance with no dc in the control winding.

---

* Decimal classification: 538×621.375.2. Original manuscript received by the Institute, June 7, 1953.

† Research engineer, Benson-Lehner Corp., Los Angeles, Calif.

3. The transfer characteristics of the core material, depicted in Fig. 1(b), are valid and unchanging; further,

$$\frac{dB}{dH} = \mu, \quad \text{and} \quad \begin{array}{l} \mu \to 0 \ \text{ when } H > H_c. \\ \mu \to \infty \ \text{ when } H < H_c. \end{array}$$

4. Ampere's Law is valid and may be expressed as:

$$I_{dc}N_{dc} = I_{ave}N_{ac},$$

and I_{ave} does not contain the component I_m defined above.

In Fig. 2 (a), (b), and (c), the wave forms of the load voltage, $E_L(t)$, of the circuit of Fig. 1(a) are shown for the respective conditions of no signal current in the control winding, one-half the full-scale signal current, and full-scale signal current. The average voltage across the load resistor is a measure of the average current in the ac circuit.

$$I_{ave} = \frac{2}{R_L T_s}\int_0^{T/2} E_L(t)dt = \frac{2}{R_L T_s}\int_{t_\beta}^{T/2} E_s(t)dt, \qquad (1)$$

from condition 4 above

$$\frac{T_s I_{dc} N_{dc} R_L}{2N_{ac}} = \int_{t_\beta}^{T/2} E_{s_{max}} \sin \omega t d(\omega t)$$

$$= \frac{E_{s_{max}}}{\omega}[1 + \cos \omega t_\beta]$$

$$1 + \cos \omega t_\beta = \frac{I_{dc}N_{dc}R_L\pi}{N_{ac}E_{s_{max}}};$$

hence

$$t_\beta = \frac{T_s}{2\pi}\cos^{-1}\left[\frac{I_{dc}N_{dc}R_L\pi}{N_{ac}E_{s_{max}}} - 1\right]. \qquad (2)$$

Equation (2) shows that the firing time is related to the control current in a cosinusoidal manner and that the peak amplitude of the leading edge of the load voltage ($E_L(t)$ when $t = t_\beta$) has a corresponding cosinusoidal variation. The load voltage will be referred to hereafter as the gate. Since both the gate and firing time have implicit relations with the equation representing the generator-voltage waveform (1) it is possible to set down their desired characteristics and by induction stipulate the conditions for Case II to realize these characteristics.

Function characteristics:

a. The firing time shall be a linear function of the control current.

b. The peak value of the leading edge of the gate is constant and the average value shall be a linear function of the control current.

c. The function generated shall not be affected by parameter variation except in scale factor.

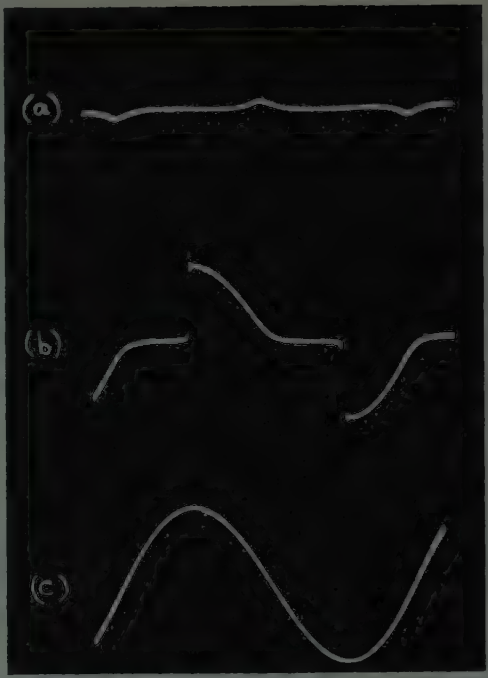


Fig. 2—Oscillograph of the load voltage waveforms for the circuit of Fig. 1 (a) where $E_s(t)$ is a sinusoidal generator. (a) Zero dc in control winding, (b) ½ full-scale control current, and (c) full-scale control current.

Case II: $E_s(t)$ is supplied by an ideal square-wave generator, with negligible internal impedance, having an average amplitude of $E_{s_{max}}$. The following conditions are stipulated to be true for all periods of time:

Conditions 1 through 4 of this case are identical to those of Case I.

5. The distributed capacity of the ac windings does not alter the magnetization current as defined in condition 2.

The circuit used for this case is the same as for the previous one, and is depicted in Fig. 1(a). The waveforms of the load voltage, as a function of the control current, are shown in the oscillograms of Fig. 3. In this figure four equal steps from zero to full-scale control current are presented.

Once again the average voltage across the load resistor determines the average current in the ac circuit.

$$I_{ave} = \frac{2}{R_L T_s}\int_0^{T/2} E_L(t)dt = \frac{2}{R_L T_s}\int_{t_\beta}^{T/2} E_{s_{max}}dt.$$

From condition 4

$$\frac{I_{dc}N_{dc}}{N_{ac}} = \frac{2E_{s_{max}}}{R_L T_s}\left[\frac{T}{2} - t_\beta\right]$$

$$t_\beta = \frac{T_s}{2}\left[1 - \frac{I_{dc}N_{dc}R_L}{N_{ac}E_{s_{max}}}\right]. \qquad (3)$$

Equation (3) shows that the desired function characteristics are realizable since the frequency and the amplitude of the supply voltage may be held to close tolerances as well as the turns ratio of the magnetic amplifier and the value of the load resistance.

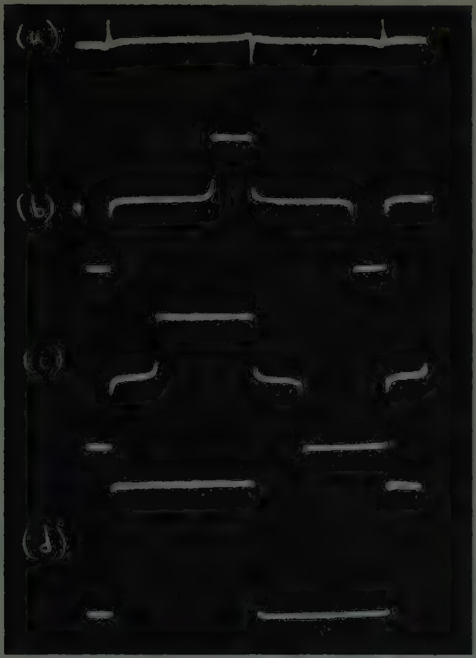


Fig. 3—Oscillograph of the load voltage waveforms for the circuit of Fig. 1 (a) where $E_s(t)$ is a square-wave generator. (a) Zero dc in control winding, (b) $\frac{1}{3}$ full-scale control current, (c) $\frac{2}{3}$ full-scale control current and (d) full-scale control current.

Core Linearity Test Procedure

The fundamental purpose of the experimental investigation was to determine what limitations the core materials of the magnetic amplifiers imposed on realizing the results anticipated from (3). Since most analog computers are limited to accuracies of the order of 0.1 per cent from practical considerations, it was felt that holding all parameters to this tolerance would suffice for the initial tests. Any appreciable deviation of the desired characteristics from the tolerance limit could then be attributed to departure from the conditions stated in Case II. The block diagram of Fig. 4 shows the manner in which the equipment was used to make the desired measurements.

The oscillator section of the frequency divider is driven by a DT cut 324.0 KC crystal. The measured temperature coefficient of this crystal, over the ambient temperature range, was better than 20 parts in a million per degree centigrade. The output of Ring 1 was the crystal frequency divided by a factor of 30, and the output of Ring 2 was the frequency of Ring 1 divided by a factor of 27. The frequency stability of the outputs from Rings 1 and 2 was as good as that from the oscillator section by virtue of the circuitry and components employed. The phase stability of these outputs was dependent upon the regulation of the bias supply for the Class C amplifiers in the Rings, and this regulation was held at about 0.1 per cent. The drift in the bias supply caused phase modulation of the lower frequencies. However, for most runs the phase-drift rate was only a few degrees per hour and was then considered negligible. The stability of the dividers, both in frequency and phase, was constantly monitored by observing their Lissajou patterns on a dual-beam scope.

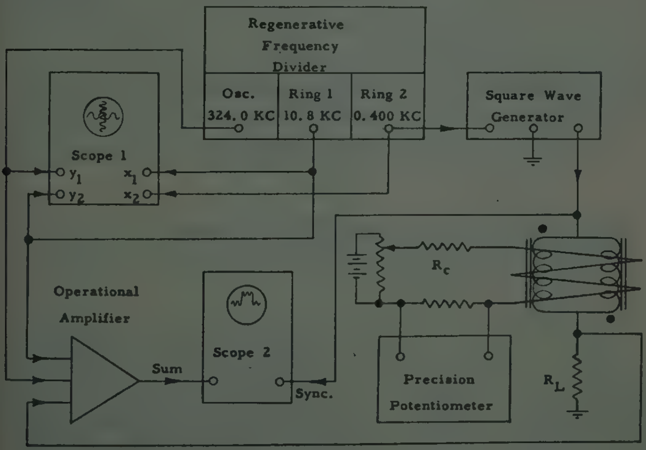


Fig. 4—Block diagram of the system employed to make the core linearity measurements.

The output of the square-wave generator was derived from the precision 400-cycle signal from Ring 2. The square wave was obtained by switching a current, regulated to 0.1 per cent, to alternate halves of a 12AT7 on corresponding half periods of the 400-cycle signal. The output impedance of the generator was less than 0.1 ohm for load impedances of 1,000 ohms or greater, and was then considered negligible.

The dc control current, of the magnetic amplifier, was measured to an accuracy of greater than 0.02 per cent by a calibrated precision potentiometer.

A fractional part of the load voltage, the output of Ring 1, and the output of the oscillator section of the divider, were fed into a summing amplifier. These voltage waveforms, including the sum, are shown in the oscillograph of Fig. 5(a) through (d) respectively.

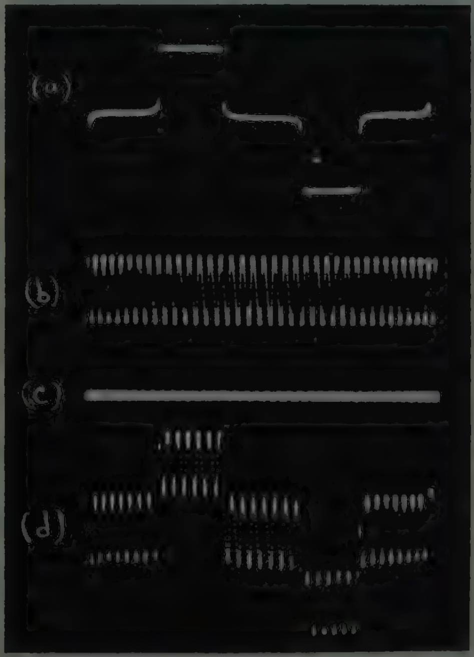


Fig. 5—Oscillogram of the input and output voltages of the summing amplifier in Fig. 4. (a) Load voltage, (b) Ring 1 marker voltage, (c) oscillator marker voltage, and (d) sum of the load, Ring 1 marker, and oscillator voltages.

MEASUREMENTS

Since the voltages from the oscillator section and the output of Ring 1 of the divider may be considered as harmonics of the square-wave generator, it follows that they provide accurate time markers for the load voltage. The generator period was divided into 27 parts by the output of Ring 1, which in turn was divided into 30 parts by the output of the oscillator section of the divider. This provided 13.5 check points for the positive (or negative) half-cycle of the load voltage with an accuracy of 0.12 per cent. The oscillographs of Fig. 6 show the manner in which the time markers were positioned with respect to the load voltage for three of the pulse-width measurements.

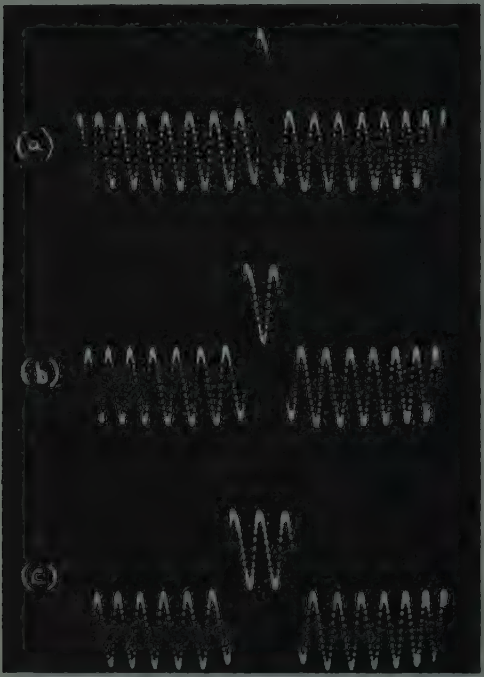


Fig. 6—Oscillograms depicting the pulse-width measuring technique employed. (a) 1/13.5 full-scale pulse width, (b) 2/13.5 full-scale pulse width, and (c) 3/13.5 full-scale pulse width.

Measurements were made to check (3) by obtaining the pulse width as a function of the control current. All parameters were varied for different runs, except $T_s/2$, and in addition temperature runs ranging from −40°C to 85°C were conducted. A summation of some data collected appears in Table I, and is indicative of the results obtained from the measurements.

It should be noted that the values of linearity obtained from the measurements were primarily restricted by the accuracy of the pulse-width measuring equipment. An interesting result obtained is that extreme temperature variations caused a slight change in scale factor (for most cases less than 0.75 per cent). Another effect that can be seen from the compilation of Table I is the reduction in the range of linearity at very low temperatures.

TABLE I

$E_{s_{\max}}$ (volts)	R_L (ohms)	T_c (°C)	Linearity (% of full scale)	Linearity Range (% of full pulse)
50.4	10K	25	0.12	89.0
50.4	15K	25	0.12	83.5
50.4	20K	25	0.12	81.5
28.8	10K	85	0.12	81.5
28.8	10K	25	0.12	81.5
28.8	10K	−43	0.12	63.0
39.6	10K	85	0.12	89.0
39.6	10K	25	0.12	89.0
39.6	10K	−43	0.12	70.5
55.8	10K	85	0.12	89.0
55.8	10K	25	0.12	89.0
55.8	10K	−43	0.12	85.0
61.2	10K	85	0.12	89.0
61.2	10K	25	0.12	89.0
61.2	10K	−43	0.12	89.0

A typical family of curves relating the pulse width to the control current is shown in Fig. 7. The parameter varied in collecting the data for these cures was $E_{s_{\max}}$. The only appreciable effect observed in varying this parameter was in scale factor.

An examination of the data collected clearly indicates that the best results were obtained when the cores made a full flux excursion, i.e., when

$$E_{s_{\max}} = \frac{2B_{\text{sat}}A\pi N_{ac}}{T_s 10^8}.$$

In the event that the cores do not make a full flux excursion (reduced $E_{s_{\max}}$) the range of linearity is reduced. On the other hand, if the cores exceed their full flux excursion, which means that they go into ac saturation, a voltage pulse appears across the load resistor with no control current flowing in the dc winding. When this case arises control is not exhibited until,

$$I_{dc}N_{dc} = I_{ave}N_{ac}.$$

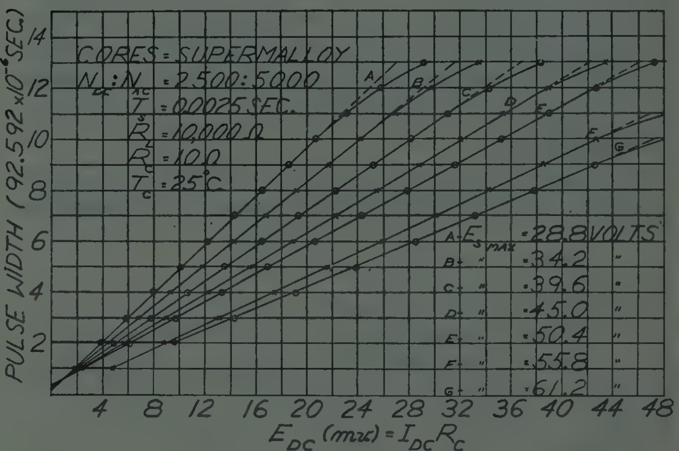


Fig. 7—Pulse width as a function of control current with the generator voltage as the varied parameter.

The parameter varied to obtain the family of curves shown in Fig. 8 was R_L. Again the greatest effect noted in parameter variation was in scale factor. However, it can be seen from Table I that the range of linearity increased as the value of R_L decreased. This is easily confirmed by realizing that the load current varies inversely as the load resistance making the effect of nonlinearity because of magnitization current of less importance for large values of load current.

Although the curves shown in Figs. 7 and 8 do not pass through the origin, it should be explained that this was primarily for the convenience of making the measurements and if the data were normalized the curves would have intercepts at the origin. The major factor causing the curves to deviate from a common zero intercept was the previously mentioned phase drift.

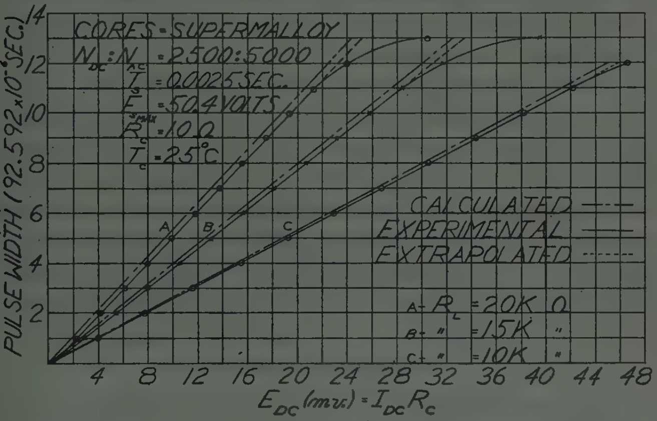


Fig. 8—Pulse width as a function of control current with the load resistance as the varied parameter.

Circuitry for Function Generation

The fundamental circuit from which the function generators will be developed was shown in Fig. 1(a). It has been demonstrated that the load voltage of the magnetic amplifier is a gate whose width is directly proportional to the control current if the conditions of Case II are observed.

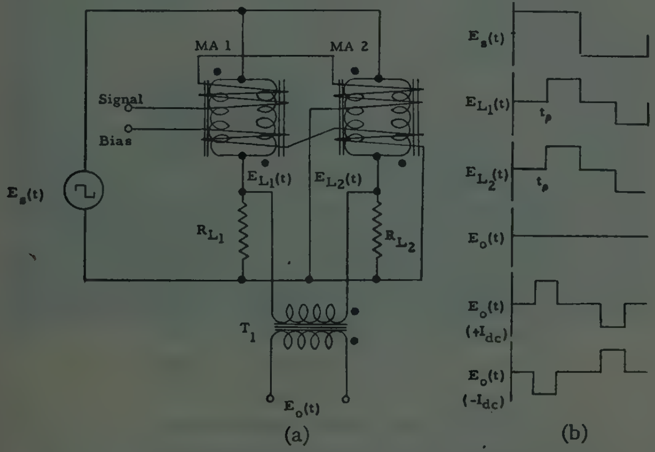


Fig. 9—Phase sensitive pulse width or pulse position generator circuitry and resulting waveforms.

The circuit of Fig. 9(a) shows how two magnetic amplifiers, their respective load resistors, a square-wave generator, and an output transformer may be connected to generate a phase-sensitive pulse-width function, or a pulse-position function.

For this circuit magnetic amplifiers 1 and 2 have their bias windings connected in series. The magnitude of the bias current is such that the cores of both mag-amps support their common supply voltage until $t=t_\beta$. Since both amplifiers are postulated to be identical in core characteristics and number of turns per winding, the firing times of the amplifiers are coincident and the voltage across the transformer (T_1) is zero. The signal windings of these amplifiers are seriately connected in push-pull. Therefore a signal current flowing in the control windings pushes one amplifier further into saturation and pulls the other out of saturation by the same amount. Since the primary winding of the transformer is connected to add the load voltages of the mag-amps, the secondary winding of the transformer has across it a phase-sensitive pulse with a gain of 2, with respect to either load voltage, for unity turns ratio in the transformer. If the signal current is held constant at some given value and the bias current is varied, the pulse position with respect to the generator voltage will vary directly as the bias current. From the above considerations it is seen that the circuit described can perform as a linear pulse-width modulator, a linear pulse-position generator, or both concurrently.

The circuit, shown in Fig. 10(a), is one for which more direct application to computer usage may be found. This diagram shows a parallel-connected magnetic amplifier with an additional ac winding on one core. This winding is phased such that, when the cores are unsaturated and acting as a low-loss transformer, the voltage across its terminals is derived from a generator supply a voltage equal in magnitude to that of the square-wave generator, but with a 180° phase reversal and an internal impedance equal to the load resistance. One terminal of this winding is connected between the mag-amp and its load resistance. The other terminal has, between it and the generator ground, the load voltage minus the reactor voltage. This is the output voltage $E_0(t)$.

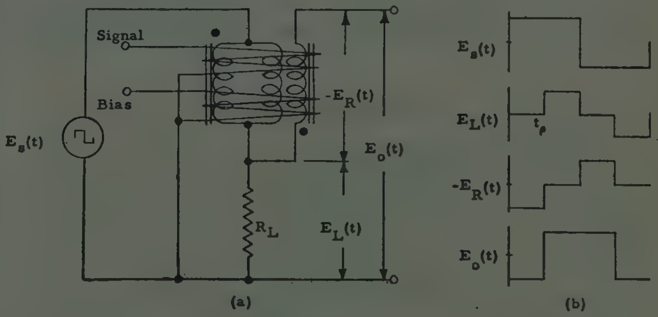


Fig. 10—Square-wave phase shifter and resulting waveforms.

The current in the bias winding is adjusted such that $t_\beta = T_s/4$. For these conditions the output voltage is then a square wave in quadrature with the supply voltage [Fig. 10(b)]. The phase angle of the output voltage can now be varied linearly, from quadrature, with the control current. Whether this phase angle is lead or lag, from the initial quadrature, depends upon the sign of the control current. Hence the circuit described functions as a linear square-wave phase shifter.

The application of some of the above described circuits in the field of computers is not too difficult to visualize. Either the pulse width generator or the pulse position generator could become an integral part of an analog to digital converter. The utilization of the phase shifter in an amplitude modulated dc multiplier is not too different from the systems to be investigated as suggested by Korn.[1] The block diagram of Fig. 11 shows one method of dc multiplication where the phase shifter is used as the demodulator, hence the multiplier, and the amplitude modulator provides the multiplicand. This type of multiplier was built and tests showed that product accuracies of the order of less than 3.0 per cent could easily be achieved without the use of high-precision components or overly careful design techniques.

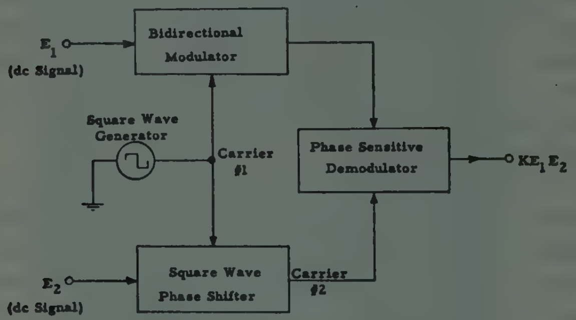


Fig 11—Block diagram of dc multiplier employing the phase shifter as the demodulator carrier.

CONCLUSIONS

A review of the data collected clearly shows that the linearity of the magnetic amplifiers with toroidal supermalloy cores was as good as the pulse-width measuring equipment used in collecting the data. Some tests run on amplifiers with toroidal deltamax cores revealed pronounced nonlinearities by comparison.

The nonlinearities of the deltamax cores can be attributed to a deviation from condition 4 of Case II, i.e.,

$$I_{dc}N_{dc} \neq I_{ave}N_{ac}.$$

The correct expression is

$$I_{dc}N_{dc} = I_{ave}N_{ac} + \epsilon,$$

when

$$I_{dc} = 0$$

$$\epsilon = -I_{ave}N_{ac}.$$

Since the load current is the magnetization current for this condition, I_{ave} must include both components, hence

$$I_{dc}N_{dc} = N_{ac}\left[-\frac{2}{T}\int_{s}^{T/2} I_m dt - \frac{2}{T}\int_{t}^{T/2} I_{ave} dt\right].$$

Since the magnetization current is a function of the coercive force of the core material, and H_c for deltamax is about an order of magnitude greater than that of supermalloy, it follows that the nonlinearities observed were to be expected.

The fact that the amplifiers displayed no adverse effects when subjected to extreme temperature variations increases their usefulness as components for computers that by necessity cannot operate continually in a controlled environment. The only precautions that need be taken with these components are that their range of linearity is not exceeded for the most extreme condition, and a reference mag-amp be supplied for automatic scale-factor adjustment.

In designing these components for computer or any type of closed-loop application, response-time considerations cannot be overlooked. Since this article does not include design criteria, other than the selection of the proper core materials, let it suffice to say that response times substantially better than those of the best servomotors are easily achieved by the choice of the proper carrier frequency and other design considerations.

ACKNOWLEDGMENT

The author wishes to express his gratitude to M. E. Mohr, head of the Computer Research and Development Department, and J. E. Richardson, research physicist, both of the Hughes Aircraft Company Research and Development Laboratories, for their invaluable aid and guidance without which this material could not have been presented. Appreciation is also expressed to the U. S. Air Force for permission to release this information.

DEFINITION OF SYMBOLS

$E_s(t)$ = generator voltage (volts)

$E_L(t)$ = load voltage (volts)

$E_R(t)$ = reactor voltage (volts)

$E_{s_{max}}$ = peak generator voltage (volts)

ϕ = magnetic flux (gauss-cm^2)

B = magnetic-flux density (gauss)

B_{sat} = saturation level of magnetic-flux density (gauss)

H = magnetizing force (oersteds)

H_c = coercive force (oersteds)

A = area of core cross-section (cm^2)

I_m = magnetization current (amperes)

L = length of magnetic path (cm)

N_{ac} = number of turns in ac winding

N_{dc} = number of turns in dc winding

I_{ave} = average value of load current (amperes)

I_{dc} = dc control current (amperes)

R_L = load resistance (ohms)

T_s = generator voltage period (seconds/cycle)

t_β = time (seconds), with respect to the generator period, at which the cores reach B_{sat}

T_c = temperature (degrees centigrade)

---

[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y.; 1952.

An Input-Output Unit for Analog Computers[*]

P. R. VANCE[†], AND D. L. HAAS[†]

***Summary*—An instrument servomechanism that can be used either as an *X-Y* recorder or as a curve-follower type of function generator is described. The theory of operation is discussed, and a typical example of the instrument's use as a function generator is presented.**

INTRODUCTION

THE DEVICE described here, and pictured in Fig. 1, is intended primarily for use with analog computers as an input-output unit. When used as an input unit, the instrument is intended to supplement other nonlinear analog-computing equipment, providing a versatile low-frequency function generator.[1] When used as an output unit, the instrument is essentially an X-Y recorder and provides a convenient means of directly plotting one voltage against another. It is particularly applicable to problems requiring complicated forcing functions or variable coefficients. Measured data, obtained by using the instrument as a recorder, can be introduced into an analog-computer problem by use of a playback feature in the instrument.

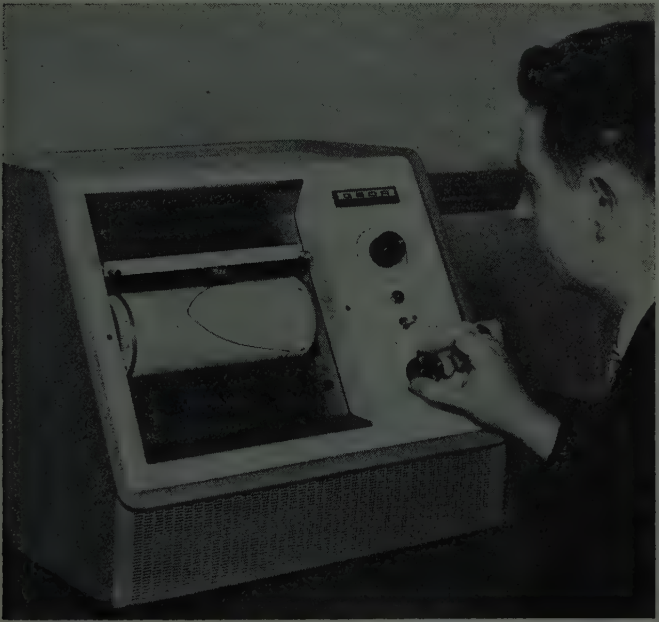


Fig. 1—Input-output unit.

THEORY OF OPERATION

The basic instrument consists of two positional servomechanisms. One servomechanism controls the peripheral displacement, X, of a cylindrical drum, which carries a sheet of $8\frac{1}{2}$-inch by 11-inch graph paper. The other servomechanism controls the lateral displacement, Y, of a carriage, to which either a pen or a potentiometer-type transducer can be attached. The drum has a peripheral velocity limit of 10 inches per second, and the carriage has a lateral velocity limit of 7 inches per second.

When the instrument is used as a recorder, the X and Y displacements are proportional to the voltages applied to the drum and pen input terminals, respectively. A pen, placed in the carriage, plots the function to be recorded on the paper carried by the drum. Either a ball point or capillary-type pen can be used. The capillary pen records a function with special conducting ink so that it can be played back later by using the instrument as a function generator. The drum and pen scale factors are adjustable in 10 calibrated steps, between 0.50 mv per inch and 10 v per inch. The static accuracies of both the drum and the pen are within 0.2 per cent of full scale.

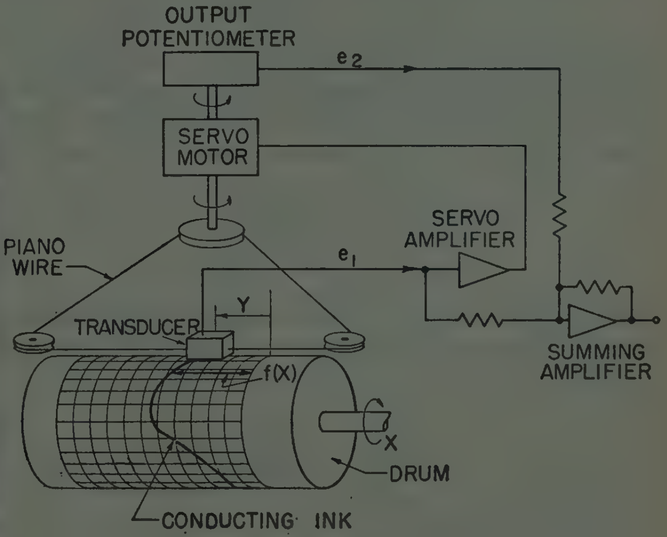


Fig. 2—Simplified schematic of curve-follower system.

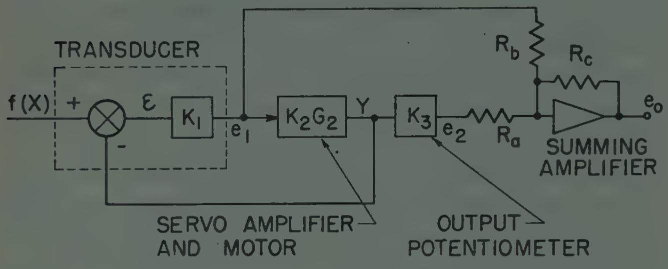
When the instrument is to be operated as a function generator, the Y servomechanism is converted to a curve follower by attaching the transducer to the carriage, as shown in Fig. 2. The function to be generated, $f(X)$, is plotted with conducting ink or a soft lead pencil and attached to the drum. The transducer makes electrical contact with the curve and provides the Y servomechanism with the error voltage required to follow the curve as the drum is positioned by the X servomechanism. An output potentiometer coupled to the carriage provides a voltage proportional to the Y displacement. Errors in following the curve, due to the dynamic limitations of the Y servomechanism, are minimized by the addition of transducer and output-potentiometer voltages in a summing amplifier. The output of the summing amplifier is proportional to $f(X)$. The abscissa scale factor is adjustable between 0.50 mv per inch and 10 v per inch. The ordinate scale factor is fixed at 10 v per inch. Static accuracies within 0.2 per cent of full scale have been measured.

---

[*] Decimal classification: 621.375.2×R365.3. Original manuscript received by the Institute, May 11, 1953.

[†] Aerophysics Departments, Goodyear Aircraft Corporation, Akron, Ohio.

[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 245–287; 1952.



f(X) = FUNCTION TO BE GENERATED IN INCHES
Y = DISPLACEMENT OF TRANSDUCER IN INCHES
X = DISPLACEMENT OF DRUM SURFACE IN INCHES
e_1 = OUTPUT OF TRANSDUCER IN VOLTS
e_2 = OUTPUT POTENTIOMETER VOLTAGE
e_o = OUTPUT OF SUMMING AMPLIFIER IN VOLTS
ε = TRACKING ERROR IN INCHES

Fig. 3—Block diagram of curve-follower system.

A block diagram of the curve-following system is shown in Fig. 3. The transducer, servo amplifier, and motor comprise a positional servomechanism, which tends to position the transducer so that Y is equal to $f(X)$:

$$\frac{Y}{f(X)}(S) = \frac{K_1K_2G_2(S)}{1 + K_1K_2G_2(S)}. \qquad (1)$$

The output of the summing amplifier is proportional to the sum of the transducer and output-potentiometer voltages:

$$e_o = -\left(\frac{R_c}{R_a}\right)e_2 - \left(\frac{R_c}{R_b}\right)e_1 \text{ volts,} \qquad (2)$$

where

$$e_1 = K_1[f(X) - Y] \text{ v, and} \qquad (3)$$

$$e_2 = K_3Y \text{ v.} \qquad (4)$$

Equations (2), (3), and (4) are solved for e_o in terms of Y and $f(X)$:

$$e_o = -\left(\frac{R_c}{R_a}\right)K_3Y - \left(\frac{R_c}{R_b}\right)K_1f(X) + \left(\frac{R_c}{R_b}\right)K_1Y \text{ volts.} \qquad (5)$$

The parameters, R_a, R_b, R_c, K_1, and K_3, are adjusted so that the first and last terms in (5) cancel each other, making the output of the summing amplifier proportional to $f(X)$ within the linearity limitations of the transducer, regardless of the tracking error. Therefore, the only limitation that needs to be placed upon $f(X)$ is that it must not require a tracking error that exceeds the range of the transducer.

The transducer consists of a printed circuit potentiometer card and pickoff card as shown in Fig. 4. The potentiometer card, as shown in Fig. 5, consists of 100 evenly spaced nickel fingers across which a resistance element is painted.

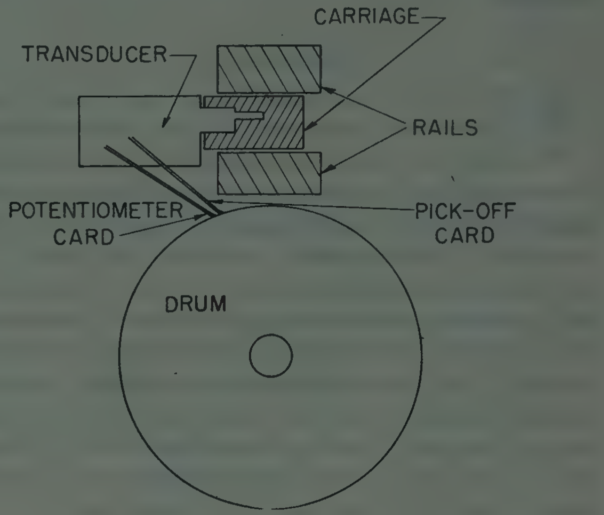


Fig. 4—Side view of transducer.

The pickoff card is identical to the potentiometer card except that the resistance element is replaced by a nickel shorting bar. Both cards ride on the surface of the drum and the nickel fingers make electrical contact with the curve, $f(X)$. Equal voltages of opposite polarity are supplied to the two ends of the resistance element. The error voltage, applied to the conducting curve by the potentiometer card, is proportional to the displacement between the curve and the center of the card. The pickoff card feeds this error voltage to the Y servo-amplifier input and to one input of the summing amplifier. Since the active width of the potentiometer card is one inch, it can maintain electrical contact with the conducting curve only if the tracking error does not exceed one-half inch.

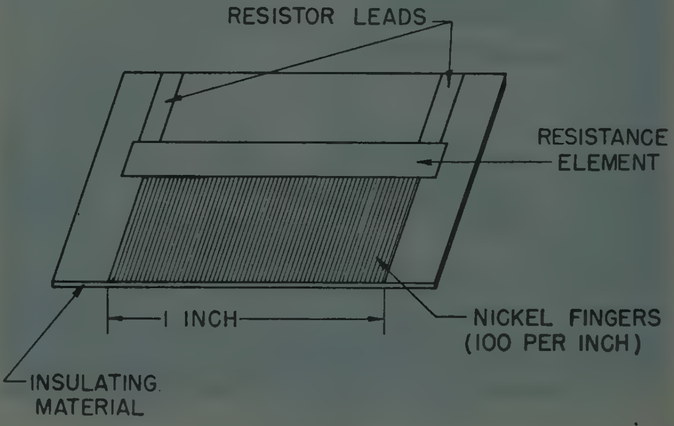


Fig. 5—Bottom view of potentiometer card.

Adding the transducer and output-potentiometer voltages produces an effect described in (2) through (5). This effect was illustrated in the laboratory by plotting a series of one-fourth-inch step functions and attaching them to the drum. The output voltages of the transducer, output potentiometer, and summing amplifier were recorded as the drum was driven at a constant velocity. From recorded voltages, (Fig. 6), it is apparent that voltage components corresponding to rapid fluctuations in $f(X)$ are supplied to the summing amplifier by the transducer while more slowly varying components of $f(X)$ are supplied by the output potentiometer.

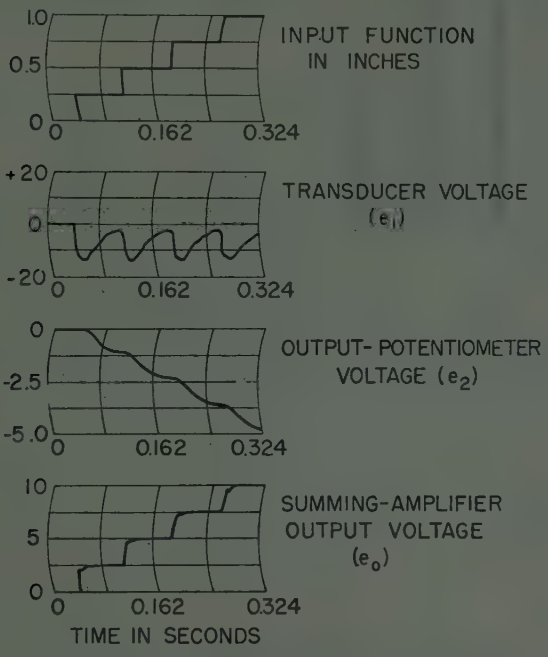


Fig. 6—Step-function response of curve follower.

APPLICATIONS

A representative application of the input-output unit described is found in the determination of the amplitude spectrum of a periodic function.[2] If $f(t)$ is a periodic function whose period is T, and if the Fourier series expansion exists, then $f(t)$ can be expressed as:[3]

$$f(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty}\left[a_n \cos\left(\frac{2\pi n}{T}t\right) + b_n \sin\left(\frac{2\pi n}{T}t\right)\right], \qquad (6)$$

where

$$\frac{a_o}{2} = \frac{1}{T}\int_0^T f(t)dt, \qquad (7)$$

$$a_n = \frac{2}{T}\int_0^T f(t)\cos\left(\frac{2\pi n}{T}t\right)dt, \text{ and} \qquad (8)$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin\left(\frac{2\pi n}{T}t\right)dt. \qquad (9)$$

The amplitude coefficients, $a_o/2$, a_n, and b_n, can be determined from an analog-computer solution of (7), (8), and (9), respectively.

One computer method of solution for the amplitude coefficients is shown in Fig. 7. An input-output unit is used to generate a voltage proportional to $f(t)$, and a sin-cos generator furnishes a voltage proportional to either cos $[(2\pi n/T)t]$ or sin $[(2\pi n/T)t]$. An electronic multiplier provides a voltage proportional to the product $f(t)$ cos $[(2\pi n/T)t]$ or $f(t)$ sin $[2\pi n/T)t]$, and an integrator, operating between the limits $t=0$ and $t=T$, completes the required operation. The integrator output corresponds to either a_n or b_n, depending upon whether the sin-cos generator is adjusted to generate a cos function or a sin function. The constant term $a_o/2$ is determined by feeding the voltage from the input-output unit directly to the integrator, and integrating from $t=0$ to $t=T$.

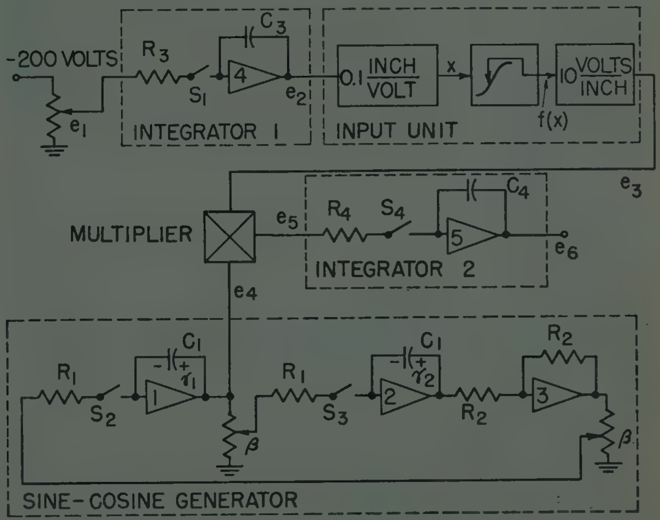


Fig. 7—Computer setup for Fourier series expansion.

The components shown in Fig. 7, other than the input-output unit, are all standard units of a general-purpose electronic differential analyzer, and interconnections between units are made through a removable problem board. The switches, S_1, S_2, S_3, and S_4, make it possible to apply initial-condition voltages to the amplifier feedback capacitors, and to hold these voltages until the problem is started. The switches operate simultaneously, providing a convenient means of starting and stopping the problem. Problem time, t, is measured from the instant of closure of the switches, and integration from $t=0$ to $t=T$ is accomplished by holding the switches closed for T secs.

In this example, $f(t)$ is a rectified sin wave, one period of which is shown in Fig. 8. The input-output unit uses the curve $f(t)$, plotted with a scale factor of 1.0 inch per second for the abscissa and 0.10 inch per v for the ordinate, to generate:

---

[2] L. Pode, "Some REAC techniques employed at the David Taylor Model Basin," Project Cyclone Symposium II, Reeves Instrument Corp., New York, N. Y., pp. 25–30; 1952.

[3] C. Louis Cuccia, "Harmonics, Sidebands and Transients in Communication Engineering," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 33–34; 1952.

$$e_3 = 10f(t) \text{ volts.} \tag{10}$$

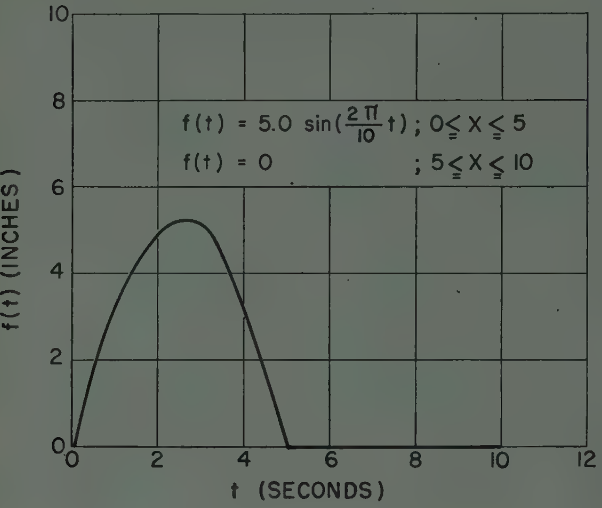


Fig. 8—Rectified sin wave.

Integrator 1 provides the proper drum-positioning voltage, e_2, to drive the drum at a rate of 1.0 inch per second.

The voltage e_4 is either a sin or a cos function, depending upon the initial-condition voltages γ_1 and γ_2 applied to the feedback capacitors of amplifiers 1 and 2, respectively. Specifically,

$$e_4 = 100 \cos \omega t \text{ volts } (\gamma_1 = +100 \text{ volts}; \gamma_2 = 0), \text{ and} \tag{11}$$

$$e_4 = 100 \sin \omega t \text{ volts } (\gamma_1 = 0; \gamma_2 = +100 \text{ volts}). \tag{12}$$

Frequency, ω, is determined by the parameters β, R, and C, which are adjusted so that ω corresponds to the appropriate harmonic of $f(t)$:

$$\omega = \frac{\beta}{R_1C_1} = \frac{2\pi n}{10} \text{ radians per sec } (n = 1, 2, 3, \cdots). \tag{13}$$

Integrator 2 is driven by the output voltage of the multiplier e_5, which is proportional to the product of e_3 and e_4. The values of the input resistance R_4 and feedback capacitance C_4 are chosen so that

$$e_{6a} = -10\int_0^{10} f(t) \cos\left(\frac{2\pi n}{10} t\right) dt \text{ volts}$$
$$(\gamma_1 = +100 \text{ volts}; \gamma_2 = 0), \tag{14}$$

and

$$e_{6b} = -10\int_0^{10} f(t) \sin\left(\frac{2\pi n}{10} t\right) dt \text{ volts}$$
$$(\gamma_1 = 0; \gamma_2 = +100 \text{ volts}). \tag{15}$$

In this particular example, the function $f(t)$ is zero for all values of t between 5 and 10 sec., and the switches can be opened at any time during this interval without affecting the voltages e_{6a} and e_{6b}.

A comparison of (14) and (15) with (8) and (9) shows that the amplitude coefficients, a_n and b_n, are proportional to the output of integrator 2:

$$a_n = \frac{-e_{6a}}{50} \text{ inches, and} \tag{16}$$

$$b_n = \frac{-e_{6b}}{50} \text{ inches.} \tag{17}$$

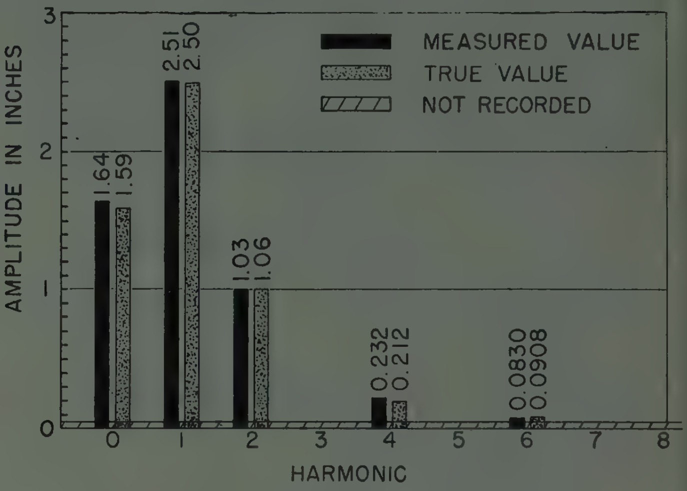


Fig. 9—Amplitude spectrum of rectified sin wave.

If the voltage e_3 is applied directly to the input of integrator 2, the output is given by

$$e_{6o} = -10\int_0^{10} f(t)dt \text{ volts.} \tag{18}$$

Comparison of (18) and (7) shows that

$$\frac{a_o}{2} = \frac{-e_{6o}}{100} \text{ inches.} \tag{19}$$

The computer solution for the amplitude spectrum, of the function described in Fig. 8, is plotted in Fig. 9. Harmonic amplitudes smaller than 0.05 inch were neglected, as indicated by the cross-hatched portion of the graph. The maximum difference between the true and measured amplitudes of any of the harmonics is less than 0.05 inch, or less than 1 per cent of the amplitude of the rectified sin wave.

Other applications are found in computer studies of guided missiles or aircraft. The instrument can be used as a recorder to provide a convenient means of plotting missile trajectories in two coordinates. As a function generator it can be used in aerodynamic studies to generate the conversion factor as a function of altitude, between Mach number and velocity. In computer studies of autopilots, the device can be used to generate forcing functions representing realistic stick and pedal motions. Another application is found in computer studies of internal combustion engines in which the device can be used to generate the lift versus stroke characteristics of cams.[4] This list of applications is by no means a comprehensive one, and is given only as an indication of the utility of the instrument.

---

[4] C. D. Morrill and R. V. Baum, "Diode limiters simulate mechanical phenomena," *Electronics*, vol. 25, no. 11, pp. 122–126; November, 1952.

Application of Electronic Differential Analyzers to Engineering Problems

C. A. MENELEY†, SENIOR MEMBER, IRE, AND C. D. MORRILL†, MEMBER, IRE

Summary—**The basic elements comprising an electronic differential analyzer are described. Fundamental concepts employed in the application of electronic differential analyzers to engineering problems are discussed, and an effective method of studying complicated dynamic systems is demonstrated. Data are presented on the types of problems which such machines are known to be capable of solving and on the extent to which they are being used in research, development and industrial organizations.**

INTRODUCTION

THE TERM ELECTRONIC differential analyzer is a general one usually used to include the general-purpose analog computer, the special-purpose analog computer employing integration, the simulator, and the differential analyzer using digital methods. The scope of this paper is limited to electronic differential analyzers employing analog techniques.

A general-purpose electronic differential analyzer contains electronic and electromechanical computing elements arranged for convenient interconnection in the solution of ordinary differential equations representing dynamic physical systems. A representative analyzer, capable of studying a system having six degrees of freedom, is shown in Fig. 1. This analyzer is six feet high and consumes one kilowatt of power. It is an independent unit containing power supplies and a removable prepatch board.

LINEAR COMPUTING ELEMENTS

The basic and most versatile element in most electronic differential analyzers[1–3] is the direct-coupled amplifier. This amplifier, shown schematically in Fig. 2A, must meet the following important requirements.[4]

1. Since variables are represented as voltages, the amplifier must be able to generate voltages of either polarity so that its output voltage may represent variables of either sign.

2. The amplifier must provide an output of opposite sign from the input so that negative feedback can be used.

3. The amplifier must have high gain and low phase shift at all frequencies within the range of the problems to be studied, and should have a good margin of stability when a large portion of negative feedback is used. The usual gain ranges from 50,000 to about 500,000 at low frequencies. The tolerable phase shift depends upon the gain at zero frequency; e.g., for an amplifier that has been provided with sufficient negative feedback to reduce the gain at zero frequency to unity, the phase shift at low frequencies may range between 0.001 and 0.01 degree per cycle per second. High gain contributes to the static accuracy of the analyzer and reduces dependence on vacuum-tube characteristics. Low phase

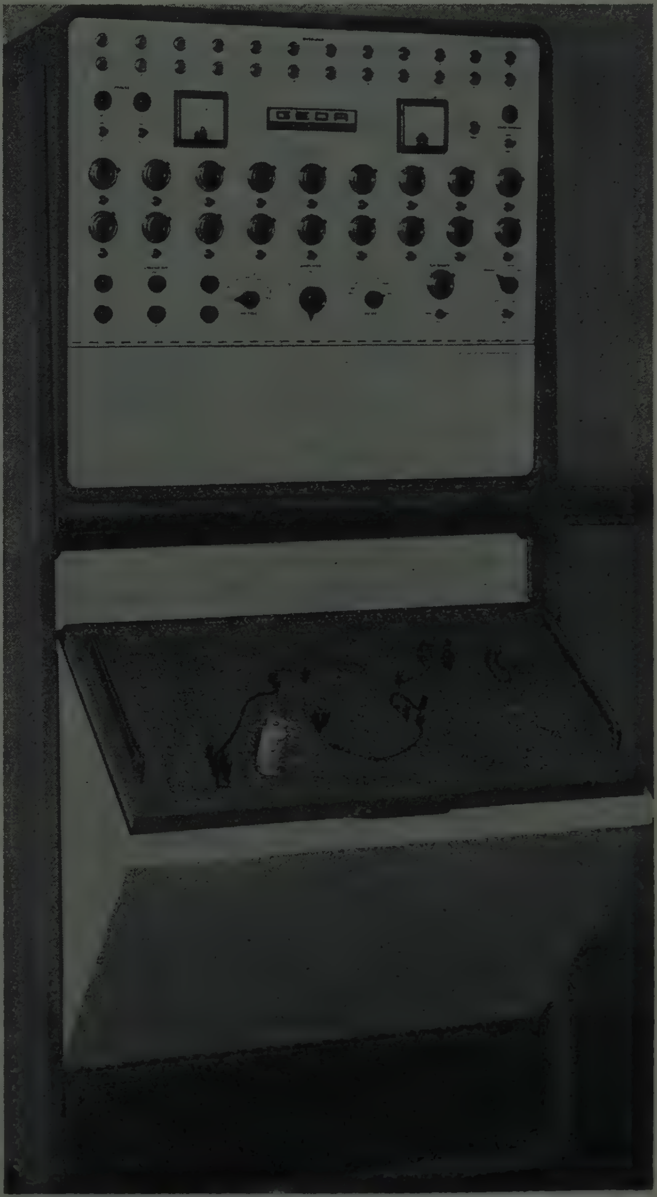


Fig. 1—Typical linear electronic differential analyzer.

---

* Decimal classification: 621.375.2. Original manuscript received by the Institute, May 11, 1953.

† Aerophysics Depts., Goodyear Aircraft Corp., Akron 15, Ohio.

[1] K. D. Swartzel, Jr., "Summing Amplifier," U. S. Patent 2,401,779; June 11, 1946.

[2] J. R. Ragazzini, R. Randall and F. A. Russell, "Analysis of problems in dynamics by electronic circuits," PROC. I.R.E., vol. 35, pp. 444–452; May, 1947.

[3] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Company, New York, N. Y.; 1952.

[4] C. A. Meneley and C. D. Morrill, "Linear analog computer design," *Proc. NEC*, vol. 5, pp. 48–63; 1949.

shift permits the study on a real time scale of systems having natural frequencies up to several hundred cycles per second.

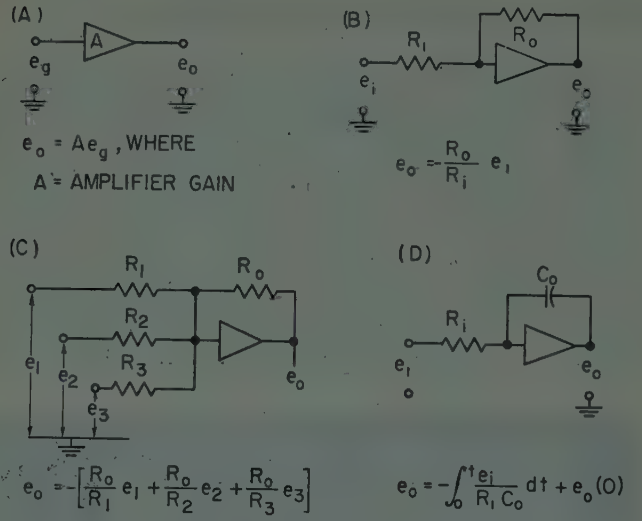

(A)
A
e_g
e_o
$e_o = Ae_g$, WHERE
A = AMPLIFIER GAIN
(B)
R_1
R_o
e_i
e_o
$e_o = -\frac{R_o}{R_i} e_1$
(C)
R_1
R_o
R_2
R_3
e_1
e_2
e_3
e_o
$e_o = -\left[\frac{R_o}{R_1} e_1 + \frac{R_o}{R_2} e_2 + \frac{R_o}{R_3} e_3\right]$
(D)
C_o
R_i
e_1
e_o
$e_o = -\int_0^t \frac{e_i}{R_1 C_o} dt + e_o(0)$

Fig. 2—Basic linear computing operations.

4. The amplifier must present a high input impedance. Since the input terminal is the grid of a vacuum tube, the grid current must be low compared with the signal current, which may be only one-tenth of a microampere. The usual grid current ranges from 10^{-9} amperes on some analyzers to 10^{-11} amperes on the better analyzers. High grid current imposes a limitation on the time duration of a computing run where integration is involved.

5. In the absence of feedback and with no signal input, the input voltage required to reduce the output to zero must be negligible.[5] An amplifier having this property is said to have low zero drift. Zero drifts range from tens of millivolts per hour in some machines to random drifts amounting to about 100 microvolts over a month's period in others. These values may be compared with signal voltage levels, which usually have full-scale limits of plus and minus 100 volts.

In the following explanation of the use of computing amplifiers in performing simple computing operations, it will be assumed that the amplifiers meet the above requirements so well that their shortcomings may be ignored.

In Fig. 2B the input voltage, e_i, applied between the input terminal and ground causes a current to flow through the resistor, R_i. If the third and fifth requirements are fully met, the voltage at the input to the amplifier must be effectively zero for all finite output voltages. Therefore, the current flowing through R_i is exactly e_i/R_i. If the amplifier itself draws no input current (the fourth requirement), this input current must flow through R_o and the amplifier must adjust its output voltage to be equal and opposite to the voltage across R_o since the terminal of R_o connected to the input grid is kept at ground potential by the high-gain amplifier. Thus, the voltage measured between the output of the amplifier and ground must be minus $e_i(R_i/R_o)$, and the input voltage has been multiplied by a constant whose value is determined by the ratio of the input and feedback resistors.

In much the same way, the amplifier may be used to sum a number of voltages. Under the conditions outlined above, the currents flowing through R_1, R_2, and R_3 of Fig. 2C are dependent only on the magnitudes of each voltage and its associated resistor. All of these currents must flow through the single resistor, R_o; if, for example, all the resistors are equal, the voltage across R_o and, therefore, the output voltage, is the sum of the input voltages.

To integrate, the feedback resistor of Fig. 2B is replaced by a capacitor (see Fig. 2D). The voltage across the capacitor, which is exactly equal to the amplifier output voltage, is proportional to the time integral of the current, e_i/R_i, through it; the proportionality constant is the inverse of the value of the capacitance. The equation for the output voltage is given in the figure; $e_o(0)$ is the voltage across the capacitor at some arbitrarily defined zero time and indicates a means of applying initial conditions in differential equations.

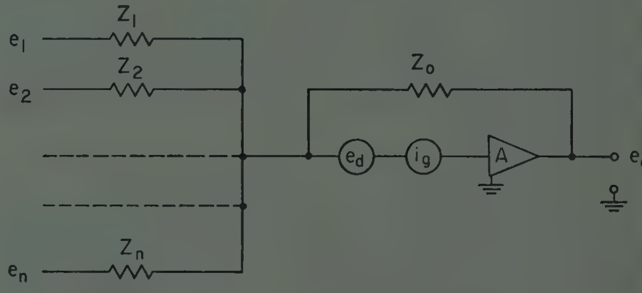


Fig. 3—Errors in summing amplifier.

It can be easily shown[4] that where several voltages are to be summed, the errors due to finite amplifier gain, grid current and drift are closely given by the following equation (see Fig. 3):

$$e_o = -Z_0\left[\frac{e_1}{Z_1} + \frac{e_2}{Z_2} + \cdots + \frac{e_n}{Z_n}\right] + Z_0(1-\beta)\left[\frac{e_1}{Z_1} + \frac{e_2}{Z_2} + \cdots + \frac{e_n}{Z_n}\right] - e_d\left[\frac{Z_0 + Z_T}{Z_T}\right]\beta - i_g Z_0 \beta, \quad (1)$$

where

$$\beta = \frac{1}{1 - \frac{Z_0}{A}\left(\frac{1}{Z_0} + \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_n}\right)},$$

$$Z_i \equiv Z_i(s),$$

---

[5] Edwin A. Goldberg, "Stabilization of wide band direct current amplifiers for zero and gain," *RCA Review*, vol. 11, pp. 296–300; June, 1950.

and

$$\frac{1}{Z_T} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_n}.$$

The first term on the right side of (1) shows the desired sum; the second term shows the error due to finite amplifier gain; third term shows error due to drift; and fourth term shows error due to grid current.

The same expressions hold for integration or for combined integration and summation if Z_0 represents the complex feedback network.

This discussion illustrates both the strength and weakness of electronic differential analyzers. Their strength is demonstrated by the fact that, with relatively simple networks and circuits, summation, integration, and change of scale and sign may be accomplished and, as will be shown, ordinary linear differential equations with constant coefficients may be solved quite easily.

Their weakness, evident from the equation of Fig. 2D, is that time is the only truly independent variable. There are certain methods of avoiding this limitation in some cases, but the methods are sometimes expensive in terms of the amount and complexity of equipment, and the process is occasionally subject to the accumulation of errors. This weakness, however, is not so serious as it may at first seem since time is at least implied in the majority of engineering problems.

NONLINEAR COMPUTING ELEMENTS

Many practical engineering problems may be satisfactorily represented by ordinary linear differential equations with constant coefficients; however, a general-purpose differential analyzer must also be able to solve linear equations with variable coefficients and nonlinear equations and must therefore include multipliers, function generators and comparators.

A multiplier is a device for obtaining the algebraic product of two variable voltages; it has two inputs, a and b, and one output, Kab, where K is usually chosen so that, when both a and b are full-scale amplitude and positive, the output is equal to both a and b. A multiplier may be either electromechanical[6] (e.g., servo-driven ganged potentiometers), or entirely electronic.[7,8] The electronic multiplier provides greater speed and extends the useful frequency range of the differential analyzer from one to three decades over the servomultiplier. The accuracies of the electronic and electromechanical multipliers are comparable, ranging from within 1 per cent to within 0.01 per cent depending upon speed and complexity; the electronic multiplier, as might be expected, is more complex, using approximately four or five times as many vacuum tubes.

The function generator in the differential analyzer occupies a position somewhat analogous to the so-called memory of a digital computer. Regular functions such as sine and cosine, or empirical data, may be stored in the function generator in the form of curves. The function generator will generally have one input, a, and one output, $f(a)$; it is available in several forms; the electromechanical units may be servo-driven curve followers, tapped, loaded, or shaped potentiometers,[9] and so forth; electronic function generators usually employ biased diodes or a masked cathode-ray tube, sometimes called a photoformer.[10] Often the particular application will indicate the preference of one type of function generator over the others. Function-generator accuracies are usually only within 1 per cent, although accuracies to within 0.1 per cent or better can sometimes be obtained.

A comparator compares two input voltages and produces an output voltage having a discontinuity at a point where the two inputs become equal in magnitude and opposite in sign. It might well be considered as a special function generator; however, it finds so many uses in this particular form that it has been given separate identity. Comparators are frequently called decision elements, logical circuits, or, sometimes, simply relays or diodes. In the usual application, a comparator combines a high-gain dc amplifier with either a relay[11] or a diode.[12] The amplifier-diode combination provides greater speed, while the amplifier-relay combination is more economical if several circuits must be switched. Comparators may be made to perform as accurately as linear computing elements; that is, to within 0.1 to 0.01 per cent. The use of comparators, multipliers, function generators and the linear elements are illustrated in *V* in the solution of a practical engineering problem.

INPUT-OUTPUT ELEMENTS

A fairly complete group of computing elements have been discussed. However, to study a dynamic system, input and output units are also needed. An input element produces a time-varying forcing or driving function; it may take many forms depending on the shape of the function required. The easiest to produce and the most commonly used is the step function, which can be generated simply by closing a switch between the problem and a calibrated voltage source. Sinusoids, exponentials, ramp functions, half sinusoids, truncated ramps and purely arbitrary forcing functions may be generated by combining the step function with certain computing elements such as integrators, function generators and comparators.

---

[6] Ivan A. Greenwood, J. Vance Holdan and Duncan Macrae, "Electronic Instruments," vol. 21, Part II, Radiation Laboratory Series, McGraw-Hill Book Company, New York, N. Y.; 1948.

[7] Edwin A. Goldberg, "A high accuracy time division multiplier," *RCA Review*, vol. 13, pp. 265–274; September, 1952.

[8] C. D. Morrill and R. V. Baum, "Stabilized time division multiplier," *Electronics*, vol. 25, pp. 139–141; December, 1952.

[9] John F. Blackburn, "Components Handbook," vol. 17, pp. 243–287, Radiation Laboratory Series, McGraw-Hill Book Co., New York, N. Y.; 1949.

[10] David E. Sunstein, "Photoelectric waveform generator," *Electronics*, vol. 22, pp. 100–103; February, 1949.

[11] R. R. Bennett, "The generation of straight line transfer relationships," Project Cyclone Symposium I, Reeves Instrument Corp., New York, N. Y., pp. 145–148; 1952.

[12] C. D. Morrill and R. V. Baum, "Diode limiters simulate mechanical phenomena," *Electronics*, vol. 23, pp. 122–126; November, 1952.

Output devices are of two general types: one type records a variable voltage as a function of time; the other type records one variable voltage as a function of a second variable voltage. The first type is usually called a recorder; the second type is called a plotting board or an *X-Y* recorder. Direct-writing recorders capable of recording variables up to about 100 cycles per second with an accuracy of about 98 per cent are available in both ink and hot-wire types. Units having higher speed and greater accuracy may be obtained or constructed but will invariably be more complicated and less convenient to use, requiring frequent calibration and/or development of film or sensitized paper. Lower-speed recorders, capable of recording frequencies of approximately one cycle per second with errors of less than 0.2 per cent, are also available.

Plotting boards or *X-Y* recorders are generally comparable in speed and accuracy to the slow-speed recorders. They generally draw curves on 8½-inch by 11-inch, 11-inch by 17-inch, or 30-inch by 30-inch paper; one plotting unit is capable of "playing back" almost immediately a record just made.[13]

The list of components is now complete for most practical purposes. Special units required in unusual applications may usually be identified with one or more of the basic computing and input-output elements. An important feature of the electronic differential analyzer should now be apparent: with a relatively small selection of computing elements, tabulated in Fig. 4, a majority of practical scientific and engineering problems may be solved in a simple straightforward manner.

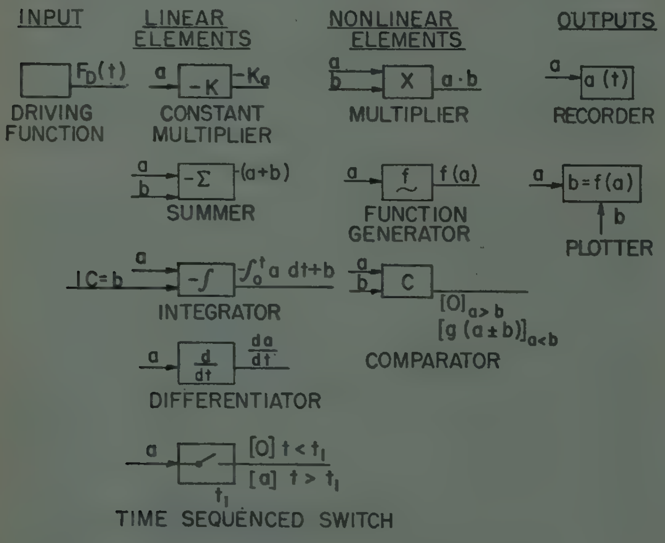


Fig. 4—Differential-analyzer elements.

REPRESENTATIVE APPLICATION

A problem exemplifying the use of the electronic differential analyzer is the analysis of an instrument servomechanism. When purely mathematical methods are used, linear characteristics[14] are usually assumed. Semianalytic methods of accounting for a predominant nonlinearity have been explored.[15-20] Sometimes, however, the combined effect of two or more nonlinearities may impair the effectiveness of the system. In such cases, simulation with an electronic differential analyzer usually provides the most satisfactory and complete method of analysis.

The components comprising the servomechanism will first be assumed linear to demonstrate more concisely the general methods used in system studies employing an analyzer.

A typical linear servomechanism is shown in block diagram form in Fig. 5. Linear relationships must be postulated to make an analysis of this servomechanism.

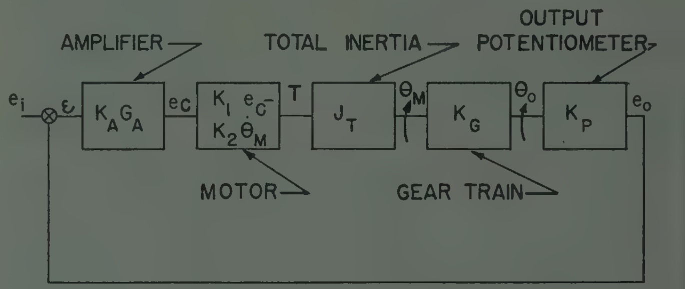


Fig. 5—Block diagram of a linear servomechanism.

For example, if a two-phase servomotor is used, it is usually assumed that the torque developed is proportional to the voltage applied to the control phase and decreases linearly with increasing speed, or

$$T_A(s) = K_M e_C(s) - K_D s\theta_M(s),^{21} \qquad (2)$$

where

$$s\theta_M = \mathcal{L}\left[\frac{d\theta_M}{dt}\right].^{22}$$

It is further assumed that the amplifier used is linear; that is,

$$e_C(s) = K_A G_A(s)\epsilon(s), \qquad (3)$$

where

$$\epsilon = e_i - e_o.$$

If the gears coupling the motor to the load are infinitely stiff and without backlash,

---

[13] P. R. Vance and D. L. Haas, "An input-output unit for analog computers," PROC. I.R.E., pp. 1483–1486; this issue.

[14] G. S. Brown and D. P. Campbell, "Principles of Servomechanisms," Chaps. 1 and 2, John Wiley and Sons, New York, N. Y.; 1948.

[15] D. A. Kahn, "An analysis of relay servomechanisms," *Trans. AIEE*, preprint T-9224, vol. 68, pp. 1079–1088; 1949.

[16] L. A. Rogers and W. C. Hurtz, "Relay servomechanisms, the shunt-motor servo with inertia-load," *Trans. ASME*, vol. 72, pp. 1163–1172; 1950.

[17] D. McDonald, "Multiple mode operation of servomechanisms," *Bull. S-3*, Cook Research Laboratories, Chicago, Ill.; 1951.

[18] A. M. Hopkins, "A phase plane approach to the compensation of saturating servomechanisms," *Trans. AIEE*, preprint TP 51–103; 1950.

[19] K. S. Miller and R. J. Schwarz, "Analysis of a sampling servo mechanism," *Jour. Appl. Phys.*, vol. 21, pp. 290–294; April, 1950.

[20] R. J. Kochenburger, "Analyzing contactor servomechanisms by frequency response methods," *Elec. Eng.*, pp. 687–692; August, 1950.

[21] See the Appendix for the definition of these terms and others used in subsequent equations.

[22] M. F. Gardner and J. L. Barnes, "Transients in Linear Systems," Chap. V, John Wiley and Sons, New York, N. Y.; 1942.

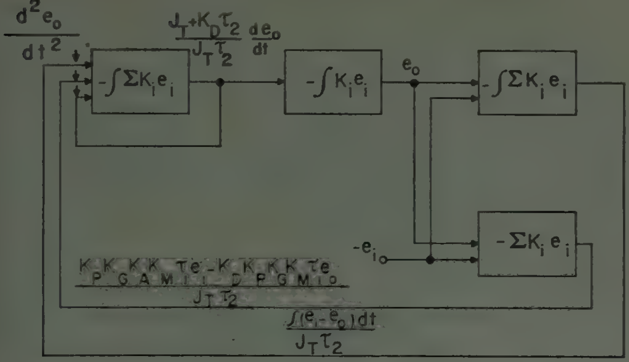

$\frac{d^2e_o}{dt^2}$
$\frac{J_T+K_D\tau_2}{J_T\tau_2}\frac{de_o}{dt}$
$-\int\Sigma K_ie_i$
$-\int K_ie_i$
e_o
$-\int\Sigma K_ie_i$
$-\Sigma K_ie_i$
$-e_i$
$\frac{K_PK_GK_AK_M\tau_1e_i-K_DK_PK_GK_M\tau_1e_o}{J_T\tau_2}$
$\frac{\int(e_i-e_o)dt}{J_T\tau_2}$

Fig. 6—Computer block diagram for solving equation 9.

$$\theta_o = K_G\theta_M, \tag{4}$$

and the total inertia at the motor shaft is:

$$J_T = J_M + K_G^2J_L. \tag{5}$$

Friction is ignored except that a sufficient gear reduction between the motor and the load is provided to reduce the static error to an acceptable amount.

The following expression relates the output voltage to the output shaft position:

$$e_o = K_P\theta_o. \tag{6}$$

The complete expression for the servo transfer function can then be written in a single equation,

$$\frac{e_o}{e_i}(s) = \frac{K_AK_MK_GK_PG_A(s)}{J_Ts^2 + K_Ds + K_AK_MK_GK_PG_A(s)}. \tag{7}$$

A number of methods of optimizing the term $K_AG_A(s)$ are available.[23,24]

Analysis of this same servomechanism can also be made with the electronic differential analyzer. Two procedures can generally be used to set up the wiring diagram for the analyzer: (1) a differential-analyzer analysis of the equations involved; and (2) a synthesis of the system which the equations represent. The procedure chosen depends upon the requirements of the problem. The first method will often require fewer computing elements and may be preferred in simulating all or part of a system which cannot or should not be changed. The second method is more readily adapted to a study of the results of varying one or more of the terms.

Equation (7) can be used to illustrate the first procedure. If $K_AG_A(s)$ in that equation is of the form $K_A[(\tau_1s+1)/(\tau_2S+1)]$, then (7) becomes:

$$\frac{e_o}{e_i}(s) = \frac{K_PK_GK_AK_M(\tau_1s+1)}{J_T\tau_2s^3 + (J_T+K_D\tau_2)s^2 + (K_D + K_PK_GK_AK_M\tau_1)s + K_PK_GK_AK_M}. \tag{8}$$

If both the numerator and denominator of the right-hand side of (8) are divided by s and rearranged,

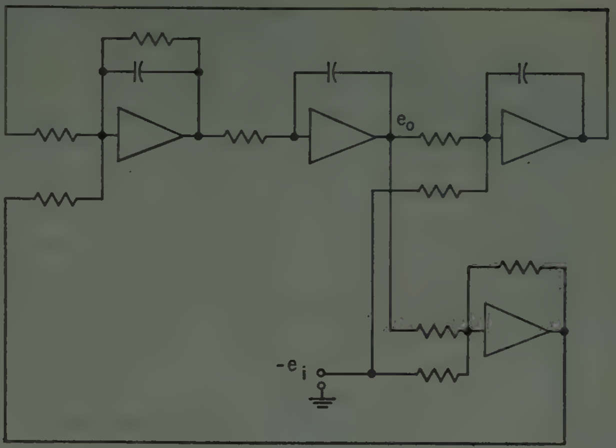


Fig. 7—Computer schematic diagram for solving equation 9.

$$s^2e_o(s) = \frac{1}{J_T\tau_2}\left\{K_PK_GK_AK_M\tau_1e_i(s) - [(J_T + K_D\tau_2)s + K_DK_PK_GK_M\tau_1]e_o(s) + \frac{e_i(s) - e_o(s)}{s}\right\}. \tag{9}$$

The analyzer block diagram with the variables shown as functions of time is given in Fig. 6. The corresponding analyzer schematic diagram is shown in Fig. 7. The values of the resistors and capacitors depend upon the scale factor in volts per unit chosen for the particular problem.[25]

The second procedure is illustrated by (2) through (6). The analyzer schematic diagram (Fig. 8) may be drawn directly from the block diagram of the system (Fig. 5). In a diagram of this kind there is usually good correspondence between the order in which the components of the real system and the order in which the components of the simulated system are arranged.

If the servomechanism to be analyzed is nonlinear, simulation by an electronic differential analyzer is the most comprehensive and most satisfactory procedure. Nonlinearities for which sufficient data are available may be taken into account.

A block diagram of a typical nonlinear servomechanism is shown in Fig. 9. Each block of the diagram corresponds to one of the partial computer schematic diagrams (Figs. 10, 12, 13, 15, 16, and 18).[26] The nonlinearities to be simulated are amplifier saturation, nonlinear servomotor characteristics, loaded gears, backlash, static and coulomb friction and granularity of the feedback potentiometer. A complete quantitative discussion of the results is beyond the scope of this paper. The method used will be explained, however, and the character of the results obtainable will be indicated.

Fig. 10 is a computer schematic of the servo error

---

[23] G. S. Brown and D. P. Campbell, *op. cit.*, chaps. 6, 7 and 8.

[24] D. McDonald, "Stabilizing servomechanisms," *Electronics*, pp. 112–116; November, 1948.

[25] G. A. Korn and T. M. Korn, *op. cit.*, chap. 2.

[26] A tabulation of the symbols used is given in the Appendix.

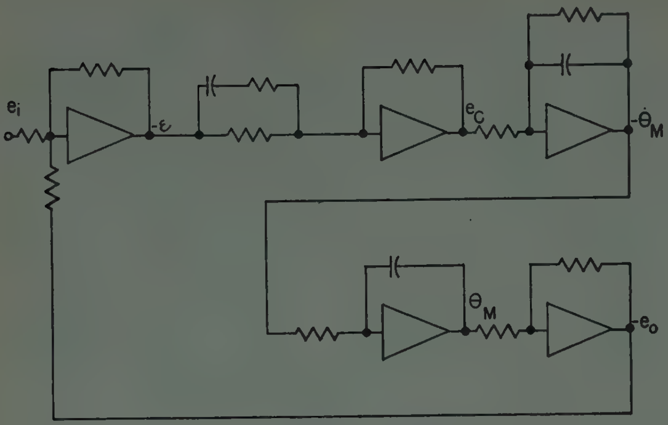

eᵢ
-ε
e_C
-θ̇_M
θ_M
-e_o

Fig. 8—Computer schematic diagram for simulating the servomechanism shown in Fig. 5.

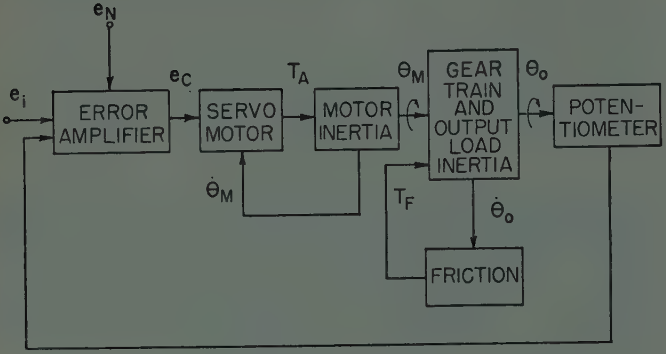

e_N
eᵢ
e_C
T_A
θ_M
θ_o
ERROR AMPLIFIER
SERVO MOTOR
MOTOR INERTIA
GEAR TRAIN AND OUTPUT LOAD INERTIA
POTEN-TIOMETER
θ̇_M
T_F
θ̇_o
FRICTION

Fig. 9—Interconnection diagram for the simulation of a nonlinear servomechanism.

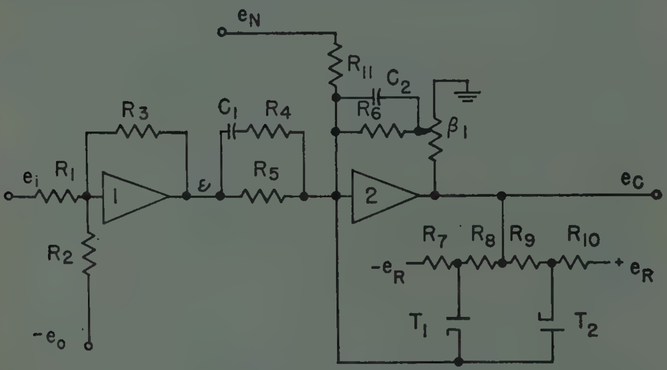

e_N
R11
C2
R6
β1
eᵢ
R1
R3
1
C1
R4
R5
ε
2
e_C
R2
-e_o
R7
R8
R9
R10
-e_R
+e_R
T1
T2

Fig. 10—Computer schematic diagram of servo error amplifier.

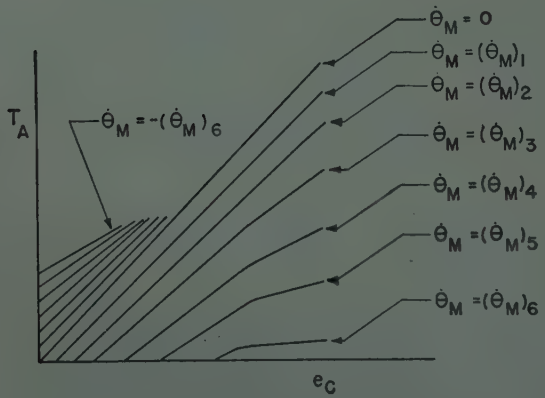


Fig. 11—Typical steady-state servomotor characteristic.

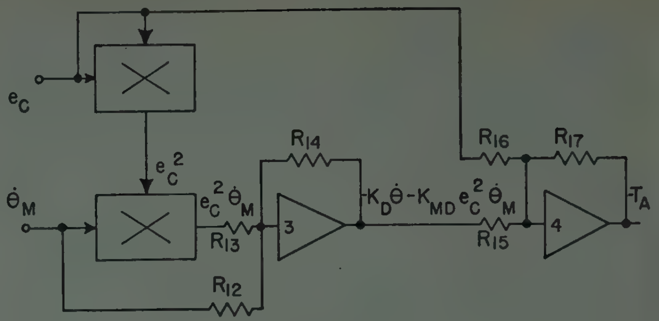

e_C
e_C²
θ̇_M
e_C² θ̇_M
R13
R12
R14
3
-K_D θ̇ - K_MD e_C² θ̇_M
R15
R16
R17
4
-T_A

Fig. 12—Computer schematic diagram for the simulation of servomotor characteristics.

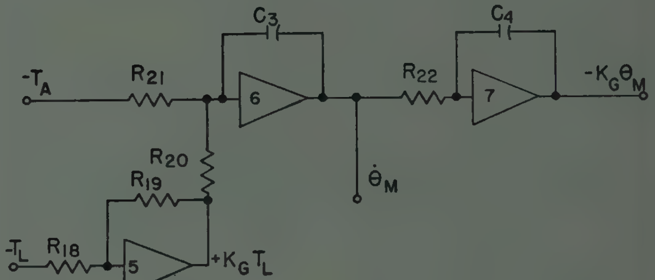

-T_A
R21
C3
6
R22
C4
7
-K_G θ_M
R20
R19
θ̇_M
-T_L
R18
5
+K_G T_L

Fig. 13—Development of $\dot{\theta}_M$ and $K_G\theta_M$ from T_A and T_L.

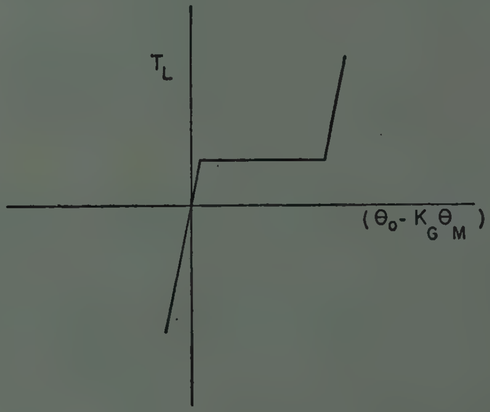


Fig. 14—Stress-strain characteristics of loaded gears.

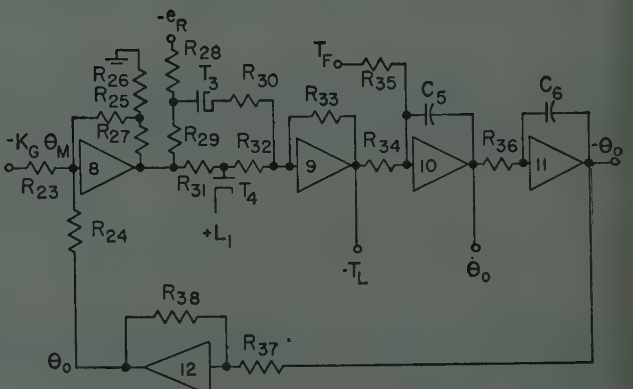

-e_R
R28
R26
R25
R27
T3
R30
T_F
R35
R33
C5
C6
-K_G θ_M
8
R29
R32
9
R34
10
R36
11
-θ_o
R23
R31
T4
R24
+L1
-T_L
θ̇_o
R38
R37
θ_o
12

Fig. 15—Development of T_L, $\dot{\theta}_o$, and θ_o from $K_G\theta_M$ and T_F.

amplifier. The stabilization network is represented by R_4 and C_1. The terminal e_N provides a means of injecting noise into the amplifier so that the effect of such noise on servo performance can be studied. Capacitor C_2 produces an effect analogous to that of the electrical time constant of the servomotor.[27] Amplifier gain may be varied with potentiometer β_1. The effect of amplifier saturation is provided by the series output limiter, R_7, R_8, R_9, R_{10}, T_1, and T_2. There are three inputs to the servo amplifier (the input voltage, e_i, the feedback voltage, e_o, and the noise voltage, e_N) and one output (the voltage applied to the servomotor, e_C).

The torque produced by a two-phase servomotor is a function of both the voltage applied to the control phase and to the speed of the motor.[28] One quadrant of a set of typical curves is shown in Fig. 11. An approximation to this function, which fits quite well the particular characteristics desired, is given by:

$$T_A = K_M e_C - K_D \dot{\theta}_M - K_{MD} e_C^2 \dot{\theta}_M. \qquad (10)$$

The computer schematic for the solution of this equation is shown in Fig. 12. There are two inputs (control voltage, e_C, and motor speed, $\dot{\theta}_M$) and one output (torque available, T_A).

The acceleration of the motor depends on the net torque and the motor inertia. The net torque is the difference between the torque available from the motor, T_A, and that required by the load, T_L. The voltage at the output of amplifier 6 (Fig. 13) represents the motor speed, which, when integrated, provides a voltage proportional to the motor shaft position at the output of amplifier 7, or:

$$\dot{\theta}_M = \int \frac{T_A - T_L}{J_M}\, dt. \qquad (11)$$

Typical stress-strain characteristics of loaded gears are shown in Fig. 14, a plot of the torque at the output shaft as a function of the relative difference between the input and output shaft positions.

In Fig. 15, amplifier 8 and associated resistors provide the high gain necessary to convert a relatively small angular difference to a relatively large torque. If there were no backlash, amplifier 8 would be all that would be required. The shunt-input limiter, T_4, provides the first break in the stress-strain characteristic of Fig. 14. The limit voltage, L_1, corresponds to the value of the applied torque that exceeds the take-up torque of the loaded gears. The stiffness of the loading spring is completely negligible so that beyond this deflection ($\theta_0 - K_G\theta_M$), there is no further change in torque, T_L, represented by the voltage at the output of amplifier 9, until the deflection has increased to a value sufficient to operate diode T_3. Beyond this value, the stiffness is again high. The difference between load torque, T_L, and torque due to friction, T_F, accelerates the output inertia, J_L. J_L is represented by R_{34} and C_5. There are two inputs to this circuit (the product of motor shaft displacement and gear ratio, $K_G\theta_M$, and the torque due to friction, T_F) and three outputs (the output shaft velocity, $\dot{\theta}_o$, the output shaft position, θ_o, and the torque available at the output shaft, T_L).

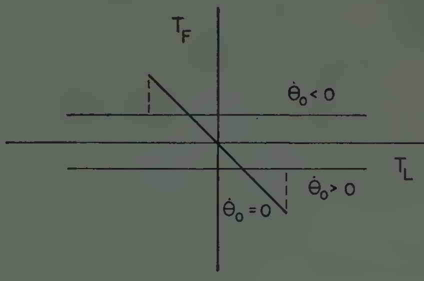


Fig. 16—$T_F = f(T_A, \dot{\theta})$.

Torque due to static and coulomb friction may be represented by a function such as that shown in Fig. 16. The differential-analyzer circuit used in this study is shown in Fig. 17. C_7 is a very small valued capacitor so that, for small inputs before the diodes conduct, the gain between the input, $\dot{\theta}_o$, and the output, T_F, is very large at all frequencies of interest. Thus, for even a minute value of $\dot{\theta}_o$, a voltage is produced at the output of amplifier 15 just sufficient to cancel the voltage proportional to T_L (see Fig. 15). Until the diodes conduct, the voltage at the output of amplifier 15 represents static friction.

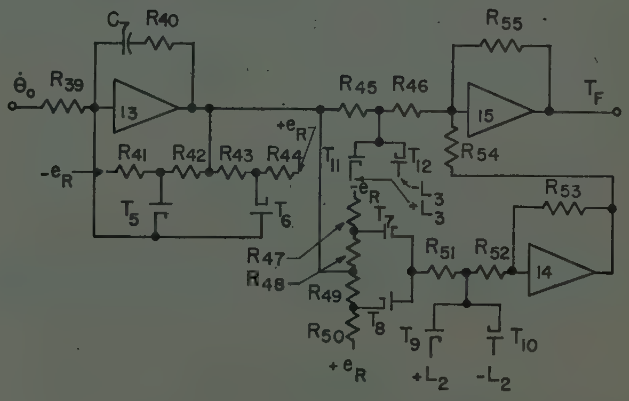


Fig. 17—Development of T_F from $\dot{\theta}_o$.

Limiter voltages L_3 are set so that conduction through diode T_{11} or T_{12} takes place at a voltage corresponding to the maximum value of static friction. Beyond this value the gain from input to output is virtually zero and $\dot{\theta}_o$ may change. The output of amplifier 13 immediately rises (or falls) to the value set by the series output limiter. Intermediate between the first and second limits, either diodes T_7 and T_9 or T_8 and T_{10} conduct, and amplifier 14 provides a voltage that is subtracted from the voltage corresponding to the maximum static friction to provide a voltage proportional to coulomb friction at the output of amplifier 15.

---

[27] L. O. Brown, Jr., "Transfer function for a two-phase induction motor," *Trans. AIEE*, preprint T1-347, vol. 70; 1951.

[28] R. J. W. Koopman, "Characteristics of two-phase servomotors," *Elec. Eng.*, vol. 68, p. 775; September, 1949.

The voltage at the arm of a potentiometer depends on the shaft position in a manner shown in Fig. 18. Fig. 19 shows the method used to simulate this relationship. The gain of amplifier 16 and associated resistors is adjusted by means of β_2 so that when the difference between θ_o and e_o represents one turn of wire on the potentiometer, the voltage at the output of amplifier 16 is large enough to fire one of the thyratrons, T_{13} or T_{14}. At this time, the output of amplifier 17 changes rapidly, reducing the difference between θ_o and e_o to zero, and the thyratron is extinguished. The time required to perform this operation is extremely small compared with the rate of change of θ_o. The repetition rate is linearly dependent on $\dot{\theta}_o$ and becomes zero when $\dot{\theta}_o$ is zero. The effect of increasing the number of potentiometer wires may be simulated by decreasing β_2.

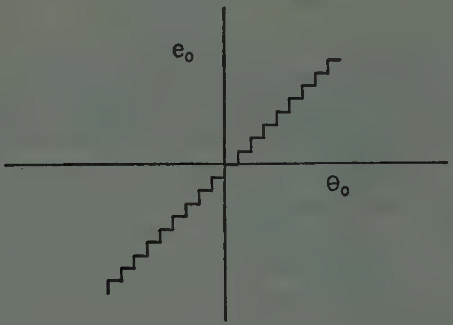


Fig. 18—Potentiometer output versus shaft position.

The results of the study showed that, for this example, a linear servo analysis has two serious shortcomings: (1) the predicted response to large signals is completely inaccurate; and (2) no indication of the size and shape of servo jitter is provided.

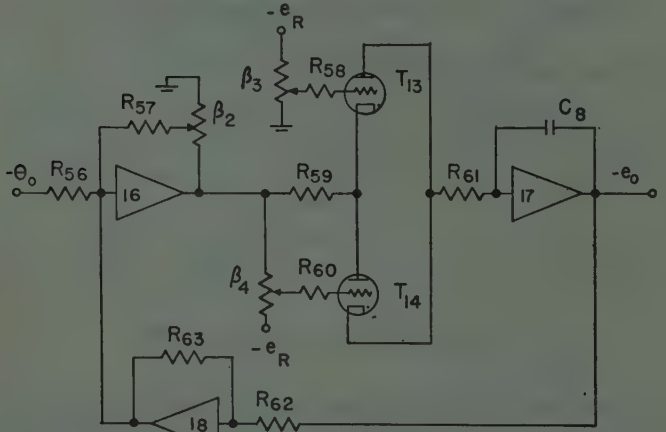


Fig. 19—Simulation of potentiometer granularity.

The agreement between the results of the nonlinear analysis and the performance of the servo was quite good. The responses to step functions of various amplitudes were in excellent agreement, the rise times of each increasing by about 4 to 1 with increase in input-step size from 10 to 100 volts. There was less similarity between the jitter of the servo and the results obtained by the differential analyzer although the amplitude and frequency of the predominant component of the jitter were in agreement; the frequency of the second most predominant frequency was high in both amplitude and frequency by about 2 to 1. This error may have been due to the omission from the analysis of potentiometer-arm characteristics (i.e., compliance).

The response of the servo and the results of the linear and nonlinear analysis are shown in Fig. 20.

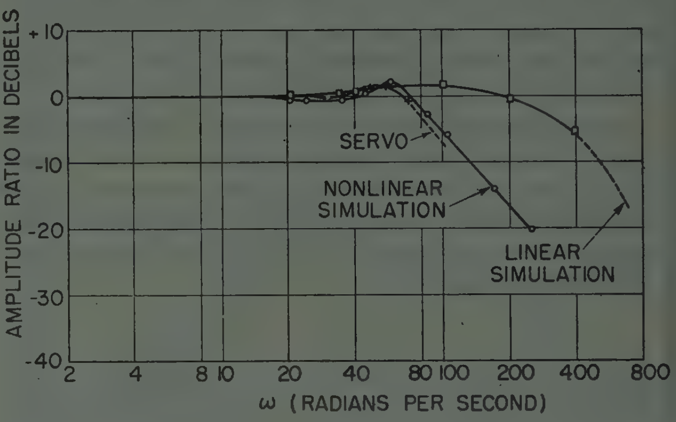


Fig. 20—Computed and measured responses as a function of frequency.

With the type of analysis described, it is possible to reduce design effort and time-consuming experimentation. Costly overdesign and unsatisfactory underdesign may be minimized. The engineer may obtain answers to such questions as:

1. Should loaded gears be used? How much backlash can be tolerated? Can gear compliance be increased without sacrificing performance?
2. What is the optimum gear ratio?
3. Is the selected motor adequate? Can a less expensive motor be used?
4. What resolution is required in the output potentiometer?
5. To achieve the desired results, must the load friction be decreased?
6. What is the effect of noise on the performance of the servo?
7. What are the tolerances on the various components?
8. What kind of external linear or nonlinear damping means would improve the performance of the servo?

It is expected that the detailed quantitative results of this study will be reported at a later date.

Scope of Application

The principal users of electronic differential analyzers are the aircraft industry and various government laboratories. Trailing these, but rapidly becoming aware of the value of this relatively new tool, are various research organizations, control manufacturers, automobile manufacturers, manufacturers of components ranging from aircraft engines and accessories to small electrical parts such as transformers and magnetic amplifiers, oil companies, power companies and schools, both for fundamental and applied research and for academic purposes.

A complete listing of the types of problems which electronic differential analyzers are known to be capable of solving would be a formidable task.[2,29–34] However, the partial list below is probably representative of the types of problems being studied in this way at the present time.

1. Analysis and synthesis of instrument servos including such unavoidable nonlinearities as static friction, gear backlash and saturation.
2. Design of process controls (for example, those used in paper mills and chemical plants).
3. Synthesis of automatic controls (for example, autopilots, atomic-reactor controls and jet-engine controls).
4. Design of suspension systems (for example, those used in bridges and automobiles).
5. Simulation of complete engines.
6. Structural vibration analysis (for example, that required in the design of aerolastic members, and turbine, aircraft, and helicopter blades).
7. Design of aircraft flight trainers and other special-purpose analog computers and simulators.
8. Diffusion problems (for example, heat flow in a friction brake, chemical processes and oil recovery).
9. Network design (for example, linear and nonlinear filters, pulse-forming networks, delay networks, equalizers).
10. Component design (for example, relays, cathode-ray tubes, magnetrons, transistors).
11. Design of piloted and pilotless aircraft (for example, airframes and guidance and control systems).
12. Ship analysis and design (for example, stability and control of surface vessels and submarines; landing of aircraft on a carrier in a heavy sea).
13. Hydraulics (for example, hydroelectric power conversion).
14. Curve fitting and Fourier analysis.
15. Data reduction
16. Basic research in nonlinear mechanics.
17. Equation synthesis.
18. Determination of auto- and cross-correlation functions.
19. Quality-control studies.
20. Traffic-flow studies.
21. Economic and business-trend studies.
22. Determination of optimum trajectories.
23. Economical power-station loading.

ADVANTAGES OF DIFFERENTIAL-ANALYZER USE

Electronic differential analyzers provide several important advantages in the study of engineering problems. In linear systems where analytic solutions are possible the differential analyzer finds application because of the ease and rapidity with which solutions are obtained. Particularly in the case of dynamic systems in which the analytic solution involves point-by-point calculations, the availability of a differential analyzer encourages studies that would be too time-consuming if carried out analytically. In those cases where nonlinearities are involved, the only hope of obtaining any useful solution often lies in the use of a differential analyzer or a digital computer.

A distinct advantage of the differential analyzer is that it is very easily set up for problem solution; the average engineer can readily learn to operate one quite capably in a few weeks' time. Since each section of a system can be separately simulated if desired, the effect on the system of changing the transfer function of any section can be readily determined. This ability furnishes the engineer with a better understanding of the system under study since the solutions are produced in a form already familiar to him.

This improved comprehension of the system in conjunction with the ease with which solutions are produced stimulate creative thinking and encourage invention. A new idea can be tried out or the component of a system can be changed so easily that new approaches to a problem can be profitably explored.

It has been found that the differential analyzer provides a new basis for understanding among engineers, somewhat analogous to the use of mathematics as a common language. Electronic, aerodynamic, servomechanical, hydraulic, and mechanical engineers, as well as mathematicians, physicists, and chemists, who become familiar with the use of the differential analyzer, soon discover the convenience of conveying their ideas in terms of computer diagrams. This new common language substantially improves their ability to understand each other's problems and increases the effectiveness of co-operative efforts.

QUANTITY OF EQUIPMENT REQUIRED

Although large variations exist in the size of electronic differential analyzers, a representative analyzer might include the following elements:

45 to 50 linear elements (summers, integrators, etc.)
3 to 5 comparators
3 to 5 function generators
3 to 5 multipliers
4 to 6 recording channels
2 to 4 X-Y recorders or plotting boards

This representative analyzer could be used effectively in the study of linear or nonlinear systems with up to 12 degrees of freedom. It could solve rather complex suspension and automatic process-control problems; many flight, ballistic, and trajectory problems; a number of nonlinear diffusion problems; and many quite

---

[29] F. J. Maginnis, "Differential analyzer applications," *General Electric Review*, vol. 48, pp. 54–59; May, 1945.

[30] G. D. McCann, S. W. Herwald and H. S. Kirschbaum, "Electrical analogy methods applied to servomechanism problems," *Trans. AIEE*, vol. 65, pp. 91–96; February, 1946.

[31] George A. Philbrick, "Designing industrial controllers by analog," *Electronics*, vol. 21, pp. 108–111; June, 1948.

[32] G. D. McCann, C. H. Wilts and B. N. Locanthi, "Electronic techniques applied to analogue methods of computation," PROC. I.R.E., vol. 37, pp. 954–961; August, 1949.

[33] Project Cyclone Symposium I, Reeves Instrument Corp., New York, N. Y.; 1951.

[34] Project Cyclone Symposium II, Reeves Instrument Corp., New York, N. Y.; 1952.

complicated network problems. In addition, the equipment could be used to solve two or more simpler problems at the same time. Such an installation would comprise four or five cabinets of equipment and could be expanded as necessary by the addition of more cabinets of linear and nonlinear elements.

CONCLUSIONS

The electronic differential analyzer is a valuable engineering tool. It has been primarily used in the aircraft industry; however, its use is rapidly spreading to other industries with fundamentally similar problems. Differential analyzers are quite easy to operate; they provide a better understanding of physical problems and tend to stimulate the flow of new ideas. They are rapidly being recognized as a basic, essential engineering tool.

APPENDIX—LIST OF VARIABLES AND CONSTANTS

e_i	Input voltage (volts)
e_o	Output voltage; that is, voltage on arm of feedback potentiometer (volts)
ϵ	$e_i - e_o$ (volts)
e_N	Noise voltage (volts)
e_C	Voltage applied to servomotor (volts)
T_A	Torque available from motor (inch ounces)
T_{SF}	Torque due to static friction (inch ounces)
T_{CF}	Torque due to coulomb friction (inch ounces)
T_F	Torque due to either static or coulomb friction (inch ounces)
θ_M	Position of motor shaft (radians)
$\dot{\theta}_M$	Motor shaft speed (radians per second)
T_L	Torque developed at the load (inch ounces)
θ_o	Position of output shaft (radians)
$\dot{\theta}_o$	Velocity of output shaft (radians per second)
J_M	Inertia of motor and first gear (inch ounce seconds squared)
J_L	Inertia of load and output gear (inch ounce seconds squared)
J_T	$J_M + K_G{}^2 J_L$
$L_1, L_2, \cdots$	Limiter-set voltages; that is, biases applied to limiter diodes (volts)
$K_A G_A$	Gain of servoamplifier (volts per volt)
K_G	Ratio of gear train coupling the motor to the output load, defined by $K_G \theta_M = \theta_o$ (radians per radian)
K_M	Steady state, linearized servomotor transfer function (inch ounces per volt)
K_P	e_o/θ_o (volts per radian)
$\pm e_R$	Positive and negative constant voltage source (volts)
K_D	Coefficient of damping (inch ounces per radian per second)
K_{MD}	Coefficient of damping (inch ounce seconds per radian volt squared)

* * *

The Solution of Partial Differential Equations by Difference Methods Using the Electronic Differential Analyzer[*]

ROBERT M. HOWE[†] AND VINCENT S. HANEMAN, JR.[‡], ASSOCIATE, IRE

Summary—**Partial differential equations can be approximated by systems of simultaneous ordinary differential equations by replacing one or more of the partial derivatives by the appropriate finite differences. The resulting ordinary differential equations can sometimes be solved directly by an electronic differential analyzer employing feedback amplifiers. Both theoretical analysis of the accuracies attainable with the difference method and actual solution examples using the electronic differential analyzer are described. Types of partial differential equations considered include the heat, wave, and beam equations.**

INTRODUCTION

THE ELECTRONIC DIFFERENTIAL analyzer is rapidly becoming an extremely important tool for engineering design. Since a computer of this type integrates with respect to only one variable, namely time, it is fundamentally limited to the solution of ordinary differential equations. To solve a partial differential equation, it is necessary first to convert the equation to one or more ordinary differential equations. If the partial differential equation is linear, this can often be done by separation of variables, which results in ordinary differential equations of the eigenvalue type. The normal modes, or eigenfunctions, can then be found, after which the complete solution is built up by combining the normal modes.

The above method of separating variables and obtaining a series type of solution can be carried out fairly efficiently on an electronic differential analyzer.[1–4] Certainly, for most problems the analyzer is much faster than any hand methods. But for the engineer who is interested in getting quantitative answers to specific problems even the analyzer approach might seem somewhat tedious. Then too, the control engineer would often like to have a real-time simulation of the system being controlled, and in many cases partial differential equations are required to describe this system. It therefore would be highly advantageous to solve the partial differential equations directly with the electronic differential analyzer. This can be done by replacing some of the partial derivatives by finite differences in order to convert the original partial differential equations into a system of ordinary differential equations.

SOLUTION OF THE HEAT EQUATION

Equation to Be Solved

As an example of a partial differential equation, let us consider the equation of heat flow through a continuous medium, since it involves second order spacial derivatives and only first order time derivatives. The basic heat equation is given by:

$$c\delta \frac{\partial u}{\partial t} = \nabla \cdot K \nabla u + f, \tag{1}$$

where

u = temperature and is a function of the spacial coordinates and time,
K = thermal conductivity, in general a function of the spacial coordinates,
c = specific heat, a function of spacial coordinates,
δ = density, also a function of spacial coordinates,
t = time
f = rate of heat supplied by sources in the medium, a function of spacial coordinates and time.

The actual heat flow or flux per unit area due to conduction normal to any surface is given by $-K$ times the component of ∇u normal to the surface. Thus the heat flux F_x across a unit surface normal to the x direction is given by:

$$F_x = -K \frac{\partial u}{\partial x}. \tag{2}$$

In a given heat flow problem it is necessary to stipulate spacial boundary conditions either on the temperature u or the heat flow $-K\nabla u$, as well as the initial temperature distribution throughout the medium.

Derivation of the Difference Equations

For simplicity in illustrating the application of difference techniques, let us assume that spacial variations in the temperature u are confined to the x direction. Equation (1) then becomes:

---

[*] Decimal classification: 621.385.2×510. Original manuscript received by the Institute, May 15, 1953. This research was partially suported by the Office of Ordnance Research, U. S. Army, under Contract No. DA-20-018-ORD-21811.

[†] Asst. prof. aeronautical eng., University of Michigan, Ann Arbor, Mich.

[‡] Capt. USAF, formerly research engineer, University of Michigan.

[1] D. W. Hagelbarger, C. E. Howe and R. M. Howe, "Investigation of the Utility of an Electronic Analog Computer in Engineering Problems," Ext. Memo. UMM-28, Univ. of Michigan Eng. Research Inst., AF Con. W33(038)ac-14222 (Project MX-794); April 1, 1949.

[2] C. E. Howe, R. M. Howe and L. L. Rauch, "Application of the Electronic Differential Analyzer to the Oscillation of Beams, Including Shear and Rotary Inertia," Ext. Memo. UMM-67, Univ. of Michigan Eng. Research Inst.; January, 1951.

[3] Howe, Howe and Rauch, "Solution of Linear Differential Equations with Time Varying Coefficients by the Electronic Differential Analyzer," Proj. Cyclone Symposium II, Part 2, 89; May, 1952.

[4] G. M. Corcos, R. M. Howe, L. L. Rauch and J. R. Sellars, "Application of the Electronic Differential Analyzer to Eigenvalue Problems," Proj. Cyclone Symposium II, Part 2, 17; May, 1952.

$$C(x)\,\frac{\partial u(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[K(x)\,\frac{\partial u(x,t)}{\partial x}\right] + f(x,t), \quad (3)$$

where we have let:

$$C(x) = c(x)\delta(x). \quad (4)$$

This could represent the temperature distribution in a medium between two infinite slabs.

Instead of measuring the temperature u at all distances x, let us measure u only at certain stations along x (Fig. 1); i.e., let u_1 be the value of u at the first x station, u_2 be the value of u at the second x station, u_n be the value of u at the nth x station. Further, let the distance between stations be a constant Δx. Thus $u(x, t)$ is replaced by $u_1(t)$, $u_2(t)$, $\cdots$, etc., and we can approximate the heat flux $F_{n-1/2}$ at the $n-\frac{1}{2}$ station as:

$$F_{n-1/2} = -K\left.\frac{\partial u}{\partial x}\right|_{n-1/2} \cong -\frac{K_{n-1/2}}{\Delta x}(u_n - u_{n-1}). \quad (5)$$

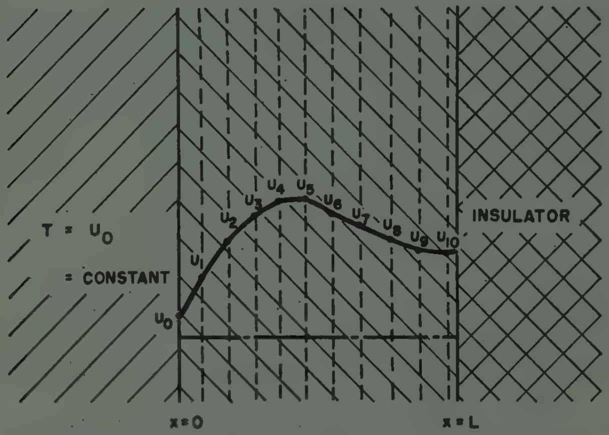


Fig. 1—Station arrangement for $N=10$, heat equation.

In fact the limit of (5) as $\Delta x \to 0$ is just the definition of the partial x derivative at that point. In the same way we can approximate the gradient of the flux at the nth station as:

$$\left.\frac{\partial}{\partial x}\left[K\frac{\partial u}{\partial x}\right]\right|_n = -\left.\frac{\partial F}{\partial x}\right|_n \cong -\frac{1}{\Delta x}(F_{n+1/2} - F_{n-1/2}). \quad (6)$$

The equation of heat-flow balance at the nth station can now be written. Thus:

$$C_n\frac{du_n}{dt} = \frac{K_{n+1/2}}{(\Delta x)^2}(u_{n+1} - u_n) - \frac{K_{n-1/2}}{(\Delta x)^2}(u_n - u_{n-1}) + f_n, \quad (7)$$

where C_n is the heat capacity at the nth station and f_n is the rate of heat supplied by a heat source at the nth station (f_n will in general be a function of time). Note that du_n/dt is now a total derivative and not a partial derivative, since by definition x is fixed for $u = u_n$.

Equation (7) will be iterated for different values of n until the boundaries in x are reached, at which point it is necessary to impose boundary conditions.

Imposing Boundary Conditions

Suppose that one of the boundary conditions specifies the temperature at $x=0$ (i.e., at the zero station). Then we have:

$$u_0 = \text{constant}$$

and hence

$$F_{1/2} = -\frac{K_{1/2}}{\Delta x}(u_1(t) - u_0). \quad (8)$$

All we have done in imposing the boundary condition, then, is to fix $u_0(t)$ at a constant value u_0. If the temperature is specified at $x=L$ (i.e., at the Nth station, where $N=L/\Delta x$), then for $u_N(t)$ we substitute $u_N=$ constant, the desired temperature.

Often a condition is placed on the rate of heat flowing past a boundary, either that this flow be zero (as for an insulating boundary) or a constant. Suppose we let:

$$F_{1/2} = \text{constant}.$$

Then the equation for the first station is:

$$C_1\frac{du_1(t)}{dt} = \frac{K_{3/2}}{(\Delta x)^2}[u_2(t) - u_1(t)] + \frac{F_{1/2}}{\Delta x} + f_1(t). \quad (9)$$

The equations for u_2, u_3, $\cdots$ are the same as usual. If we desired $F_{N-1/2}=$ constant as a boundary condition, then the equation for the Nth station is similar.

Actually, there is no reason to limit ourselves to constant boundary conditions. For example, if the temperature u_0 at one of the boundaries is a known function of time, this function can readily be introduced by means of a function generator. The process of setting in boundary conditions is evidently quite straightforward. The boundary occurs at an integral station when temperature at the boundary is specified, whereas the boundary occurs at a half-integral station when the heat flow at the boundary is specified.

Imposing Initial Conditions

In addition to specifying boundary conditions in this type of heat problem, it is necessary to specify the initial temperature distribution in our medium. Thus we have:

$$u_1(0) = U_1,\ u_2(0) = U_2,\ \cdots,\ u_N(0) = U_N. \quad (10)$$

These initial conditions must then be imposed on the electronic differential analyzer. Before considering the analyzer circuit, let us review briefly its operation.

Principles of Operation of the Electronic Differential Analyzer

The basic component of the electronic differential analyzer is the operational amplifier, which is shown in

Fig. 2. It consists of a high-gain dc voltage amplifier, a feedback impedance Z_f, and in general several input impedance (Z_a, Z_b, Z_c in Fig. 2). If we neglect the current into the dc amplifier itself (i.e. neglect the current to the grid of the input tube), it follows that $i_a+i_b+i_c=i_2$. Let us also neglect the voltage input e' to the dc amplifier as small compared with input voltage e_a, e_b, e_c and the output voltage e_2. Then we have:

$$\frac{e_a}{Z_a}+\frac{e_b}{Z_b}+\frac{e_c}{Z_c}=-\frac{e_2}{Z_f}$$

or

$$\text{output voltage} = e_2 = -\left(\frac{Z_f}{Z_a}e_a+\frac{Z_f}{Z_b}e_b+\frac{Z_f}{Z_c}e_c\right). \qquad (11)$$

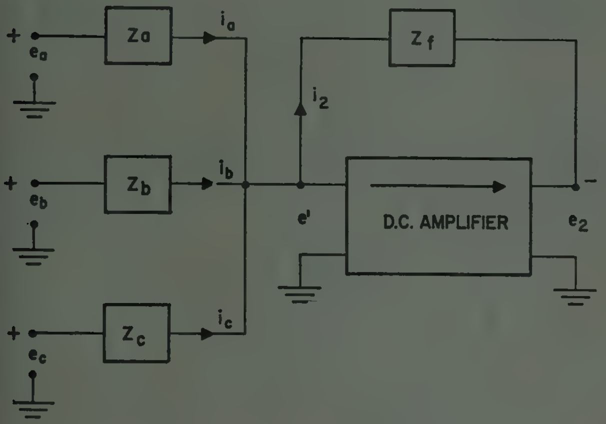

+
e_a
Za
i_a
Z f
i_2
+
e_b
Zb
i_b
e'
D.C. AMPLIFIER
e_2
−
+
e_c
Zc
i_c

Fig. 2—Operational amplifier used for summation

If the impedances in Fig. 2 are all resistors, then the operational amplifier can be used to sum the three voltages e_a, e_b, and e_c and at the same time multiply these voltages by constants Z_f/Z_a, Z_f/Z_b, Z_f/Z_c respectively. Note also that the sign of the output sum is reversed. On the other hand, if an input resistor R is used but the feedback impedance is a capacitor C, then the output voltage is the time integral of the input voltage, the time constant of integration being RC seconds.

Since operational amplifiers can perform the functions of summation, sign-changing, multiplication by a constant and integration, they can be used to solve ordinary linear differential equations with constant coefficients. By employing time-variable resistors the analyzer can solve equations with non-constant coefficients,[1-4] while multiplication devices allow the solution of nonlinear differential equations. For a more complete discussion of the theory of electronic differential analyzers the reader is referred to other articles.[1,5,6]

Differential-Analyzer Circuit for Solving Heat Equation

For purposes of illustration, let us assume the following boundary conditions for our conducting slab; at $x=0$ the temperature remains fixed at 0 and at $x=L=\Delta x(N+\frac{1}{2})$ the heat flow is zero. The space between $x=0$ and $x=L$ is therefore broken into N cells, and from (7), (8), and (9) we can write the complete set of differential equations. The initial conditions specify the temperature for each station at $t=0$. A schematic diagram showing the station locations for $N=10$ is given in Fig. 1.

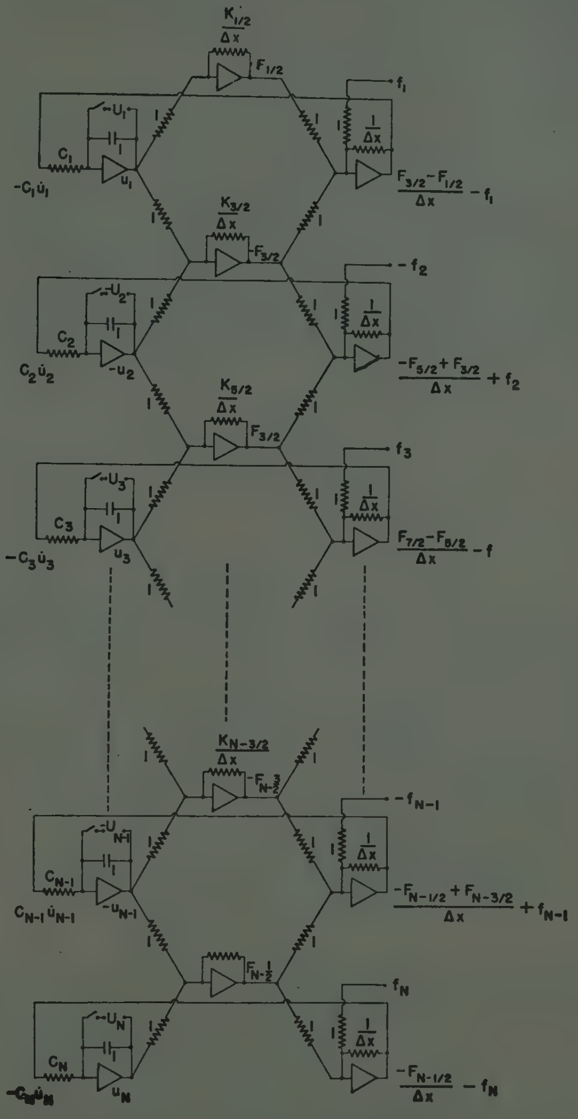

$\frac{K_{1/2}}{\Delta x}$
$F_{1/2}$
f_1
$-U_1$
C_1
U_1
$-C_1\dot{u}_1$
1
$\frac{1}{\Delta x}$
$\frac{F_{3/2}-F_{1/2}}{\Delta x}-f_1$
$\frac{K_{3/2}}{\Delta x}$
$F_{3/2}$
$-f_2$
$-U_2$
C_2
$C_2\dot{u}_2$
$-u_2$
$\frac{-F_{5/2}+F_{3/2}}{\Delta x}+f_2$
$\frac{K_{5/2}}{\Delta x}$
$F_{5/2}$
f_3
$-U_3$
C_3
$-C_3\dot{u}_3$
u_3
$\frac{F_{7/2}-F_{5/2}}{\Delta x}-f$
$\frac{K_{N-3/2}}{\Delta x}$
$-F_{N-\frac{3}{2}}$
$-f_{N-1}$
U_{N-1}
C_{N-1}
$C_{N-1}\dot{u}_{N-1}$
$-u_{N-1}$
$\frac{-F_{N-1/2}+F_{N-3/2}}{\Delta x}+f_{N-1}$
$F_{N-\frac{1}{2}}$
f_N
$-U_N$
C_N
$-C_N\dot{u}_N$
u_N
$\frac{-F_{N-1/2}}{\Delta x}-f_N$

Fig. 3—Computer circuit for solving the general heat equation with temperature=0 at $x=0$ and heat flux=0 at $x=L=(N+1/2)\Delta x$.

The computer arrangement for solving the difference equations is shown in Fig. 3. Note that the outputs of each successive row of amplifiers are reversed. This allows the necessary differences to be taken without sign-reversing amplifiers. Note also that the heat flow or flux F is available at any half-station as a dependent variable. Thus the temperature u and heat flux F

---

[5] J. R. Ragazzini, R. H. Randall and E. A. Russell, "Analysis of problems in dynamics by electronic circuits," Proc. I.R.E., vol. 35, pp. 444–452; May, 1947.

[6] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., New York, N. Y.; 1952.

across the slab can be observed directly as a function of time.

It is possible to reduce the number of amplifiers from three to one per station. In many ways, however, the circuit of Fig. 3 is simpler despite the increased number of amplifiers. To change the conductivity K or heat capacity C at any station, only the appropriate resistor has to be varied. Initial temperature distribution across the slab is changed by setting the $U_1, U_2, \cdots U_n$ voltages to the desired values. The heat sources through the slab are represented by the voltages $f_1, f_2, \cdots f_n$ which may be varied as a function of time in any desired manner.

Solution by Separation of Variables

In order to evaluate the accuracy of the difference technique, it is worth while to solve the partial differential equations of heat flow by separating variables. For simplicity we will solve the problem of the temperature distribution between two infinite slabs held at a temperature of zero. Assume that the medium has constant conductivity K and constant specific heat capacity C. Also assume no heat sources within the medium. Then from (3):

$$\frac{C}{K}\frac{\partial u}{\partial t} = \frac{\partial^2 u}{\partial x^2}. \tag{12}$$

The boundary conditions are:

$$u(0, t) = u(L, t) = 0. \tag{13}$$

Let us assume as a simple initial condition that the temperature in the medium is everywhere constant at $t=0$. Thus:

$$u(x, 0) = U_0 = \text{constant}. \tag{14}$$

The complete solution can be written in the series form:

$$u(x, t) = \frac{4U_0}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\frac{n\pi x}{L}\,e^{-(K/C)(n^2\pi^2/L^2)t} \qquad (n = 1, 3, 5, \cdots). \tag{15}$$

This solution actually represents an infinite number of sinusoidal temperature distributions across the medium from $x=0$ to $x=L$. At $t=0$ the sine waves all add up to give the initial flat temperature distribution. For $t>0$ the sine waves decay exponentially at different rates, with the decay rate faster for those sine waves having more nodes and loops. The resulting temperature distribution at various times is plotted in Fig. 4, where we have used a dimensionless time variable τ defined as:

$$\tau = \frac{K}{CL^2}t. \tag{16}$$

We will now proceed to calculate the decay-time constants for the normal modes of the difference equation representation. If these agree well with the decay-time constants in the solution above, and if the equivalent normal modes show good agreement with sine waves, then we can expect accurate results using the difference technique.

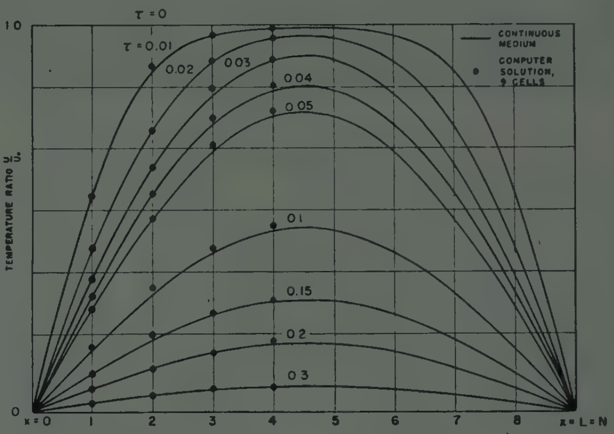


Fig. 4—Tempertaure distribution as a function of time.

Solution of the Difference Equation for N Cells

When the space between $x=0$ and $x=L$ is broken up into N cells, the general difference equation is given by (7). At station 1 and station $N-1$ the difference equation is obtained by setting u_0 and u_N equal to zero respectively. In the problem under consideration the conductivity K and specific heat capacity C are constant. By proper choice of our distance variable x we can make $\Delta x=1$, so that $L=N\Delta x=N$. By proper choice of our time variable t we can make $C/K=1$ so that for $f=0$, (7) becomes for the ith cell,

$$\dot{u}_i = u_{i+1} - 2u_i + u_{i-1}. \tag{17}$$

To solve for the normal modes we assume that the temperature u_i at the ith station varies with time as $a_i e^{-\lambda t}$, where a_i is a constant. If this is true, then (17) becomes a set of $N-1$ simultaneous algebraic equations. The only nontrivial solution of the equations is obtained when the determinant of the coefficient vanishes. This determinant, when expanded, becomes a polynomial in λ of order $N-1$. The polynomial will have $N-1$ positive roots λ_n which are the decay constants for our N cell system. To solve this determinant for a specific N is very tedious, and to solve it in general would be next to impossible. The roots λ_n can be found much more easily by the following procedure:

Assume that the spacial mode shape for the difference equations is the same as for the continuous equation, i.e., sinusoidal. If this is true, then for the temperature u_i at the ith station we have:

$$u_i = a\sin\frac{n\pi i}{N}e^{-\lambda_n t}. \tag{18}$$

From simple trigonometry it follows that:

$$u_{i+1} - u_{i-1} = 2a\sin\frac{n\pi i}{N}\cos\frac{n\pi}{N}e^{-\lambda_n t}. \tag{19}$$

From (17), (18) and (19) we have for the ith station:

$$(2-\lambda_n)\sin\frac{n\pi i}{N}\,\epsilon^{-\lambda_n t} = 2\sin\frac{n\pi i}{N}\cos\frac{n\pi}{N}\,\epsilon^{-\lambda_n t},$$

from which:

$$\lambda_n = 2\left(1-\cos\frac{n\pi}{N}\right). \tag{20}$$

It is easy to show that (18) satisfies the boundary conditions. Thus, our assumed solution is the exact solution, where the decay constants λ_n are given by (20). Expanding (20) in a power series, we have:

$$\lambda_n = \left(\frac{n\pi}{N}\right)^2\left[1-\frac{1}{12}\left(\frac{n\pi}{N}\right)^2+\cdots\right]. \tag{21}$$

In the limit of infinitely many cells the λ_n values given in the above equation reduce to the decay constants in (15), since here $L = N\Delta x = N$ and $K/C = 1$.

In Fig. 5 the percentage deviation in decay constant due to the difference method as a function of the number of cells N is shown. Note that the lower modes (lower values of n) require fewer cells to give accurate decay constants.

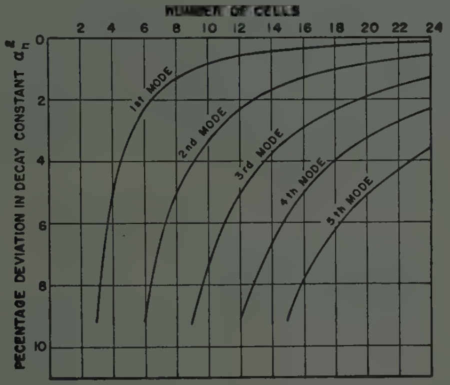


Fig. 5—Percentage deviation in the decay constant as a function of the number of cells.

To summarize, we see that when the spacial derivatives of the heat equation in a uniform medium are replaced by finite differences, the resulting normal mode shapes agree exactly, whereas the decay constants (eigenvalues) for each mode are somewhat smaller. This means that the higher modes will decay somewhat slower when the difference equation approximation is used. The error is bigger for higher modes, but fortunately the higher modes are generally much less important.

Differential-Analyzer Solution for One-Dimensional Heat Flow

Let us now examine the actual electronic differential analyzer solution of the heat-flow, problem considered in the last section, namely the temperature distribution between two infinite slabs a distance L apart and with boundaries held at zero temperature. This problem was solved with 9 cells; the computer circuit is similar to that shown in Fig. 3, with $\Delta x = 1$, $C = 1$, $K = 1$, $f = 0$, and $u_0 = u_N = 0$. Recordings of the temperature solution at stations 1, 2, 3, and 4 after an initially constant temperature distribution are shown in Fig. 6. Points from the computer solutions are compared with the theoretical temperatures in Fig. 4.

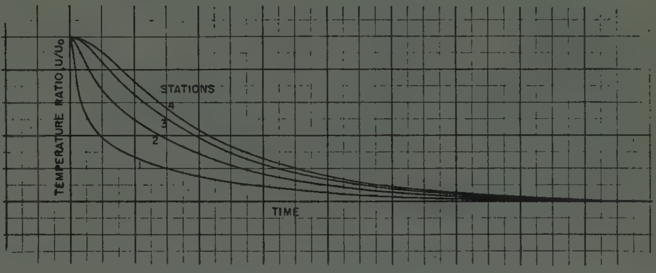


Fig. 6—Sample solutions of heat equation.

Since our initial temperature distribution is symmetric about the station $4\frac{1}{2}$, as are our boundary conditions, the temperature distribution remains symmetrical as a function of time. Therefore, the heat flow will be zero at station $4\frac{1}{2}$, and the appropriate boundary condition can be established there. If this is done, it is only necessary to solve the problem half-way across the distance between the slabs, the solution for the other half being symmetrical. Thus only four cells are actually required for this particular problem.

Computer Solution for Two-Dimensional Heat Flow

It was felt that it would be interesting to solve at least one second-order space problem using the difference technique. Because only one amplifier per cell is required, the heat equation was selected as the simplest two-dimensional problem for the electronic differential analyzer. Consider a homogeneous medium of rectangular cross section (Fig. 7). Let the temperature u be a function of x and y and independent of the height z. The walls are held at zero temperature and separated by X and Y respectively. We can select the units of time so that $K/C = 1$. Thus, the heat equation becomes:

$$\frac{\partial u}{\partial t} = \frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} \tag{22}$$

with boundary conditions:

$$u(-X/2, y, t) = u(X/2, y, t) = u(x, -Y/2, t)$$
$$= u(x, Y/2, t) = 0.$$

By selecting the units in x and y properly we can make $\Delta x = \Delta y = 1$. Thus for an $N \times N$ cell division $X = Y = N$.

Since the initial distribution is symmetrical with respect to the x and y axes, we can solve the problem in one quadrant, subject to the new boundary conditions:

$$u\left(-\frac{X}{2}, y, t\right) = u\left(x, \frac{Y}{2}, t\right) = 0 \tag{23}$$

$$\frac{\partial u}{\partial x}(0, y, t) = \frac{\partial u}{\partial x}(x, 0, t) = 0. \qquad (24)$$

The difference equation for the temperature $u_{n,m}$ becomes:

$$\frac{du_{n,m}}{dt} = u_{n+1,m} - u_{n-1,m} - 4u_{n,m} + u_{n,m+1} + u_{n,m-1}. \qquad (25)$$

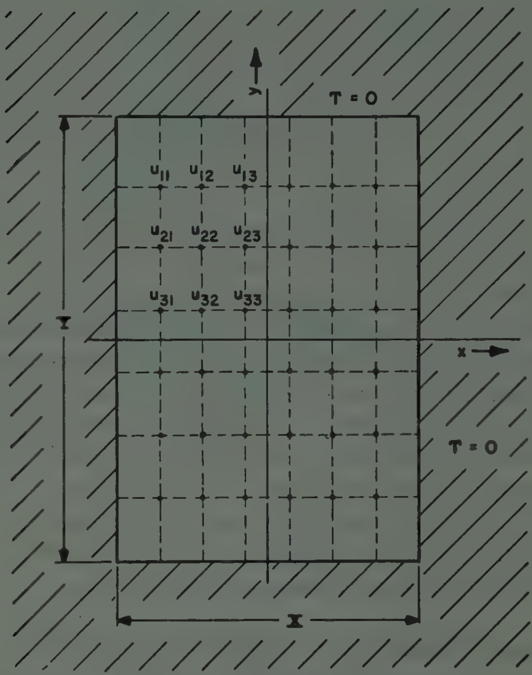


Fig. 7—Two dimensional problem in heat flow.

Let us consider the 7-cell by 7-cell system shown in Fig. 7. The boundary conditions of (23) are imposed by setting:

$$u_{01} = u_{02} = u_{03} = u_{10} = u_{20} = u_{30} = 0,$$

and the boundary conditions of (24) by setting:

$$u_{13} = u_{14}, \qquad u_{23} = u_{24}, \qquad u_{33} = u_{34},$$
$$u_{31} = u_{41}, \qquad u_{32} = u_{42}, \qquad u_{33} = u_{43}.$$

As in the case of the one-dimensional heat flow treated in the previous sections, we solve the problem for an initial temperature which is everywhere constant. Thus, the initial condition becomes:

$$u_{n,m} = U_0 = \text{constant}.$$

When this problem was solved with the electronic differential analyzer, the resulting temperatures agreed closely with the theoretical values calculated for a continuous medium.

Summary of Investigation of the Use of Difference Techniques for the Heat Equation

We have shown that it is both simple and straightforward to solve the heat equation with the electronic differential analyzer by replacing spacial derivatives with finite differences. Normal mode shapes show exact agreement with those calculated by separation of variables for the simple problems considered. Decay constants corresponding to the various modes also show good agreement but tend to be somewhat lower than the values calculated by separation of variables, particular for higher modes or if fewer cells are used. For most engineering problems the order of eight to sixteen cells per spacial dimension should be completely adequate (Fig. 5). Only one operational amplifier is needed per cell, although in some problems it may be more convenient to use three amplifiers per cell. The problem is completely stable, and the final outputs of the computer are temperature and heat flow as a function of spacial co-ordinates and time.

The difference method can be used for problems where the coordinate systems are not Cartesian. The authors have solved successfully problems in cylindrical co-ordinates and the method should be equally effective for spherical and other co-ordinate systems.

It should be pointed out that the heat equation can be solved by the difference method with a passive network of resistors and capacitors. The active-circuit approach presented here has the advantage of versatility, ability to handle nonlinearities, and low-impedance outputs. In addition, the extreme flexibility in time scale of the electronic differential analyzer should allow a real-time simulation of heat-transfer systems when those systems are part of an automatic control process. Such a simulation could be extremely useful in designing and testing the control system.

SOLUTION OF THE WAVE EQUATION

Equation to Be Solved

One of the most important partial differential equations met in engineering is the wave equation. If we let ϕ represent the magnitude of a disturbance in any medium in which wave propagation can take place, then we can write the wave equation as:

$$\nabla^2\phi = \frac{1}{v^2}\frac{\partial^2\phi}{\partial t^2}. \qquad (26)$$

Here v is the wave velocity in the medium and t is the time variable. Equation (26) must of course be subject to spacial boundary conditions and initial time conditions. The spacial derivatives of the wave equation have exactly the same form as the heat equation, but the time derivative is second order instead of first order. The difference techniques for converting the partial differential equation to a system of ordinary differential equations in time are also practically identical.

In order to have a specific problem involving the wave equation to use as an example, the classical problem of the vibrating string will be treated. Consider the string shown in Fig. 8. Let the string be fastened at $x=0$ and $x=L$, and assume that the transverse displacement of the string is $\phi(x, t)$. If T is the longitudinal tension in the string and $\mu(x)$ is the mass per unit length of the string at any x, then the equation of motion for the string becomes:

$$\frac{\partial^2\phi}{\partial x^2} = \frac{\mu(x)}{T}\frac{\partial^2\phi}{\partial t^2} \tag{27}$$

with boundary conditions

$$\phi(0, t) = \phi(L, t) = 0, \tag{28}$$

which is seen to be the wave, (26), in one space dimension.

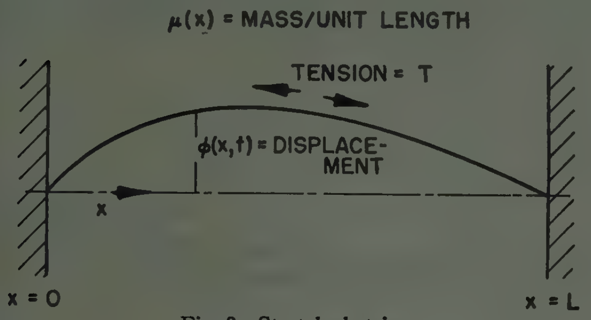

μ(x) = MASS/UNIT LENGTH
TENSION = T
φ(x,t) = DISPLACEMENT
x
x = O
x = L

Fig. 8—Stretched string.

Thus the velocity of wave propagation in the string is given by $v=\sqrt{T/\mu}$ and in general may be a function of x. When the wave velocity is a function of spacial coordinates, (27) is much more difficult to solve by separation of variables, and hence it is of considerable interest to have a direct method of solution by means of a computer.

Derivation of the Difference Equation for the Stretched String

We now proceed to break the string up into N cells a distance Δx apart. The difference equation for ϕ_n, the displacement at the nth station, is given by:

$$\frac{(\Delta x)^2}{v_n^2}\frac{d^2\phi_n}{dt^2} = \phi_{n+1} - 2\phi_n + \phi_{n-1}. \tag{29}$$

Here $v_n=\sqrt{T/\mu_n}$, where v_n is the wave velocity at the nth station and μ_n is the mass per unit length at the nth station.[7] The boundary conditions given in (28) are imposed by letting $\phi_0=\phi_N=0$. The computer circuit for solving the difference equation is shown in Fig. 9. The equation is subject to initial condition $\phi_1(0)$, $\phi_2(0)$, $\cdots$ $\phi_{N-1}(0)$ and $\phi_1(0)$, $\phi_2(0)$, $\cdots$ $\phi_{N-1}(0)$.

For some types of problems involving the wave equation, $\partial\phi/\partial x$ may be specified at the boundary instead of ϕ. In this case the boundary occurs half-way between two stations, and the boundary condition is imposed by equation the ϕ's on either side of the boundary.

Comparison of Normal Modes for Continuous and Difference Equations

Once again it will prove instructive to solve for the normal modes of vibration of our stretched string by separating time and space variables. By comparing the normal mode shapes and frequencies obtained by this method with those gotten from the difference equations, we can evaluate critically the accuracy of the difference method as a function of the number of cells. If the string is uniform, separation of variables yields pure sinusoidal mode shapes with a normal-mode frequency ω_n given by:

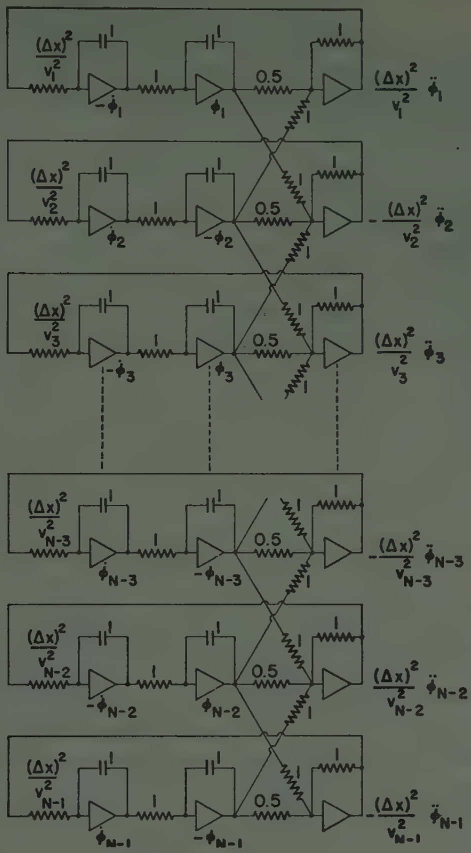

$\frac{(\Delta x)^2}{v_1^2}$
$-\phi_1$
ϕ_1
0.5
1
$\frac{(\Delta x)^2}{v_1^2}\ddot{\phi}_1$
$\frac{(\Delta x)^2}{v_2^2}$
ϕ_2
$-\phi_2$
$-\frac{(\Delta x)^2}{v_2^2}\ddot{\phi}_2$
$\frac{(\Delta x)^2}{v_3^2}$
$-\phi_3$
ϕ_3
$\frac{(\Delta x)^2}{v_3^2}\ddot{\phi}_3$
$\frac{(\Delta x)^2}{v_{N-3}^2}$
ϕ_{N-3}
$-\phi_{N-3}$
$-\frac{(\Delta x)^2}{v_{N-3}^2}\ddot{\phi}_{N-3}$
$\frac{(\Delta x)^2}{v_{N-2}^2}$
$-\phi_{N-2}$
ϕ_{N-2}
$\frac{(\Delta x)^2}{v_{N-2}^2}\ddot{\phi}_{N-2}$
$\frac{(\Delta x)^2}{v_{N-1}^2}$
ϕ_{N-1}
$-\phi_{N-1}$
$-\frac{(\Delta x)^2}{v_{N-1}^2}\ddot{\phi}_{N-1}$

Fig. 9—Computer circuit for solving the wave equation.

$$\omega_n = \frac{n\pi}{L}\sqrt{\frac{T}{\mu}}, \qquad n = 1, 2, 3, \cdots. \tag{30}$$

As in Section II we also assume sinusoidal mode shapes for the difference equation, from which the normal-mode frequency λ_n is given by:

$$\begin{aligned}\lambda_n^2 &= \frac{2T}{\mu}\left(1-\cos\frac{n\pi}{N}\right)\\ &= \left(\frac{n\pi}{N}\right)^2\frac{T}{\mu}\left[1-\frac{1}{12}\left(\frac{n\pi}{N}\right)^2+\cdots\right]\\ &\qquad n = 1, 2, \cdots.\end{aligned} \tag{31}$$

Here $\Delta x=1$ and therefore $N=L$. In the limit of infinitely many cells N the λ_n given in (31) reduces to ω_n for the continuous string. For a finite N the normal-mode frequencies from the difference equations are evidently lower than those for the continuous string. A plot of this frequency deviation as a function of the number of cells for the first seven modes is shown in Fig. 10.

---

[7] In this case the difference equation actually represents the physical problem of a string with mass concentrated at each x station.

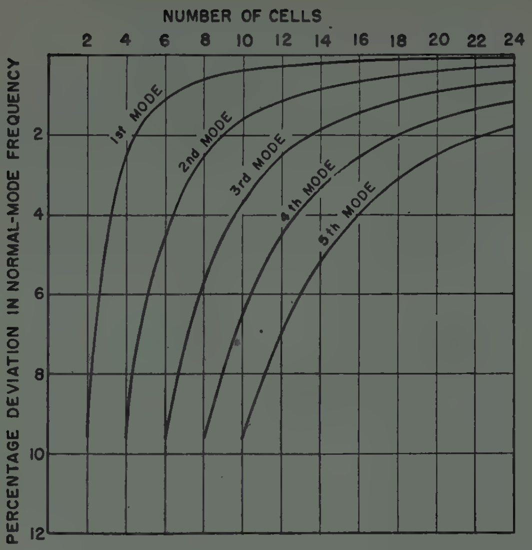


Fig. 10—Comparison of normal-mode frequencies of the difference equations and the continuous string.

8-Cell Computer Solution of Wave Equation

An 8-cell approximation to the continuous string was set up on the differential analyzer, using integrator time constants of 0.2 seconds. Comparison of computer normal-mode frequencies and theoretical frequencies is shown in the following Table I.

TABLE I

Mode Number	Cont. String	8-Cell Theoretical	8-Cell Computer
1	0.313 cps	0.310 cps	0.310 cps
2	0.625	0.610	0.608
3	0.938	0.884	0.877
4	1.250	1.125	1.124
5	1.563	1.321	1.316
6	1.875	1.470	1.468

Summary of Investigation of Difference Techniques Applied to Wave Equation

The equation of the stretched string has been solved both by separation of variables and by replacing spacial derivatives with finite differences. Comparison of the normal-mode shapes in both cases shows exact agreement. Comparison of normal-mode frequencies shows the difference equation frequencies are somewhat lower than the true frequencies, particularly for higher modes or if fewer cells are used (Fig. 10). Since the string equation is the wave equation, the above remarks apply to the solution of the wave equation in general by difference techniques.

The solution of the wave equation by difference methods is easily performed by the differential analyzer when the medium of propagation is nonuniform. Also, the effect of damping forces can readily be included, as well as effects of external time-varying forces along the string. Boundary conditions which are time varying can be handled, too.

Thus far we have considered partial differential equations with boundary conditions occurring a finite distance apart. It seems evident that our difference techniques as used here are limited to this type of equation. Thus, it would not appear possible to solve problems in semi-infinite or infinite media unless one can approximate the boundary conditions at a finite distance.

VIBRATING BEAMS

Equation to Be Solved

It would seem of particular engineering interest to investigate the usefulness of the difference technique in solving the problem of flexural vibration of beams Consider the vibrating beam shown in Fig. 11. If we limit ourselves to the transverse deflection shown and assume that the flexural planes remain parallel, then for small deflections the equation of motion is given by:

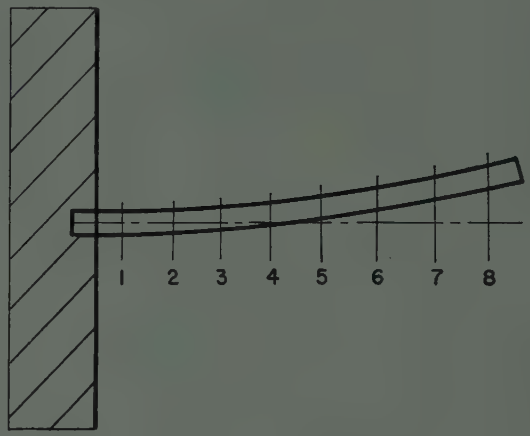


Fig. 11—Vibrating beam.

$$\rho(x)\,\frac{\partial^2 y(x,t)}{\partial t^2}+\frac{\partial^2}{\partial x^2}\left[EI(x)\,\frac{\partial^2 y(x,t)}{\partial x^2}\right]=0, \qquad (32)$$

where

x = horizontal distance from left end of beam
t = time
$y(x, t)$ = transverse deflection of the beam at any instant
$\rho(x)$ = mass per unit length of the beam
$EI(x)$ = flexural rigidity.

The bending moment $M(x, t)$ is given by:

$$M(x,t)=EI(x)\,\frac{\partial^2 y(x,t)}{\partial x^2} \qquad (33)$$

and the shear force is given by:

$$V(x,t)=\frac{\partial}{\partial x}\,M(x,t). \qquad (34)$$

Equation (32) is of course subject to both boundary and initial conditions. One type of beam of considerable engineering interest is the cantilever beam (one end built-in, the other free). We will also consider the hinged-hinged beam because it is the easiest to analyze theoretically and will give us a good idea of how the other beams will behave when difference techniques are used.

Derivation of the Difference Equation for the Vibrating Beam

Once again the partial differential (32) for the vibrating beam is converted into a set of ordinary differential equations by using the difference technique. Thus, distance along the beam is broken into N segments of width Δx; the displacement y_n at the nth station will then be a function of time only. We have from (32) as the equation of motion of the nth cell:

$$(\Delta x)^2 \rho_n \frac{d^2 y_n}{dt^2} + M_{n+1} - 2M_n + M_{n-1} = 0, \quad (35)$$

where

$$M_i = \frac{EI_i}{(\Delta x)^2}(y_{i+1} - 2y_i + y_{i-1}). \quad (36)$$

We also note that:

$$V_{n-1/2} = \frac{M_n - M_{n-1}}{\Delta x} \quad (37)$$

and

$$\left.\frac{\partial y}{\partial x}\right|_{n-1/2} = \frac{y_n - y_{n-1}}{\Delta x}. \quad (38)$$

Before writing down the complete set of difference equations for N cells, it is necessary to consider the boundary conditions. Assume we have an N cell beam and wish to impose the boundary conditions associated with a particular end fastening, e.g., a free end at the right-hand extremity of the beam. This means that both the shear V and bending moment M must vanish at the beam end. Let us assume, then, that the end occurs at $N+\frac{1}{2}$ and that $V_{N+1/2}=0$. From (37) this implies that $M_N = M_{N+1} = 0$. But from (35) this means that:

$$(\Delta x)^2 \rho_N \frac{d^2 y_N}{dt^2} + M_{N-1} = 0$$

and

$$(\Delta x)^2 \rho_{N-1} \frac{d^2 y_{N-1}}{dt^2} = 2M_{N-1} + M_{N-2} = 0.$$

The remainder of the equations are similar to (35) until the left-hand boundary is reached, at which point the difference equations again depend on the type of end fastening.

Following the same line of reasoning as above, one obtains the following set of conditions (see Table II) for the difference equations for various end fastenings of an N cell beam:

TABLE II

End	Where End Occurs	End Condition
Free	$N+\frac{1}{2}$	$M_N = M_{N+1} = 0$
Hinged	N	$M_N = y_N = 0$
Built-In	$N+\frac{1}{2}$	$y_N = y_{N+1} = 0$

Computer Circuit for Solving the Cantilever Beam by Difference Techniques

Since it involves both a free end and a built-in end, the cantilever beam shown in Fig. 11 seems the best choice for a specific example. The left-hand end of this beam occurs at station $\frac{1}{2}$, while the right-hand end occurs at station $N+1/2$. From (35) and (36) along with boundary conditions the computer circuit shown in Fig. 12 is obtained. Initial conditions on y_n and $\dot{y}_n$ must of course be specified in an actual problem. Notice that even though the left-hand end of the beam occurs at station $\frac{1}{2}$, the displacement y_1 at station 1 is held fixed at zero.

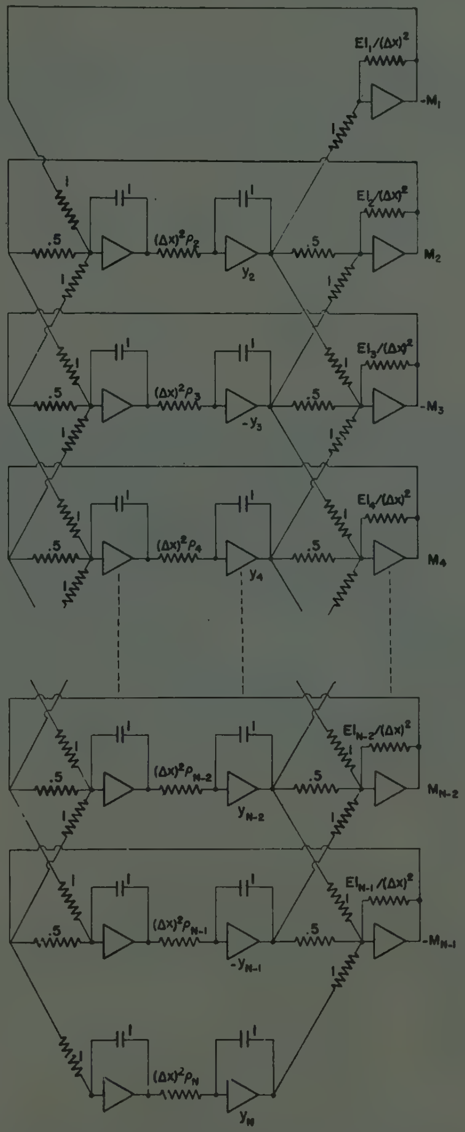


Fig. 12—Computer circuit for solving the cantilever beam by the difference method.

Accuracy of the Difference Method for Hinged-Hinged Beams

In order to check the accuracy of the difference method for beams, we will now solve for the normal modes of vibration of a hinged-hinged beam by separation of variables. The resulting mode shapes and frequencies will then be compared with the difference-equation solution of the normal modes for a hinged-hinged beam. From (32) we have for a uniform beam:

$$\frac{\rho}{EI}\frac{\partial^2 y}{\partial t^2}+\frac{\partial^4 y}{\partial x^4}=0. \tag{39}$$

It is easy to show that the normal modes of vibration of the uniform hinged-hinged beam are sinusoidal in shape; the normal-mode frequency is given by:

$$\omega_n=\left(\frac{n\pi}{L}\right)^2\sqrt{\frac{EI}{\rho}}, \qquad n=1,2,3,\cdots. \tag{40}$$

Following the method used for the heat equation one can show that the mode shapes for the difference-equation representation of the hinged-hinged beam are also sinusoidal, where the normal-mode frequency λ_n is given by:

$$\begin{aligned}\lambda_n{}^2&=\frac{2EI}{\rho}\left[3-4\cos\frac{n\pi}{N}+\cos\frac{2n\pi}{N}\right]\\&=\left(\frac{n\pi}{N}\right)^2\frac{EI}{\rho}\left[1-\frac{1}{6}\left(\frac{n\pi}{N}\right)^2+\cdots\right]\\&\qquad n=1,2,3,\cdots.\end{aligned} \tag{41}$$

Again we have taken $\Delta x=1$, so that $N=L$. As the number of cells N becomes very large the normal-mode frequency λ_n approaches the value ω_n for the continuous beam. For finite N the difference-equation frequency λ_n is somewhat lower than the true frequency ω_n. A plot of the percentage deviation in normal-mode frequency versus the number of cells is shown in Fig. 13 for the first five modes.

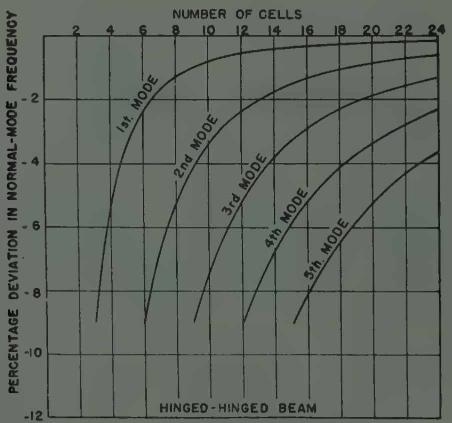


Fig. 13—Frequency deviation for a hinged-hinged beam.

Accuracy of Difference Method for Cantilever Beams

In order to find the normal-mode frequencies for a continuous uniform cantilever beam it is necessary to solve a transcendental equation.[8] The following values are obtained (see Table III) for the dimensionless frequency parameter $\beta_n=\omega_n\sqrt{\rho L^4/EI}$:

TABLE III

Mode	1	2	3	4	5
β_n	3.516	22.03	61.7	121.0	199.8

There appears to be no simple way to find the normal-mode frequencies and shapes for the difference approximation to the cantilever beam. After assuming the deflection y_i at each station varies as $\sin \lambda t$ we obtain a set of $N-1$ simultaneous algebraic equations. These equations can be satisfied only if the determinant of the y_i coefficients vanishes. This in turn gives a polynomial of degree $N-1$ in λ^2, the roots of which are the eigenvalues λ_n. The problem must be resolved for each different number of cells N, and the algebra becomes quite tedious for large N.[9] In Fig. 14 the percentage deviation in normal-mode frequency λ_n calculated in this way is plotted as a function of the number of cells for the first four modes. In Fig. 15 mode shapes for the difference approximation are compared with the continuous mode shapes for 4 and 8 cells. Note that even with only 4 cells (requiring 9 operational amplifiers) the first several modes are fairly well represented.

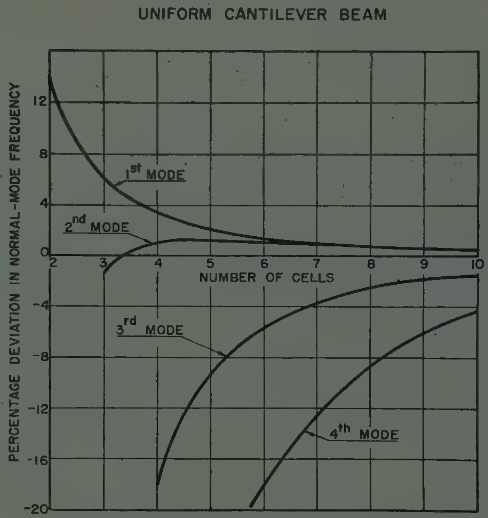


Fig. 14—Frequency deviation for a cantilever beam.

Computer Solution for an 8-Cell Uniform Cantilever Beam

An 8-cell cantilever beam was set up on the electronic differential analyzer using integrator time constants of 0.2 second. Normal-mode frequencies were obtained by driving the cells at anti-nodal points with sinusoidal voltages at the normal-mode frequency. Table IV compares the computer and theoretical normal-mode frequencies. The input resistors used in the circuit for computing differences were calibrated to 0.01 per cent, while

---

[8] S. Timoshenko, "Vibration Problems in Engineering," D. Van Nostrand Co., New York, N. Y.; 1937.

[9] V. S. Haneman, Jr. and R. M. Howe, "Solution of Partial Differential Equations by Difference Methods Using the Electronic Differential Analyzer," AIR-1, Univ. of Michigan Eng. Research Inst.; October, 1951.

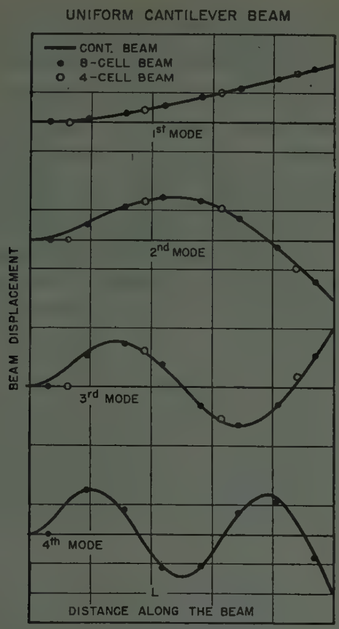


Fig. 15—Comparison of mode shapes for 4 and 8 cell cantilever beam and continuous beam.

the resistors representing flexural rigidity EI and mass per unit length ρ were calibrated to about 0.5 per cent. It was found that a 1 per cent change in one of the input resistors used for taking differences perturbed the period of the fundamental normal mode by the order of 1 per cent.

TABLE IV

Normal-Mode Frequency			
Mode	Continuous Beam	8-Cell Theoretical	8-Cell Computer
1	0.0437 cps	0.0442 cps	0.0436 cps
2	0.275	0.276	0.274
3	0.768	0.750	0.747
4	1.507	1.39	1.37

Computer Solution for an 8-Cell Nonuniform Cantilever Beam

An 8-cell nonuniform cantilever beam was simulated on the differential analyzer. This beam had the configuration shown in Fig. 16 and could represent an aircraft wing with taper ratios of 2:1 in both chord and thickness. Use of the clamped boundary condition implied that the wing mass was small compared with the mass of the fuselage. Two problems were solved:

1. The tapered beam alone; and
2. The tapered beam with the addition of a concentrated load at station 8.

This load simulated a wing tank of half the weight of the wing. A gust load of one-second duration was applied as a force proportional to the chord at each cell. Fig. 17 is a sample of the deflection at station 8, and also shows the one-second gust load. No structural damping was included in these examples, but it can be accomplished by simply connecting the appropriate resistors across the integrating condensers. An integrator time constant of 0.2 second was used.

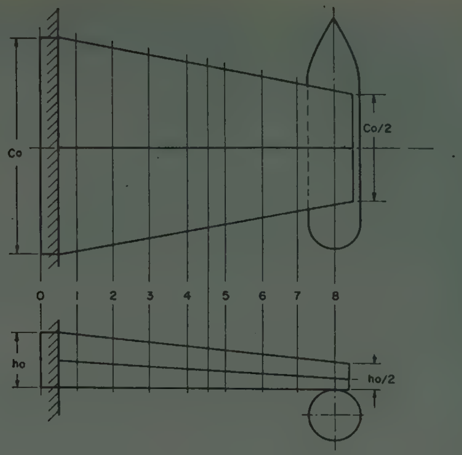


Fig. 16—Non-uniform cantilever beam with concentrated load.

The normal-mode frequencies were obtained for the 8-cell beam with and without the wing tank. These are shown below, in Table V, along with the values for normal-mode frequencies obtained by a differential analyzer solution of the continuous problem.

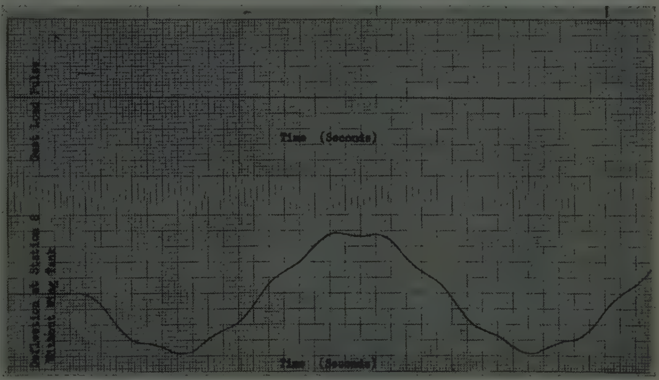


Fig. 17—Sample solution of 8 cell non-uniform beam.

TABLE V

Normal-Mode Frequency			
Mode	8-Cell Continuous	8-Cell Difference	8-Cell Difference
	(No Wing Tank)	(No Wing Tank)	(With Wing Tank)
1	.0773 cps	.0767 cps	.0372 cps
2	.331 cps	.326 cps	.256 cps
3	.820 cps	.784 cps	.709 cps
4		2.016 cps	2.000 cps

In Fig. 18 the moments near the root (station 1) and near mid span (station 4) are recorded for the cases with and without wing tank. For both recordings identical one-second gust loads were applied.

Real-Time Simulation of Beam Structures

One of the advantages of electronic differential analyzers over other types of analog computers is the

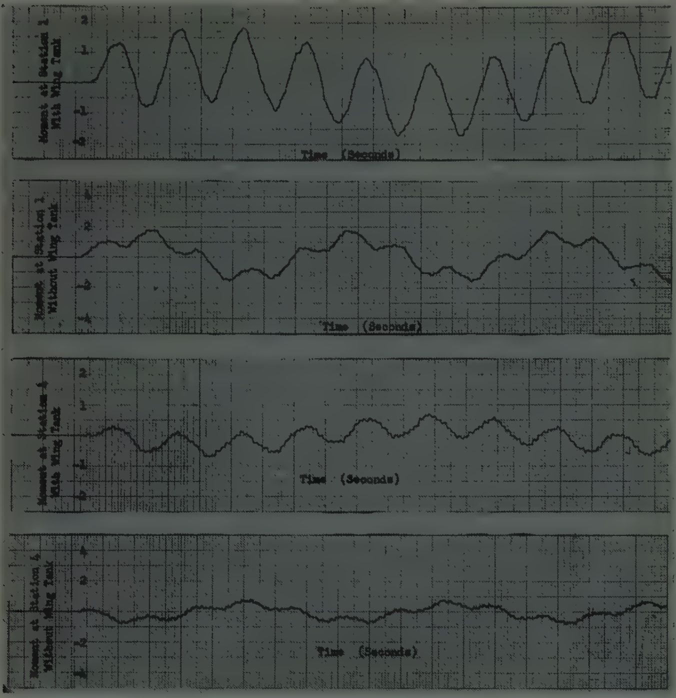


Fig. 18—Comparison of the moments at stations 1 and 4 for the nonuniform cantilever beam with and without the concentrated load.

extreme flexibility of their time scales. For example, it is possible with the analyzer to simulate on a one-to-one time scale the aircraft wing discussed in the previous section. If integrator time constants of 0.02 second are used, the frequency of the fundamental mode for the 8-cell tapered wing becomes 0.77 cps, the order of magnitude of the frequency for an actual structure.

There is one important effect which must be considered when so speeding up the time scale. Limitations in bandwidth of the dc amplifiers may cause the beam oscillations for the higher modes to exhibit a slight exponential buildup in magnitude.[10] However, the introduction of a small amount of viscous damping (considerably less than actually exists in the structure) easily stabilizes the circuit.

A real-time simulation of structural characteristics could be very useful in testing autopilot designs for some of the larger aircraft and missiles, where structural characteristics must be considered in the control problem.

Effect of Small Voltage Transients

The deflection of a beam for a given force is proportional to the fourth power of the length of the beam. Thus as more and more cells are added to the differential-analyzer circuit, the output voltages representing beam deflections become more and more sensitive to voltage inputs. The latter may be purposely introduced to simulate forces, or may be inadvertently introduced as a result of power-supply fluctuations or transient voltages when the initial conditions are released. The sensitivity of the network to such disturbances will increase as the fourth power of the number of cells. With electronically regulated power supplies and dc amplifiers which were manually balanced to within 0.01 volt referred to input, no particular difficulty was experienced with the above effect in solving the 8-cell beam problem.

Summary of Difference Technique for Vibrating Beams

The vibrating-beam equation has been solved with the difference method both theoretically and with the electronic differential analyzer. Results show that normal-mode shapes and frequencies exhibit good agreement with continuous beams providing 3 or more cells per half-wave length of the normal mode are used. Cantilever and hinged-hinged beams have a fixed equilibrium position relative to their surroundings and hence are stable on the electronic differential analyzer. Free-free beams are not supported, however, and will tend to be unstable, since any small voltage unbalance will cause them to rotate and translate as well as vibrate. Damping can easily be included in the beam equation by placing the appropriate resistors across integrating condensers. Any variable force as a function of time can be introduced at any point or points along the beam. The final computer response gives directly the bending moment and the displacement as a function of time and distance along the beam.

This same difference method can be used to solve beams with both torsional and lateral bending.[11] In this case the torsional equation is similar to the wave equation treated in Section III. The proper cross-coupling resistors then tie the two systems together.

* * *

---

[10] A. B. Macnee, "Some limitations of the accuracy of electronic differential analyzers, Proc. I.R.E., vol. 40, pp. 303–308; March, 1952.

[11] McCann and MacNeal, "Beam-vibration analysis with the electric-analog computer, *Jour. Appl. Mech.*, p. 17; March, 1950.

Analog Computing Applied to Noise Studies*

R. R. BENNETT†, ASSOCIATE, IRE

Summary—**Analog computing may be employed to study the behavior of physical systems subjected to random inputs. For linear systems the superposition property permits the incorporation of impulse or frequency response methods of analysis. Nonlinear systems are handled by generating appropriate random inputs and making direct measurements of the behavior of the system model or analog.**

INTRODUCTION

PROBLEMS involving noise arise in many branches of engineering and science. The answers to such problems can usually be expressed only in statistical terms. For example, the designer of automatic control systems is often confronted with system inputs which are combinations of predictable and random functions. Analysis of the behavior of such systems is usually complicated by the fact that they are nonlinear, time-varying, or both. The model or analog approach to such problems, wherein the appropriate inputs are generated and applied to the system analog, is a powerful means for obtaining solutions. This paper is concerned with the application of analog computing to the study of systems subjected to random inputs.

LINEAR SYSTEMS

If the system of interest is linear we may take advantage of the corresponding superposition property. By linear system is meant any system having an input-output relationship which can be described by a linear differential equation. Time-varying systems are thereby included. Any linear system may be characterized by a weighting function, $h(t_2, t_1)$ defined as follows:

> $h(t_2, t_1)$ is the system output, measured at time t_2, in response to a unit impulse applied to the input at time t_1, where $t_2 \geqq t_1$.

The response to an arbitrary input may then be expressed, by superposition, in terms of the weighting function.

In particular, if the input is white noise of spectral density N (measured over positive frequencies only), the mean square ensemble output at time t_2 is given by[1]

$$\widetilde{\overline{V^2(t_2)}} = \frac{N}{2}\int_{-\infty}^{t_2} h^2(t_2, t)\,dt, \qquad (1)$$

where the symbolism of the left-hand side of (1) signifies that the output, V, of a number (theoretically infinite) of identical systems, each subjected to similar noise, is measured at time t_2; the individual measurements are squared and are then averaged over the ensemble of systems.

If the input is stationary noise of spectral density $w(f)$, the mean square ensemble output is given by the known expression

$$\widetilde{\overline{V^2(t_2)}} = \int_0^\infty w(f)\,\lvert H(t_2, j2\pi f)\rvert^2 df, \qquad (2)$$

where

$$H(t_2, s) = \int_0^\infty h(t_2, t_2 - x)e^{-sx}dx \qquad (3)$$

is the Laplace transform of the weighting function. By Plancherel's theorem, (1) is clearly a special case of the latter.

Even though the input noise is not stationary it may still be possible to determine a combination of stationary noise and a linear operator, $k(t_2, t_1)$, which will produce (insofar as the mean square output is concerned) the equivalent of the given noise. This construction is shown in Fig. 1(b). The constructed system, k, is cascaded with h, to form a single weighting function, h', as in Fig. 1(c). The problem thus reduces to the previous one.

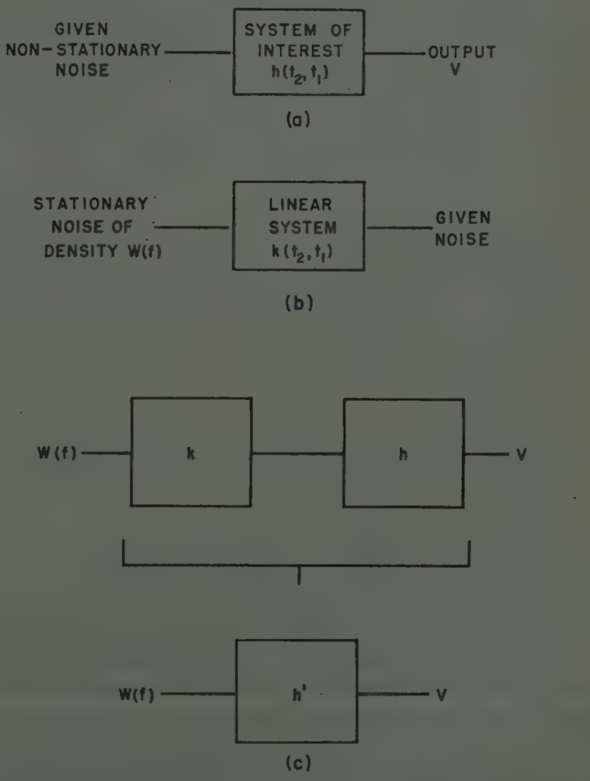

GIVEN NON-STATIONARY NOISE
SYSTEM OF INTEREST h(t₂, t₁)
OUTPUT V
(a)
STATIONARY NOISE OF DENSITY W(f)
LINEAR SYSTEM k(t₂, t₁)
GIVEN NOISE
(b)
W(f)
k
h
V
W(f)
h'
V
(c)

Fig. 1—Representation of nonstationary noise by a combination of stationary noise and a linear operation. (a) Original problem. (b) Replacement of nonstationary noise by stationary noise and linear operator $k(t_2, t_1)$. (c) Reduction of cascaded operators to single operator.

---

* Decimal classification: 621.375.2×R361.211. Original manuscript received by the Institute, February 11, 1953; revised manuscript received July 2, 1953.

† Research and Development Laboratories, Hughes Aircraft Co., Culver City, Calif.

[1] While the mean square output may not be the only quantity of interest it is usually the most significant.

The role of the analog computer is now that of determining the weighting function, since this may be difficult by analytical methods. The most common problem is the one in which the time of measurement or observation, t_2, is fixed; the time of occurrence of the impulse input, t_1, is variable. A valuable computing technique, attributable to Laning and Battin,[2] is available which enables one to compute directly the desired weighting function in terms of the variable t_2-t_1. Associated with the analog instrumentation of this technique is an interesting topological property.

Any linear system may be instrumented by a combination of three types of operations. In terms of analog computing or block diagrams these three operations are shown in Fig. 2(a). They are (a) summation, (b) multiplication by a function of time, and (c) linear constant coefficient operation. By using the same topological system block diagram, but with the direction of flow through each block reversed as shown in Fig. 2(b), we arrive at what may be called the Adjoint System.[3] The input of the original system becomes the output of the adjoint system, and vice versa. The adjoint system has the property that its response to a unit impulse, applied at time t_2, is the desired weighting function. It is necessary to have time run backwards in the adjoint system, and thus laboratory time for the computer instrumented for the adjoint system corresponds to the variable t_2-t_1 of the original problem. This method can often effect a considerable saving in computing time.

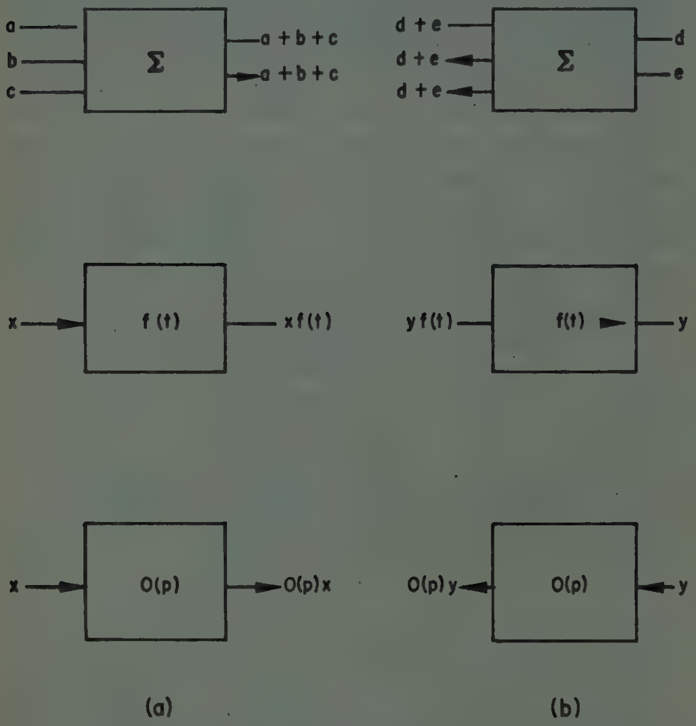


Fig. 2—Construction of Adjoint System used to obtain weighting function. (a) Building blocks of original system. (b) Transformed blocks of Adjoint System.

As an illustration of the adjoint computing technique consider the following circuit problem. An RC network (Fig. 3(a)) has a time-varying resistance whose value is given by

$$R = \frac{1}{1+t}.$$

At time $t=0$ switch S is closed. Consider the time of observation or measurement in this case to be $t=t_2=1$ sec. That is, a measurement is made across C one second after the switch is closed.

The value of the output, e_0, at this instant can be obtained by appropriately weighting the values of the input, e_i, during the interval $0 \leqq t \leqq 1$. Thus, in this problem t_1 takes on values between zero and one second.

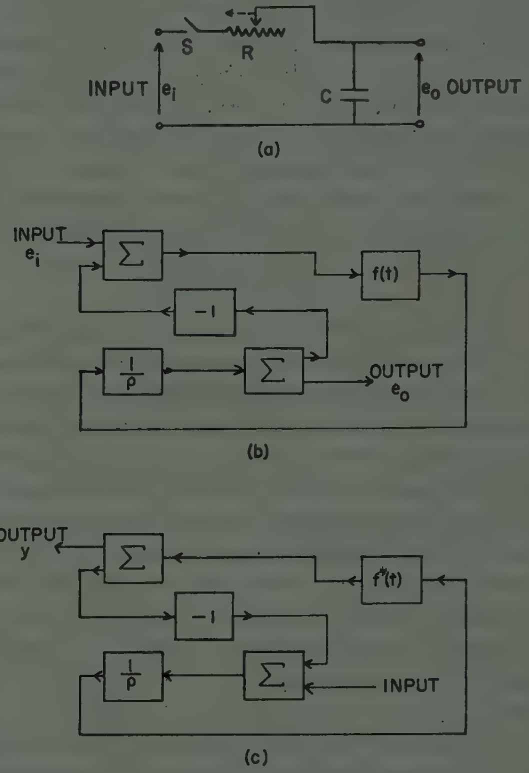


Fig. 3—Example of use of adjoint computing technique. (a) Time-varying circuit example. (b) Typical analog computer instrumentation for circuit. (c) Adjoint computer arrangement obtained from (b) by reversing direction of flow through individual blocks.

A typical analog computer instrumentation for the circuit of Fig. 3(a) is shown in Fig. 3(b). (The value of C is taken to be unity.) The multiplying function $f(t)$, is given graphically in Fig. 4(a). Using the arrangement of Fig. 3(b) one could determine the appropriate weighting function by applying an impulse to the input (or better by starting the integrator with the proper initial value) and measuring the output at time $t=1$ sec. It would of course be necessary to repeat this computer operation many times. Each time the input impulse would be injected at a different instant, corresponding to t_1 having a sufficiently large number of values in the range $0 \leqq t \leqq 1$.

---

[2] J. H. Laning, Jr., and R. H. Battin, "On an Application of the Use of Analogue Computers to Methods of Statistical Analysis." Project Cyclone Symposium II, Reeves Instrument Corp., New York, N. Y.; 1952.

[3] So called because the differential equation describing this rearranged system is the mathematical adjoint of the equation representing the original system.

The adjoint system for this example is given in Fig. 3(c). It is obtained from Fig. 3(b) by simply reversing the direction of flow through each of the blocks. As pointed out above, the input and output of the adjoint system are reversed from those of the original computer diagram. The multiplying function, here denoted by $f(t)$, is shown in Fig. 4(b) plotted versus adjoint Iomputer time, t^*. If the computer circuit of Fig. 3(c) is supplied with a single unit impulse at $t_1 = 0$ the output, y, will be the curve of Fig. 4(c), which is precisely the desired weighting function in its entirety. Thus, in one operation of the computer we have obtained what took several operations using the arrangement of Fig. 3(b).

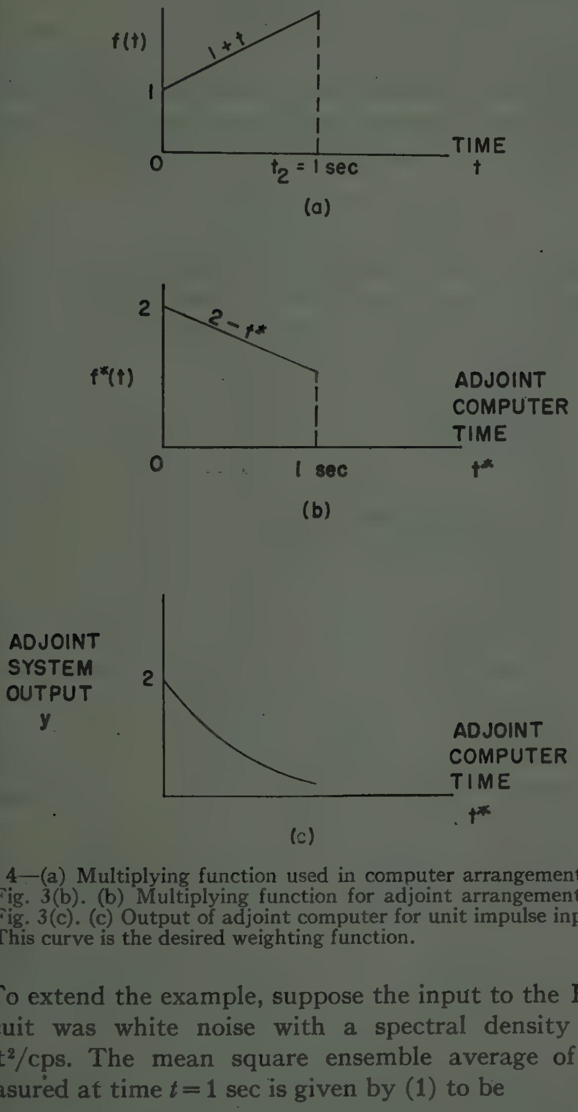


Fig. 4—(a) Multiplying function used in computer arrangement of Fig. 3(b). (b) Multiplying function for adjoint arrangement of Fig. 3(c). (c) Output of adjoint computer for unit impulse input. This curve is the desired weighting function.

To extend the example, suppose the input to the RC circuit was white noise with a spectral density N volt²/cps. The mean square ensemble average of e_0 measured at time $t = 1$ sec is given by (1) to be

$$\widetilde{[e_0|_{t=1}]^2} = \frac{N}{2}\int_0^1 y^2 dt^* \text{ volt}^2.$$

This integration operation can of course be accomplished automatically in the computer.

NONLINEAR SYSTEMS

For nonlinear systems in general it is necessary, when attempting to find the response to statistical inputs, to generate the appropriate inputs and apply these to the analog. It follows that the measurements taken from the analog will exhibit a statistical character. It is important that the significance which can be attached to a set of such measurements be fully understood.

If a complete time history of the variables of interest is desired, the usual recording methods common to analog computer operation are applicable. If, however, the values of the variables at a specific instant are desired, it is expeditious to record only those values. A storage scheme may be used to retain the answers of interest until the end of the problem. It is also economical to provide some automatic means for repeating solutions on the computer. The only difference between the successive solutions is that a different sample of noise or random input is applied each time. Mathematically, the form of the equations is the same each time; the forcing functions, initial conditions, and certain parameters vary randomly from solution to solution. The statistical measure now consists of an ensemble measure over the possible solutions of the same transient problem.

Random Inputs: The random inputs to the analog computer correspond to the various qualities of the problem of interest which are statistical in nature. These may be of various types. Perhaps the most common type of input is a noise voltage which varies with time. Such noise might represent, for example, tube noise in a radar system. A random initial condition may be considered an input. A parameter, such as system gain, which is constant during a single sequence of the system's operation, may vary randomly from solution to solution. Or, a combination of the foregoing may exist in a single system.

An example of a system experiencing both random initial conditions and a random-forcing function is shown in Fig. 5. In the electron tube shown electrons leave the gun in a random direction, representing a random initial condition. Subsequently each electron passes between two deflection plates where it experiences a force-versus-time which is of the nature of random noise. The result of interest in this example is the deflection, y, of the electron at the instant it reaches (or passes above or below) the target electrode. Examining the deflections of a large number of electrons then constitutes the desired statistical study.

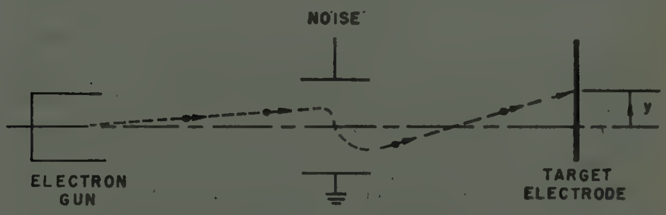


Fig. 5—Electron tube model.

An earlier paper cited means for generating random forcing functions.[4] In particular, a noise generator was described which gave an output having constant spectral density at low frequencies and a normal or gaussian amplitude distribution. Methods for converting this noise to other forms were mentioned.

In analog computers it is common to instrument an initial condition as the initial charge on a condenser. If the initial value is normally distributed from solution to solution, the appropriate charge can be obtained by momentarily connecting the condenser to the output of a noise generator before the problem begins. Of course proper allowance must be made for the magnitude of the noise. And, if the initial condition has a mean value a corresponding dc voltage must be added.

While a normal or gaussian distribution is common in nature, it may be necessary to simulate an initial condition which has some other distribution. This may be done by passing the available gaussian noise through a function generator (a device, common to analog computers, whose output is an arbitrary function of the input) such that the output of the function generator has the desired distribution. The problem here may be stated as follows: Given an available noise voltage, x, which is normally distributed with a probability density $p_1(x)$, what functional relationship is necessary to produce a voltage $z=f(x)$ which has an arbitrary distribution given by $p_2(z)$? By making the mean value of each distribution zero (a mean other than zero is handled by simply adding the required dc voltage), a simple, though not unique, solution is to choose

$$\int_0^x p_1(x)dx = \int_0^z p_2(z)dz. \tag{4}$$

Fig. 6 shows the generation of a uniform distribution, $p_2(z)$, also common in nature, from the normal distribution $p_1(x)$. The functional relationship $z=f(x)$, shown graphically, can be seen to squeeze the high values of x down to values slightly less than a, the maximum value of z.

A coefficient in a differential equation can be made random from solution to solution by employing a multiplying device. Before the problem solution begins a condenser is charged by a noise generator, in the same fashion as was mentioned in connection with random initial conditions. The condenser voltage is then used to supply one input of the multiplier. The other input is the variable which is to be multiplied by the random coefficient. As suggested by the previous paragraph, the probability distribution of the coefficient may be made arbitrary.

Measurement Theory: The number of solutions or runs which must be carried out to obtain a given accuracy for the result may be calculated by known statistical methods. For example, if the distribution of the successive values of a particular variable, picked off at a specific instant over a number of runs, is approximately gaussian the limits of confidence for the result may be simply obtained. Let these successive values be $y_1, y_2, \cdots, y_N$.[5] That is, there are N total solutions to the same problem, each having a different sample of input. We introduce the measured mean,

$$y = \frac{y_1 + y_2 + \cdots + y_N}{N},$$

the measured mean square value,

$$\overline{y^2} = \frac{y_1^2 + y_2^2 + \cdots + y_N^2}{N},$$

and the measured standard deviation,

$$\sigma = \sqrt{\overline{y^2} - \bar{y}^2}.$$

Then, for a reasonably large number of runs, the measured value of the standard deviation will lie within the range

$$\sigma_0 \pm \frac{2\sigma}{\sqrt{2N}},$$

where σ_0 is the "correct" value, with 95 per cent confidence.[6] Correct value here means the value which

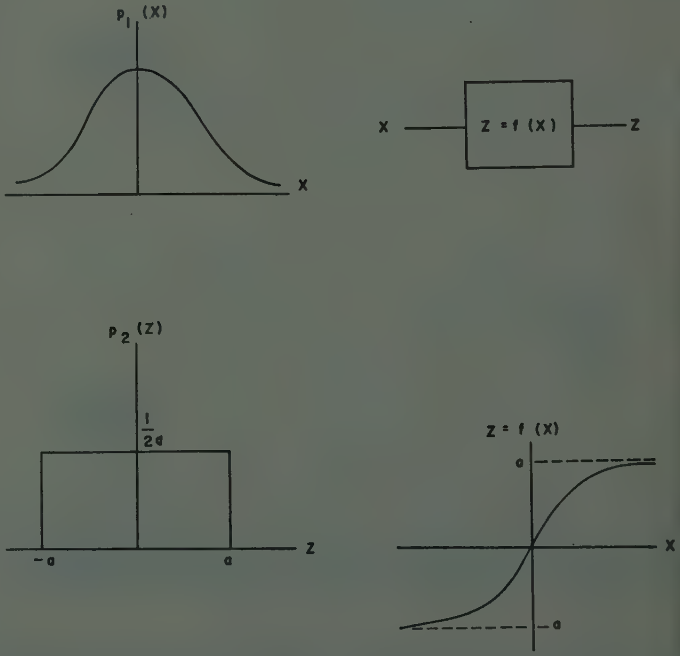


Fig. 6—Generation of uniform probability distribution from gaussian distribution.

---

[4] R. R. Bennett and A. S. Fulton, "The generation and measurement of low frequency random noise." *Jour. Appl. Phys.*, pp. 1187–1191; Sept., 1951.

[5] It is assumed here that the successive values are independent. They might represent the deflections of successive electrons in the example of Fig. 3. Independence would result if the successive electrons were spaced apart in time over a time interval which is long compared to the reciprocal of the bandwidth of the noise voltage on the deflection plates. Independence of the directions in which successive electrons leave the gun would also be necessary.

[6] H. Cramer, "Mathematical Methods of Statistics," Princeton University Press, Princeton, N. J.; 1946.

would be obtained for an infinite number of runs. The 95 per cent confidence signifies that the measured value of the deviation will fall within the above limits 95 per cent of the time, on the average. (That is, there is one chance in twenty, on the average, that σ will lie outside this range.) A confidence level of 95 per cent is of course arbitrary. However, it has an intuitive appeal for most engineering problems. Similar limits may be calculated for any desired level of confidence.

With 95 per cent confidence the measured value of the mean, $\bar{y}$, will lie within the interval

$$\bar{y}_0 \pm \frac{2\sigma}{\sqrt{N}},$$

where $\bar{y}_0$ is the "correct" mean.

By way of example, suppose 100 runs are made. Suppose, further, that the average (measured mean) of the variable y, averaged over the 100 runs, is 5 cm and the measured standard deviation is 1 cm. We may then assert, with 95 per cent confidence, that the correct value of the standard deviation lies in the range

$$1 \pm \frac{2}{\sqrt{2 \cdot 100}} = 1 \pm .14 \text{ cm},$$

or between 0.86 cm and 1.14 cm. The correct mean lies, with the same confidence, between 4.8 cm and 5.2 cm. If this degree of uncertainty in the result is not tolerable, the only alternative open is to make more runs.

It is to be noted that the accuracy obtainable increases as only the square root of the number of runs, N. Apparently, then, a compromise must be made between desired accuracy and time consumed in obtaining the solution. For many engineering problems 100 runs are sufficient to form a basis for judgment. Indeed, the length of time required for statistical studies on an analog computer makes operation at speeds greater than those corresponding to real time seem desirable.

Another type of measurement may be illustrated by referring again to the electron tube example of Fig. 5. Suppose that only a fraction of the electrons strike the target electrode, and suppose, furthermore, that this fraction is the quantity of interest. By obtaining a large number of solutions and counting those solutions which yield a value of y corresponding to a hit an estimate of this fraction is obtained.[7] We now desire to know the statistical accuracy of this estimate.

Fig. 7 gives the limits of accuracy which can be expected for such a measurement. This particular plot is for 100 solutions and a confidence level of 95 per cent. Suppose that by observation of 100 solutions it is found that 40 of them indicate an electron striking the target electrode. The measured probability of hitting is thus 0.4. From Fig. 7 the correct value (for an infinite number of solutions) lies, with 95 per cent confidence, between 0.3 and 0.5.

The curve of Fig. 7 is not restricted to a gaussian distribution; it is applicable to any distribution. Furthermore, it is clearly applicable to a measurement involving any number of dimensions. That is, the target electrode of the example could be two- or three-dimensional. A fourth dimension could be included by considering those electrons which strike between time t_1 and time t_2. The number of dimensions may be extended indefinitely.

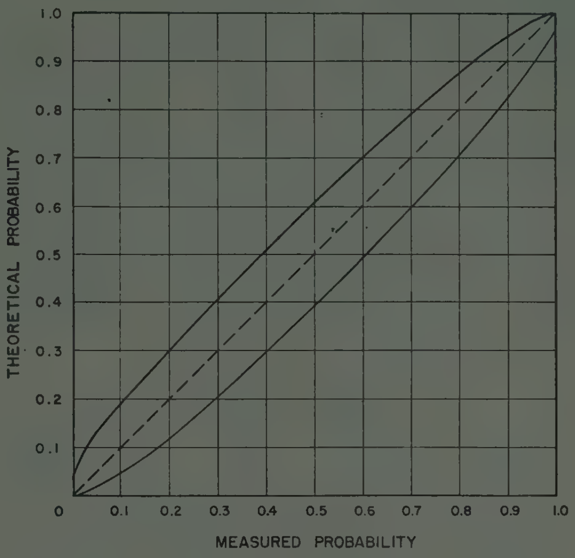


Fig. 7—Ninety-five per cent confidence limits for measured probability. Sample size of 100. (Values taken from W. J. Dixon and F. J. Massey "Introduction to Statistical Analysis," McGraw-Hill Book Co., New York, N. Y.; 1951.)

While Fig. 7 is for 100 samples and 95 per cent confidence, similar curves may be constructed for any sample size and confidence level. For N greater than 100, and for the same confidence, the displacement of the boundary curves of Fig. 7 from the dotted line is given approximately by multiplying the displacement shown by $10/\sqrt{N}$.

The foregoing theory of measurement by no means exhausts the methods applicable to the interpretation of analog computer results. The reader may consult standard texts and reference works for additional material.

Recording: It is desirable to record not only the individual results of analog computer solutions to problems involving noise but also certain combinations of results. For example, the mean and mean square values of an ensemble of solutions may be of interest. There are available a number of automatic schemes for accomplishing this. Rapidity in obtaining combinations of results is important in those exploratory studies which base a choice of parameters upon the previously obtained answer.

Conversion of the output of an analog computer to digital form provides a convenient means for manipulating combinations of solutions.

---

[7] Independence of the successive solutions is again assumed.

Economic Analogs*

OTTO J. M. SMITH†, SENIOR MEMBER, IRE

Summary—**Each type of electronic analog has a use in the solution of a set of economic problems. The large, general-purpose analog computer can solve dynamic-unilateral systems. This can be used for the analysis of a single business, the analysis of an industry, or the study of the economy as a whole. It is hoped that analogs of this type will be used to analyze the effects of proposed governmental budgetary policies, legislation, and regulations, which will have economic effects. The analog of international trade is a decision-function network which has many points in common with automobile and communication traffic control. Large machines for solving *n*-equations in *n*-unknowns can be used for linear-static problems such as the determination of average production levels in a large number of interrelated industries. This latter analog is relatively in accurate and is sensitive to the accuracy of the input data. Small scale, specific-purpose analogs can be built for a large variety of isolated dynamic problems, such as the determination of the best ordering rate for a small-retail grocer, and the design of the optimum ratio of inventory capacity to production capacity in a small-proposed business. The effect of statistical fluctuations can be most easily observed by using an analog with a noise generator.**

INTRODUCTION

THERE HAS BEEN a great surge of interest in the use of electrical models or computers for the solution of economic problems. Models of this sort are useful for both the practicing economist and the research theoretician. In the first place a model may allow one to predict the nature of the resultant change in an economic system due to the introduction of changes such as price controls, cost-of-living increases, a different tax schedule, a different business policy, or governmental regulations. A model of an airlift or any other type of economic activity can be set up in such a manner that the optimum utilization of available funds can be seen.

The other use of models is for testing hypotheses. One can formulate an explanation, or an hypothesis, concerning our economic system, and from this hypothesis derive equations describing the nature of the economy in which we live. But usually these equations are so difficult to solve that it is not possible to state definitely whether or not the hypothesis corresponds with reality. By using models one can construct an economic system corresponding to any hypothesis and compare the response of this system to the known responses of the actual economy. In such a manner some estimate can be made concerning the validity of the assumed hypotheses. No attempts will be made to classify all the different types of economic problems and the kinds of models which could be built for them, but a few of the simpler problems and the electronic analogs which have already been built for them will be discussed.

Thinking in terms of how an analog will behave is also very valuable, even if no analog is built. It leads the economist into the fields of vector diagrams, Laplace transforms, stability of closed-loop systems, noise saturation, and stabilizing networks. It points to the many advantages of running frequency-response and white-noise tests.

LINEAR STATIC UNILATERAL ANALOG

Many economic problems fall into the form of *n* equations in *n* unknowns. For example, the price of beans might be a function of the price of cans, the cost of cannery labor, the cost of farm labor, the weather during the previous year, the interest rate, and so forth. Since many of the factors entering into the price of beans are in themselves economic factors, this problem becomes one of solving for a large number of prices given a large number of parameters, including the rates of change of one price with respect to another.

A macroeconomic problem of the same type is the static description of the economy as an interlinked sequence of production processes, each requiring part of the outputs of several other factories, and in turn its output being required by other factories or providing consumer goods. This is *n* equations, where the variables are the quantities produced by each factory and the parameters are the amounts of steel, cobalt, labor, and so forth, required per unit output of a factory. If a consistent solution exists where all the variables are positive, the system as a whole is productive.

The analog for this is a large number of voltage sources, each representing the production rate for one commodity. For each production process there is a linear equation which can be put in the form of the sum of different proportions of component voltages adding to zero. The parameters are potentiometer settings; the production components are the potentiometer currents when they are connected to the appropriate input voltages. The potentiometer currents are added in *n* different current indicators, and the solution is obtained by a systematic trial and error adjustment of the voltages until all of the current indicators read zero. Inputs and outputs are represented by currents of opposite polarity, so that all voltage sources have to be center-tapped.

This is essentially the inversion of an *n*-order matrix. By the use of unilateral amplifiers, the trial and error feature can be eliminated. The output commodity in each equation can be solved for, and would be the amplifier input current. Each amplifier provides the voltage drive for the following processes. In this form, dynamic elements like production-time delays and inventory-storage capacities can be introduced.

---

* Decimal classification: 621.3752×388×R143. Original manuscript received by the Institute, December 29, 1952.

† Department of Engineering, University of California, Berkeley, Calif.

Another way in which this analog can be used is to determine the parameters of the economy, *i.e.*, the rates of change of one variable with respect to another, or the potentiometer settings, given several sets of prices in the economy.

At this point a distinction should be made between two possible types of analogs; the one just described is a unilateral (or cause-and-effect) analog, that is, the power flows from the voltage sources to the current indicators but cannot flow in the opposite direction. This is an analog wherein each part represents a particular transference equation for the economic system. A bilateral analog would be an *n*-loop electrical network wherein the entire network represents the entire economic system. Now, the parameters in the bilateral network are not the same as they are in the unilateral network. Take, for example, the rate of change of the price of beans with respect to cannery labor cost. The economy is a closed-loop system, and the change in the price of beans will eventually reflect back on the cannery labor cost. One can not say which is cause and which is effect, because each performs both functions. There are in reality two transferences, one directly from labor to beans, and the other through the entire network back from the price of beans to the cannery labor cost. Therefore the measured rate of change of the price of beans with respect to cannery labor cost on the actual economy is a closed-loop parameter, and is not the value or values to be used in an equivalent open-loop or unilateral-type analog. This is an important point, for some economists make the mistake of using closed-loop parameters as though they were measured on an isolated, unilateral sample of the economy, wherein the cost of cannery labor influenced only the price of beans, and this were isolated from the rest of the world. Since only the closed-loop parameter is known, one can use an analog to determine the correct value of the open-loop parameters. This is done by adjusting the unilateral analog potentiometers with unloading amplifiers in a trial and error manner until the changes in labor cost and the magnitude of the labor cost will produce the correct amount of change in, and magnitude of, the cost of beans with the entire system operative. In this manner every parameter of the system can be corrected for the change from the measured closed-loop value to the constructional open-loop value. Each resultant parameter magnitude tells the economist how much is direct cause and effect, and how much system feedback.

DYNAMIC BILATERAL SYSTEM

An electrical network including capacitances and inductances, or electronic integrators and differentiators, can be made to represent a dynamic bilateral economic system. The classic example of this is the study of inventory oscillations. Consider a factory producing goods which are stored in inventory and eventually sold. If the inventory should diminish there would be a short delay before the new production rate necessary to replenish the inventory is established. If the inventory should become excessively great there would be a short delay before the marketing branch could adopt a new price schedule, and increase its sales. Very crudely, then, the inventory could be represented as in Fig. 1, as a capacity C where coulombs represent the quantity of goods.[1] C is charged up through a production inertia inductance L_2 from a battery E_2, and discharged through a marketing inertia inductance L_1 into a circuit representing the consumers' price demand characteristic.

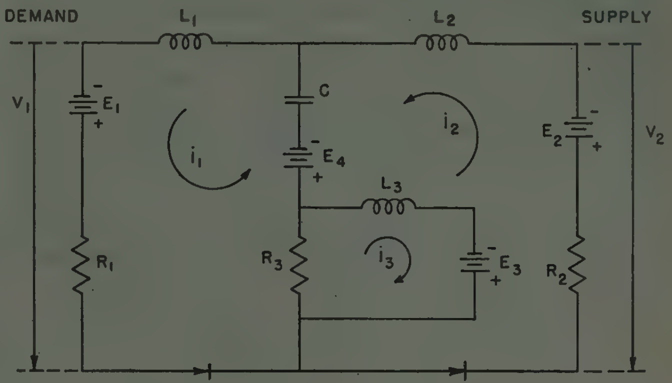


Fig. 1—Bilateral inventory analog. From "Analog Computing Techniques Applied to Economics," by Strotz, Calvert, and Morehouse.

The consumer-demand price versus sales rate is approximated linearly by E_1, the apparent maximum price at zero sales rate; R_1, the rate of decrease of price necessary to increase the sales rate; and E_1/R_1, the apparent maximum sales rate at zero price. The production-supply price versus sales rate is approximated linearly by E_2, the necessary price for zero sales rate, and R_2, the rate of increase of price with sales rate. (For all businesses where efficiency increases with production, R_2 must be negative.) In this analog, voltage is price per unit, current is sales rate in units per time, power is dollar value rate, charge is product quantity, and energy is total dollar value.

Since E_1 is larger than E_2, it can be seen that the source of energy (or dollars) for this economic system comes from the consumer. The diodes permit dollars to go from consumer to producer, but not in the opposite direction. A biased diode in the inventory branch can be used to prevent the inventory from going negative. This system is linear except for transients so large that the inventory goes to zero, the production rate reaches saturation, or the production or sales rate goes to zero. Tests for stability on the linear system are adequate, because the nonlinearities contribute slightly to stability, although they subtract from economic efficiency.

DYNAMIC UNILATERAL SYSTEM

The unilateral analog consists of a set of amplifiers which can be connected either as buffers to lower the impedance, as nonlinear function generators, or as feedback integrators or differentiators. They are used in exactly the same manner as in the solution of servomechanism problems with an analog computer. In the case of inventory and production-rate oscillations, one input to the system is the desired inventory level which is determined by business policy (see Fig. 2). From this is subtracted the actual inventory level and the error is amplified by the production-scheduling-policy-decision amplifier. The output specifies the production rate which passing through a time delay is integrated to give the goods component, which is added to the inventory level.

---

[1] See Bibliography reference 10.

The price-supply curve is a voltage source with nonlinear internal impedance which drives the demand-price curve, another voltage load with a nonlinear internal impedance. The sales rate and price exists at the terminals of these two units—the sales rate is integrated and subtracted from the inventory quantity. The sales price is multiplied by the rate, integrated, and goes into the profit computer. The production rate is integrated and subtracts from the raw-materials inventory, which causes a deviation between the desired raw-materials-inventory level and the actual level. This deviation actuates the amplifier representing the ordering of new raw materials. The ordered raw materials are delayed in delivery by an electronic-delay network, and the output of this network is integrated and added to the raw materials inventory.

Both the bilateral and the unilateral dynamic analogs show clearly the type of inventory oscillations which are commonly observed by economists. Furthermore, it is easy to determine the effect upon inventory stabilization of the variation of different parameters in the analog. As in servomechanisms, particular attention has to be given to excessive time delays, and wherever possible a prediction of future trends, or the introduction of phase-lead networks which utilize the rates of changes of signals, is very desirable. Also, as in servomechanisms, one must beware of too much of a good thing. The improper use of trend predictors or phase-lead networks will increase the system-frequency response so greatly that high frequency noise will be magnified by the system, and the inventory variations become random at a high frequency. Excessive gain due to overzealousness on the part of the manager can result in sinusoidal oscillations at the low-resonant frequency given by the production delay and inventory time constant.

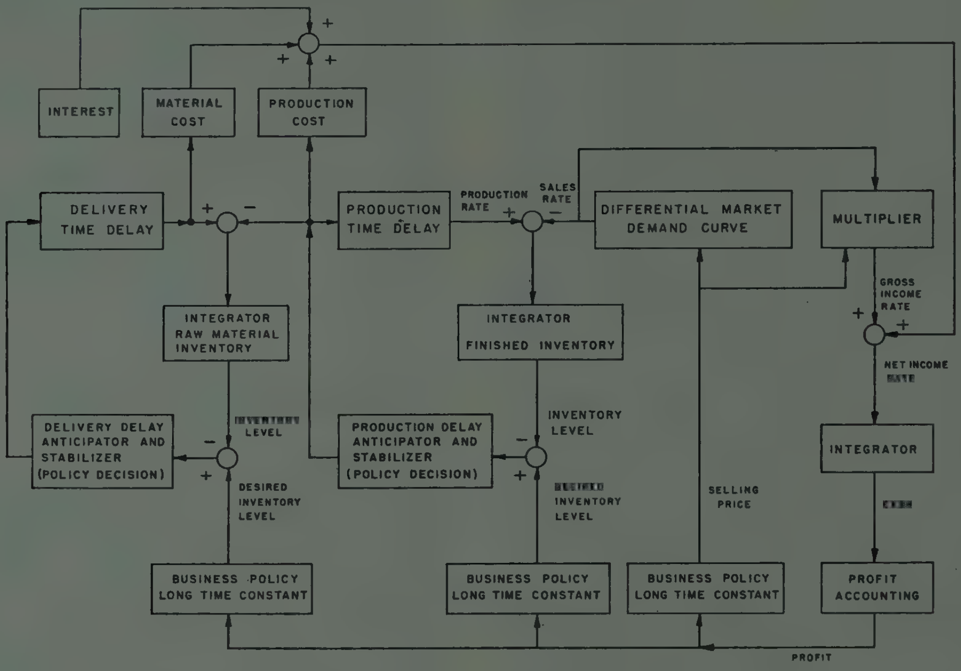

INTEREST
MATERIAL COST
PRODUCTION COST
DELIVERY TIME DELAY
PRODUCTION TIME DELAY
PRODUCTION RATE
SALES RATE
DIFFERENTIAL MARKET DEMAND CURVE
MULTIPLIER
INTEGRATOR RAW MATERIAL INVENTORY
INTEGRATOR FINISHED INVENTORY
GROSS INCOME RATE
NET INCOME
DELIVERY DELAY ANTICIPATOR AND STABILIZER (POLICY DECISION)
LEVEL
PRODUCTION DELAY ANTICIPATOR AND STABILIZER (POLICY DECISION)
INVENTORY LEVEL
DESIRED INVENTORY LEVEL
INVENTORY LEVEL
SELLING PRICE
INTEGRATOR
BUSINESS POLICY LONG TIME CONSTANT
BUSINESS POLICY LONG TIME CONSTANT
BUSINESS POLICY LONG TIME CONSTANT
PROFIT ACCOUNTING
PROFIT

Fig. 2—Unilateral production analog.

The analog shows that the purpose of the inventory is two-fold. Statistical variations in the sales rate should be smoothed out by the inventory. The set point should be approximately half of the capacity for maximum usefulness. A high-gain feedback system around a pure production time delay can be stabilized only with a cascade time constant many times greater than the production delay. The production-scheduling policy and the inventory capacity provide this stabilizing time constant (mid-frequency attenuation).

This problem can be set up on any of the general purpose analogs like the BEAC, REAC, EASE, or GEDA. Production rates and sales rates can be prevented from going negative with diode clippers. Inventories are prevented from going negative by relays which change from inventories normally controlled by sales to sales fixed by production when the inventory reaches zero. Oversupply also actuates a relay to change the inventory cost and the sale-price computer.

Another type of analog is the representation of the macrodynamic features of our economy. The basic features of the macrodynamic economy were described by Kalecki in 1933, and enlarged upon by Keynes in 1935 (see Fig. 3). There is a production plant which manufactures all capital goods, the input being an investment rate, and the output being the delivery of goods at some average time later and a contribution to the national income because of the purchase of raw materials and the payment of wages during the production interval. The delivered goods go to replace depreciated capital goods, and to increase the capital goods on hand; that is, they are integrated and added to the capital goods remaining on hand. The portion of national income from the production of capital goods is added to the portion of national income from the production of consumers' goods. The total national income influences the rate of consumption, for as wages rise people spend more; therefore, there is a small positive-feedback loop with a gain less than one which goes from total national income back to the proportion of national income due to consumption. The investor attempts to maximize profit and his actions may be represented by a simple investment formula, *i.e.*, investment rate increases as the national income goes up, because there is a greater expectation of profit during times of high national income, and investment rate decreases as the total capital goods on hand increases, because there is less expectation of a market for new capital goods when the country already has a considerable quantity on hand.

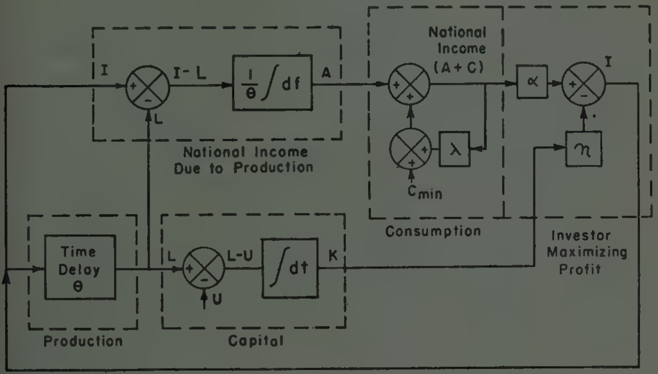


Fig. 3—Macrodynamic capital production analog.

This complete set of relationships, shown in Fig. 3, has been represented by attenuators, unloading amplifiers, integrators and adders. After this system was set up for an analog computer it was tested open-loop by opening the circuit at the investment-rate point and measuring its loop characteristics, using ordinary frequency-response techniques. It was predicted and shown experimentally that the system was unstable, for all of the parameters of our economy were set in from a knowledge of the average production delay, the consumption time constant and the depreciation time constant. With these parameters it was shown that the closed-loop system oscillated continuously at a period of ten years. It was also shown that any attempt to stabilize this system by the imposition of regulatory means was almost doomed to failure. Whatever the regulatory means that are proposed—whether legislative or by government manipulation of tax scales, permissible investments, subsidies, government contracts, and so forth—the investor is aware of these conditions and adopts a new function for maximizing profit. This new function is essentially a separate, negative-feedback closed loop and performs the function of almost completely cancelling out the effect of the proposed regulatory means.

The amplitude of oscillation in an unstable-linear analog has no meaning, for it increases until the amplifiers saturate. The hypothesis of an economic nonlinearity, and its addition to the system using biased-diode function generators, will give oscillation amplitudes with a meaningful dollar value. Transients in a system as lightly damped as this one will last for many cycles. In other words, the transient introduced by World War I is still essentially undamped. One cannot say that World War II was a new transient in the system. Rather it was the system response on the output of a significant discontinuity due to the superposition of the previously introduced transients. The discontinuity is a change in one or more of the system parameters which occurs suddenly as a function of the instantaneous amplitude of the oscillation. This discontinuity introduces power into the system and tends to maintain a relaxation type of oscillation.

DECISION FUNCTION NETWORK

Another type of economic system is the representation of international trade or the flow of goods from a large number of producers as, for example, milk from farmers, to a large number of consumers as, for example, city dwellers. This type of system consists of a price supply curve for each producer represented by a battery voltage and a series resistor, a price demand curve for each consumer represented by another battery and series resistor, and a transportation cost which links the two. The transportation cost is some minimum possible regardless of quantity, plus an increase in cost which is incremental with quantity. The transportation analog consists of two biased diodes back to back which will not carry current in either direction unless the price at one locality exceeds the price at another locality by more than the minimum transportation cost. The rate of flow of quantity of goods between the two points is represented by current. There are resistors in series with each biased diode to generate the incremental transportation cost. This type of analog will allow one to compute a variety of problems in international trade, and to compute the optimum distribution of individual goods produced and sold throughout the United States. Since many sales contracts and selling agreements cannot be cancelled at a moment's notice, there is a lag in the shift of goods from one market to another in case the demands or prices in the markets change. These lags can be represented in the decision function network by means of energy storage elements, series inductances for lags in sales rates, and capacitors for inventories, which perform the function of giving delays in the price schedules following changes in factors contributing to changes in price schedules.

All the sources are connected to all the consumers through transportation elements, and the most significant static results are the determination of which diodes are open and which are closed.

NOISE

If one looks at a chart of closing quotations on the stock market, or the Dow-Jones Industrial average, the national debt, or almost any chart which would appear in an economic journal, he is immediately struck by the fact that the chart shows a large component of high-frequency random noise. Almost all economic systems have a large component of random variation which the servo man calls noise. They are not noise saturated, for they do not drive from full production to zero production at these high frequencies. There is a definite need for the design of the stabilizing loops in economic systems, (*i.e.*, the business-policy decision loop), from the viewpoint of discriminating against the random noise inputs. It is profitable to be able to predict future values of curves of national debt, interest rate, and expected sales in the same manner that a radar computer extrapolates the statistically most probable future value for an input curve with a large proportion of high-frequency noise. In other words, the economist needs to think in terms of power-density spectra and transfer functions when he talks about business policy decisions. The economic system can be designed to maximize profit in the same manner as a servomechanism is designed to minimize error power. For this purpose, a low-frequency noise generator should be provided with the analog. If one is not available, an approximation can be achieved by performing a number of tests in different frequency bands, using a fixed frequency whose amplitude is equal to the rms value of the noise in that frequency band.

SPECIFICATIONS

A dynamic unilateral analog computer to be most useful for economic problems needs to have several additional components which occur only infrequently in engineering problems. One is a "dead time" or transmission-line type of delay, as distinguished from RC time constants. This is useful for production and transportation delays. One form is a magnetic drum with adjustable recording and playback heads, using pulse length modulation at a high repetition rate. Another useful component is a relay-operated discontinuity to keep real quantities positive. This is similar to the analog for position limiting.

Diodes for keeping production rates and sales positive are easily introduced externally on general purpose analogs, and biased-diode function generators and multipliers are now commonly available.

CONCLUSION

Although only a few specifically economic analogs have so far been built, and it is unlikely that many businesses can afford a general purpose unilateral analog computer, still, the analog techniques are very valuable to an economist because they give him a tool for thinking. They direct his analysis of a problem in the correct manner. One finds a number of articles in *Econometrica* now which use the Nyquist criteria for stability, and one can find vector diagrams for economic systems which look surprisingly like problems in positional control. In other words, economists now recognize that economics is a study of closed-loop, nonlinear, dynamic systems and as such they need to use exactly the same tools which servomechanisms and system-design men are now using. These analogs will not make it any easier for the economist to get the data necessary for a satisfactory analysis, but they will point up to the economist what type of data he should measure on the economic system in order to get the most useful and fruitful results.

BIBLIOGRAPHY

Economic Analogs

1. M. Kalecki, "A macrodynamic theory of business cycles." *Econometrica* (Chicago, Ill.), pp. 327–344; July, 1935.
2. H. F. Erdley, "Business Cycle Stability from an Electrical Analog of an Economic System," M.S. Thesis, University of California, Berkeley, Calif.; June, 1950.
3. W. T. Newlyn, "The Phillips/Newlyn hydraulic model," *Yorkshire Bull. Economic and Social Research*, vol. 2, pp. 111–127; July, 1950.
4. A. W. Phillips, "Mechanical models in economic dynamics," *Economica*, n.s., vol. XVII, pp. 283–305; August, 1950.
5. H. A. Simon, "An Exploration Into the Use of Servomechanisms Theory in the Study of Production Control," Cowles Commission Discussion Paper, Economics Number 288, University of Chicago; August 17, 1950.
6. N. F. Morehouse, R. H. Strotz, and S. J. Horowitz, "An electro-analog method for investigating problems in economic dynamics: inventory oscillations," *Econometrica*, (Chicago, Ill.), vol. 18, pp. 313–328; October, 1950.
7. S. Enke, "Equilibrium among spatially separated markets: solution by electric analog," *Econometrica* (Chicago, Ill.), vol. 19, pp. 40–47; January, 1951.
8. O. J. M. Smith, "Electronic Analog for an Economic System," I.R.E. Conference Paper, Seattle, Wash.; June, 1951.
9. W. R. Fair, "An Analog Computer for Testing Business Policies," Electrical Engineer's Thesis, University of California; June, 1951.
10. R. H. Strotz, J. F. Calvert, and N. F. Morehouse, "Analog computing techniques applied to economics," *Trans. AIEE*, vol. 70, part I, pp. 557–563; 1951.
11. F. S. Lee, "The History of Economic Analogs," EE 200 Paper, University of California Engineering Library; February, 1951.
12. O. J. M. Smith and H. F. Erdley, "An electronic analogue for an economic system," *Elec. Eng.*, vol. 71, no. 4, pp. 362–66; April, 1952.
13. B. S. Golosman, "The History of Electrical Economic Analogs," EE 200 Paper, University of California Engineering Library, Berkeley, Calif.; 1952.

Related Economic Articles

1. J. V. Neumann (translation by O. Morgenstern), "A model of general economic equilibrium," *Rev. Economic Studies* (London, England), vol. 13(1), pp. 1–9; 1945–46.
2. P. A. Samuelson, "Foundations of Economic Analysis," Harvard University Press, Cambridge, Mass.; 1948.
3. R. Frisch, "Forecasting a multilateral balance of payments," *Amer. Economic Rev.*, vol. XXXVII, pp. 535–551; September, 1947.
4. D. Hawkins, "Some conditions of macroeconomic stability," *Econometrica* (Chicago, Ill.), vol. 16, pp. 309–352; October, 1948.
5. W. W. Leontief, "Computational problems arising in connection with economic analysis of interindustrial relationships," "Proceedings on Large Scale Digital Calculating Machinery," Harvard University Press, Cambridge, Mass., pp. 169–175; 1948.
6. J. Von Neumann and O. Morgenstern, "Theory of Games and Economic Behavior," Princeton University Press, Princeton, N. J., 1947.

7. O. Aukrust, P. J. Bjerve, and R. Frisch, "A System of Concepts Describing the Economic Circulation and Production Process," Memorandum from the University Institute of Economics, Oslo, Norway; March, 1948.
8. T. C. Koopmans, "Identification problems in economic model construction," *Econometrica*, vol. 17; April, 1949.
9. W. W. Leontief, "Dynamic Analysis of Economic Equilibrium," Proceedings of a Second Symposium on Large Scale Digital Calculating Machinery, Harvard University Press, Cambridge, Mass., pp. 333–337; September, 1949.
10. M. K. Wood and G. B. Dantzig, "Programming of Interdependent Activities, Part I, General Discussion, and Part II, Mathematical Model," *Econometrica* (Chicago, Ill.), vol. 17, pp. 193–211; July–October, 1949.
11. R. M. Goodwin, "The multiplier as matrix," *Economic Jour.*, vol. LIX, pp. 537–555; December, 1949.
12. R. M. Goodwin, "Does the matrix multiplier oscillate," *Economic Jour.*, vol. LX, pp. 764–770; December, 1950.
13. R. M. Goodwin, "The non-linear accelerator and the persistence of business cycles," *Econometrica* (Chicago, Ill.), vol. 19, pp. 1–17 January, 1951.
14. W. W. Leontief, "The Structure of the American Economy, 1919–1939," Oxford University Press, New York, N. Y.; 1951.
15. I. O. Scott, "An exposition of the Keynesian system," *Rev. Economic Studies*, vol. IXX(1), pp. 12–18; 1950–51.
16. R. Stone, "Simple Transaction Models, Information and Computing," Conference on Automatic Control, University of Cambridge, Department of Applied Economics, Cambridge, England; July, 1951.
17. A. Tustin, "The Construction of a Complex Multi-Loop Network Modelling the Major Interdependencies of an Economic System," Birmingham University, England. Paper at a Conference on Automatic Control Systems held at the Aeronautical College, Cranfield, England, July 16–21, 1951. Review of a Conference on Automatic Control Systems, Office of Naval Research, London, Technical Report ONRL-96-51, pp. 19, 20.
18. H. B. Chenery, "Overcapacity and the acceleration principle," *Econometrica*, vol. 20, pp. 1–28; January, 1952.
19. R. Solow, "On the structure of linear models," *Econometrica*, vol. 20, pp. 29–46; January, 1952.
20. H. A. Simon, "On the application of servomechanism theory in the study of production control," *Econometrica*, vol. 20, pp. 247–268; April, 1952.
21. M. Shubik, "A business cycle model with organized labor considered," *Econometrica*, vol. 20, pp. 284–294; April, 1952.
22. J. L. Holley, "A Dynamic Model: I. Principles of Model Structure," *Econometrica*, vol. 20, pp. 616–642; October, 1952.

Related Engineering Articles

1. N. Wiener, "Cybernetics," John Wiley and Sons, New York, N. Y.; 1948.
2. G. H. Orcutt, "A new regression analyser," *Jour. Roy. Statistical Soc.*, (Series A), vol. CXI, part I, pp. 54–70; 1948.
3. E. A. Goldberg, "Electronic simultaneous equation solver," *Jour. Appl. Phys.*, vol. 19, pp. 338–345; April, 1948.
4. L. M. Haupt, "Solution of simultaneous equations through use of a.c. network calculator," *Rev. Sci. Instr.*, vol. 21, pp. 683–686; August, 1950.
5. L. Klein and R. Solow, "Economic model building," *Mech. Eng.*, vol. 72, pp. 990–991; December, 1950.

Correspondence

An Historical Note on the Autocorrelation Function*

In the literature on random processes the earliest use of the autocorrelation function is usually attributed to G. I. Taylor.[1] Later the transform relationship between autocorrelation function and power density spectrum was discovered by Wiener.[2] More recently, Golay[3] has noted the relationship of the autocorrelation function type of analysis to some of Michelson's[4] work with interferometric techniques. The first of Michelson's studies antedated those of Taylor by some thirty years.

It is the purpose of this note to point out the almost complete identity between Michelson's use of the interferometer in determining the power density spectrum of a source of incoherent radiation and the present-day use of autocorrelation for similar purposes, employing what we now know as the Wiener Theorem. It will be shown that Michelson's procedure consisted of observing the autocorrelation function and measuring those properties of it which, upon Fourier transformation, were sufficient to determine the corresponding power density spectrum, except for the value of its center frequency.

The autocorrelation function $\phi(\tau)$ and the power density spectrum $S(\omega)$ of a random function of time, $f(t)$, are related by the Wiener Theorem

$$\phi(\tau) = \langle f(t)f(t+\tau)\rangle = \int_{-\infty}^{\infty} S(\omega)\cos\omega\tau d\omega, \quad (1)$$

in which the symbol $\langle\ \rangle$ indicates the infinite time average. Here $S(\omega)$ is defined as non-zero in the positive frequency range only. When $S(\omega)$ is a narrow band spectrum centered at some ω_0, $\phi(\tau)$ will have the character of a phase-modulated cosine wave of radian frequency ω_0 whose envelope varies symmetrically with τ. By rewriting the above expression (replacing ω by $\omega+\omega_0$) the envelope and phase functions are found to be

$$E(\tau) = [A^2(\tau) + B^2(\tau)]^{1/2} \quad (2)$$

and

$$\theta(\tau) = \tan^{-1} B(\tau)/A(\tau), \quad (3)$$

respectively, where

$$A(\tau) = \int_{-\infty}^{\infty} S(\omega+\omega_0)\cos\omega\tau d\omega \quad (4)$$

and

$$B(\tau) = \int_{-\infty}^{\infty} S(\omega+\omega_0)\sin\omega\tau d\omega. \quad (4a)$$

Conversely, knowing $A(\tau)$ and $B(\tau)$, it is possible to recover $S(\omega+\omega_0)$, the spectrum shape with unspecified center frequency, by an inverse relationship as follows:

$$S(\omega+\omega_0) = \frac{1}{2\pi}\int_{-\infty}^{\infty} e^{-j\omega\tau}dt \int_{-\infty}^{\infty} S(w+\omega_0)e^{jw\tau}dw$$

$$= \frac{1}{2\pi}\int_{-\infty}^{\infty}[A(\tau)\cos\omega\tau + B(\tau)\sin\omega\tau]d\tau$$

$$= \frac{1}{2\pi}\int_{-\infty}^{\infty} E(\tau)\cos(\omega t+\theta(\tau))d\tau. \quad (5)$$

Note that if $S(\omega+\omega_0)$ is even, $B(\tau)$ and $\theta(\tau)$ are identically zero.

The output of an interferometer is the sum of the two functions $f(t)$ and $f(t+\tau)$, where τ is the time equivalent to the difference in path lengths. The intensity of the output is thus

$$I(\tau) = \langle[f(t) + f(t+\tau)]^2\rangle. \quad (6)$$

As τ is advanced there will appear a series of maxima and minima in the output intensity corresponding to constructive and destructive interference, respectively, and the magnitude and phase of these fluctuations will vary with τ. Michelson defined the "visibility" $V(\tau)$ of these interference fringes as

$$(I_{\max} - I_{\min})/(I_{\max} + I_{\min}), \quad (7)$$

where $I_{\max}$ and $I_{\min}$ are the intensities of a maximum and the immediately adjacent minimum. Substituting, we find for stationary $f(t)$ that V is proportional to

$$\langle f(t)f(t+\tau)\rangle_{\max} - \langle f(t)f(t+\tau)\rangle_{\text{adjacent min}}.$$

But this is just twice the envelope $E(\tau)$ of the correlation function as described in the preceding paragraph.

Michelson made many experimental determinations of $V(\tau)$ from which he then obtained the spectrum $S(\omega+\omega_0)$ by the transformations mentioned above. In the case of asymmetrical spectra he also determined the necessary phase function, $\theta(\tau)$.

Paul E. Green, Jr.
Lincoln Laboratory
Mass. Inst. of Tech.

---

* Received by the Institute, May 15, 1953.
Research in this document was supported jointly by the Army, Navy, and Air Force under contract with the Massachusetts Institute of Technology.

[1] G. I. Taylor, "Diffusion by Continuous Movements," *Proc. London Math. Soc.*, Ser. 2, vol. 20, pp. 196–212; 1922.

[2] N. Wiener, "Generalized harmonic analysis," *Acta Mathematica*, vol. 55, pp. 117–258; 1930.

[3] M. J. E. Golay, "Correlation versus linear transforms," PROC. I.R.E., vol. 41, pp. 268–271; February, 1953.

[4] A. A. Michelson, "Application of interference methods to spectroscopic measurements," *Phil. Mag.* vol. 31, pp. 340–348; April, 1891. See also *Studies in Optics;* Chapter 3, University of Chicago Press, 1927.

Correspondence

AC Circuits*

I am writing in connection with the review of W. R. LePage's "Analysis of Alternating-Current Circuits."[1] As this book is of value primarily in undergraduate electrical engineering courses, it is assumed that the review was published as a service to those who choose the texts for such courses. Having taught from the book for two years prior to publication, I feel that some remarks supplemental to the review would be appreciated by anyone considering the use of Dr. LePage's book as a text.

The most important supplementary piece of information is that the book, with its choice of subject matter and less than 400 pages of main text, is intended to cover about the first four hours of ac circuits or the first six hours of circuits, dc and ac. Most modern electrical engineering curriculums will have about three more hours than this, for which a more advanced text is in order. This fact is indicated in the review, but only in the phrase, ". . . and coupled-tuned circuits are not discussed."

Dr. LePage proceeds rather slowly to the point of representing all ac phenomena with complex quantities only. On the way he devotes a good deal of space to the development of the concepts he elects to use and to the behavior of circuit elements and simple combinations of circuit elements under time-varying excitations, sinusoidal and otherwise. The instantaneous value viewpoint is retained until the author thinks he has not only stated a more powerful viewpoint but also has developed the viewpoint in the student's mind. As a matter of fact, a great deal of space is devoted to the attempt to prepare the student's mind for each new step. It is not the purpose of this letter to argue whether or not this effort is well-advised; though certainly no insinuation is intended that it is not. But if the review reports on this aspect of the book, it is only in the phrase, "simple resonant circuits are withheld until page 125."

Two features of this volume are still unique among books of its type, so far as I know, and consequently seem to require mention in a review. There is an extensive treatment of the response of nonelectronic and electronic meters of various response characteristics to irregular waveforms such as found in modern electron-tube circuits. And particularly striking is the use of duality. No development is presented without its dual being treated immediately afterward or perhaps even simultaneously. Neither of these aspects of the book is commented on in the review.

While the above information is presented with the sincere thought that it represents a useful addition to the review published in the PROCEEDINGS, an additional comment seems to be in order. I believe it is the experience of many others as well as myself that it is very difficult to determine dependably the worth of a technical book without using it or studying it for some time. As a consequence, these remarks do not reflect any discredit on the reviewer, who no doubt is a busy man in a position of considerable importance. His comments on isolated detail throughout the book indicate some study of the book, but perhaps not enough to give adequate authority to judgments on over-all approach, philosophy, technique, and results. Also his familiarity with present-day needs of prospective users of the book seems subject to question.

If criticism of these conditions is not warranted, at least the question might be raised whether a review made under these circumstances is sufficiently valuable to present in the PROCEEDINGS.

DAVID W. SPENCE
L. C. Smith College of Engineering
Syracuse University
Syracuse, New York

---

* Received by the Institute, April 10, 1953.

[1] W. R. Le Page, "Analysis of Alternating-Currents," McGraw-Hill Book Co., Inc., New York, N. Y., reviewed in PROC. I.R.E., vol. 41, p. 306; February, 1953.

Echo Distortion in the FM Transmission of Frequency-Division Multiplex*

W. J. Albersheim and J. P. Schafer[1] have shown that when the delay time is sufficiently small (i.e. when the feeder is sufficiently short in the antenna echo case), the maximum distortion, occurring when the echo is in quadrature with the signal, is given by

$$\frac{D_2}{S} = 0.2r\tau^2 sp\sqrt{1 - 0.5p/p_m}$$

where

D_2/S = ratio of distortion to signal (volts) at baseband frequency p (radians/sec).
r = relative echo amplitude.
τ = delay time (secs).
s = FM carrier frequency deviation (radians per sec).
p_m = maximum baseband frequency (radians per sec), the baseband being assumed to extend down to zero frequency.

We are very often concerned with conditions at the upper end of the band ($p = p_m$), where (unless pre-emphasis is used) the distortion is greatest. Then,

$$\frac{D_2}{S} = 0.14r\tau^2 sp_m. \tag{1}$$

The restrictions on the validity of this formula are, approximately,

$$\tau p_m < 1,$$

and

$$\tau s < 1.$$

These conditions, in practice, are quite likely not to hold. Thus, with a deviation of ±4 mc and an air-spaced feeder length of 100 ft (0.2 μsec delay), we find that $\tau s = 5$. Unfortunately, it appears that in this region a more extended analysis would not be easy.

It is known that when τ is sufficiently large, the distortion must approach a constant value, and, in fact, when $s \gg p_m$, Albersheim and Schafer derive an expression for this limiting value which, at the upper end of the band, takes the form

$$\frac{D}{S} = 5.8r(p_m/s)^{1.5}e^{-2.88(p_m/s)^2}. \tag{2}$$

What we require to complete the picture is some means of filling in the curve of distortion/signal in the intermediate region not covered by (1) and (2). The purpose of the present note is to point out that experimental curves of the type shown in Fig. 8 of Albersheim and Schafer can readily be generalized to cover this requirement, even though they are measured only for one delay time.

The argument is very simple. The expression for distortion/signal can only be a function of r, τ, p_m, s and p, and since we are interested in the upper end of the baseband we may neglect the last variable. r is accounted for by the result, verified over an extensive range by Albersheim and Schafer, that the distortion is directly proportional to the echo strength. Now, since D/S is dimensionless, τ, p_m and s can only appear as one or more of the combinations τp_m, τs, p_m/s, and writing the last as $(\tau p_m)/(\tau s)$, it is evident that D/S may be

$$D/S = rF\{(\tau p_m), (\tau s)\}.$$

Thus, to make the curves of Fig. 8 (Albersheim and Schafer, p. 320) applicable to values of the parameters other than those used during the measurements, we re-plot using as abscissae frequency deviation x delay times, in place of frequency deviation, and instead of labeling the curves with the respective maximum modulating frequencies, p_m, we label them with the appropriate values of $p_m\tau$. It is assumed that the test frequencies are effectively at the top end of the band, since curves of distortion against base-band frequency tend to flatten off at the highest frequencies.

These re-plotted curves are shown in Fig. 1. In the original, three of the test frequencies are given as *higher* than the maximum modulating frequency. Since this seems unlikely, it has been assumed that there is a typographical error here, and the larger of the two values has in each case been tentatively taken as the true maximum modulating frequency. If this assumption is incorrect, the errors involved will only be off the order of a decibel.

---

* Received by the Institute, March 16, 1953.

[1] W. J. Albersheim and J. P. Schafer, "Echo distortion in the fm transmission of frequency-division multiplex," PROC. I.R.E., vol. 40, pp. 316–328; March 1952.

Correspondence

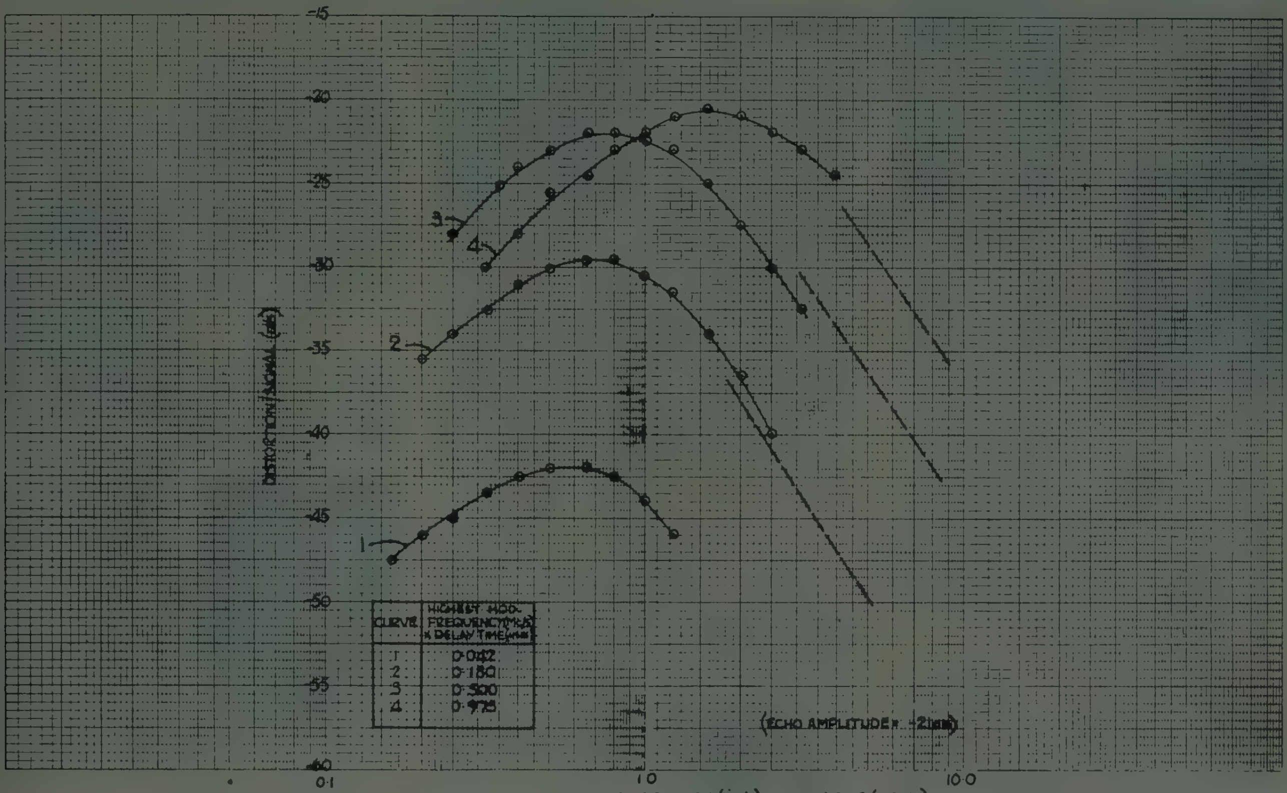


Fig. 1—Curves from Fig. 8 of Albersheim and Schafer, redrawn in terms of $rs/2\pi$ and $rp_m/2\pi$. Dashed straight lines are computed asymptotes.

As an example of the use of Fig. 1, the highest modulating frequency in one case considered was 1.052 mc., and the deviation ±4.5 mc. Standing wave ratios at the upper and lower ends of the antenna feeder were taken as 1.2 and 3 respectively, so that the echo strength, neglecting feeder attenuation, is −26.8 db. Thus, 5.8 db has to be added numerically to values derived from Fig. 1. Considering air-spaced feeder of length l feet, the delay time comes out as 0.00203 l μsecs. Equation (1) will apply when $l < 17$ ft, approximately, so that in this region

$$\frac{D_2}{S} = 4.72 \times 10^{-6} l^2.$$

This gives us the sloping straight line in Fig. 2.

Now, curve 2 of Fig. 1 applies in the present case when the delay time is 0.180 /1.052 = 0.171 μsecs. Thus, the appropriate abscissa is 0.171 × 4.5 = 0.770, and we read off a distortion value = −29.5 db. Adding −5.8 gives −35.3 db. Similarly, values are read off curves 1, 3 and 4, and the resulting four points are plotted in Fig. 2. Equation (2), which applies in this case, gives an upper limit, when l is large, equal to −31.9 db, and using this and the four experimental points as a guide we can draw a plausible-looking curve to cover the region in which both equations (1) and (2) break down.

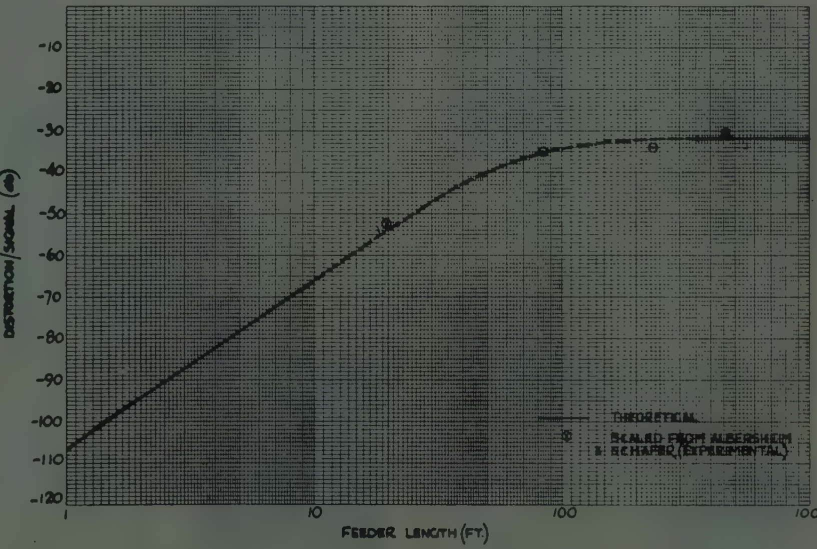


Fig. 2—Flat noise loading. Noise band 0–1.052 mc. Frequency deviation ±4.5 mc. Echo amplitude = −26.8 db.

Of course, since the measured points are rather scanty some imagination has to be used in drawing the dotted portion of the curve, and an error of the order of two db is quite likely. A few more experimental curves to cover intermediate regions of Fig. 1 would be helpful. If these were available it would seem that the problem of the evaluation of distortion due to uncompensated echoes, in the case of the flat noise band whose lowest frequency is zero, could be regarded as solved for practical purposes, at least when the variation of antenna impedance over the rf band can be neglected.

R. G. Medhurst
Research Laboratories
The General Electric Co., Ltd.
Wembley, Middlesex, England

Contributors to Proceedings of the I.R.E.

Samuel N. Alexander (M'44) was born in Wharton, Texas, on February 22, 1910. He completed the A.B. degree in physics and the B.S. degree in electrical engineering at Oklahoma University in 1931, the M.S. degree in electrical engineering at M.I.T. in 1933 under a Tau Beta Pi Fellowship, and conducted D.Sc. research under a Coffin Foundation Fellowship in 1934.

S. N. Alexander

From 1935 to 1940, Dr. Alexander was with Simplex Wire and Cable Company on instrumentation and measurement work, and also was a Research Assistant at M.I.T. during 1939–40. He was with the Navy Department until 1944 on electronic instrumentation tasks and then joined Bendix Aviation Corporation, as a senior project engineer, to develop military telemetering equipment.

After transferring to the National Bureau of Standards in 1946, Dr. Alexander took special training on digital computers at the University of Pennsylvania. He organized and supervised the development team that completed SEAC, the first operational electronic digital computer in the U. S., in May 1950.

In addition, Dr. Alexander served as technical representative for five Government agencies that have acquired computer installations and is consultant on electronic processing of paper-work to Census Bureau, Treasury, Social Security Administration, General Accounting Office, and Navy Supplies and Accounts. He is a member of the American Physical Society, A.I.E.E., Association for Computing Machinery, Phi Beta Kappa, Sigma Xi, Tau Beta Pi, and Sigma Tau.

❖

Biagio F. Ambrosio (A'45) was born in Brooklyn, N. Y., on February 7, 1913. He received the B.S.E.E. degree from the University of Michigan in 1937.

B. F. Ambrosio

From 1937 to 1939 Mr. Ambrosio was a carrier engineer, with the Postal Telegraph Corp., a division of International Telephone and Telegraph Corp. There he did development in teletype equipment, designed and developed carrier systems over land lines, and made transmission line studies.

From 1939–1948 Mr. Ambrosio was an electrical engineer concerned with the research and development of computing machines with International Business Machines He worked in the design and development of business accounting machines and communication machines.

From 1948 to 1949 Mr. Ambrosio was an electronic engineer at the U. S. Navy Electronics Laboratory in San Diego, Calif., where he did research and development of communication systems.

In 1949 Mr. Ambrosio became senior engineer with the Machine Development Unit of the Institute for Numerical Analysis, National Bureau of Standards in Los Angeles, Calif. In this position he designed and developed a high-speed digital computer, specializing in electrostatic memory and its circuitry. He now holds patents in the field of computing and communications.

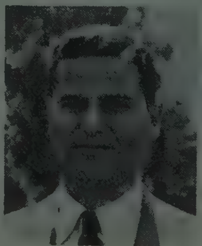
❖

Robert R. Bennett (S'46–A'50) was born in Spokane, Wash., in 1926. He received the B.S. degree from the California Institute of Technology in 1945. He served as a naval officer on the Pacific Fleet Staff and later returned to Cal Tech to receive the M.S. and Ph.D. degrees in electrical engineering, the latter in 1949. Since that time Dr. Bennett has been a member of the technical staff of the Hughes Research and Development Laboratories, Culver City, Calif.

R. R. Bennett

❖

George W. Brown was born in Boston, Mass., on June 3, 1917. He received the A.B. with highest honors in mathematics from Harvard University in 1937, and the A.M. in mathematics from the same institution in 1938. His Ph.D. in mathematics was awarded by Princeton University in 1940.


G. W. Brown

During 1940–41, he was a research statistician with R. H. Macy & Co., New York. From 1942 to 1945 he worked at Princeton on a wartime project for Army Ordnance. In 1945–46 he was an engineer in the Research Laboratory of the Radio Corporation of America, Princeton, New Jersey. He was Associate Professor of Statistics and Professor of Statistics at Iowa State College in 1946–48. From 1948 to 1952 he was a member of the staff of the RAND Corporation. He joined the International Telemeter Corporation as a senior staff member in July 1952. He has been a Visiting Professor of Engineering and Mathematics at UCLA since 1948.

Dr. Brown is a Fellow of the Institute of Mathematical Statistics, and a member of the American Statistical Association, the Association for Computing Machinery, Phi Beta Kappa, and Sigma Xi.

❖

Werner Buchholz (S'44–A'49–SM'52) was born in Germany, on October 24, 1922. He received the B.A.Sc. degree in 1945 and the M.A.Sc. degree in 1947 from the University of Toronto. In 1946 he went to the California Institute of Technology as a graduate student and instructor. While there he participated in the development of the Caltech Analog Computer and obtained the Ph.D. degree in electrical engineering in 1950.

W. Buchholz

In 1949, Dr. Buchholz joined the Poughkeepsie Engineering Laboratory of the International Business Machines Corp. He participated in the early stages of the planning, system design, and programming of the IBM Type 701 computer until the design was frozen. He is now a project engineer in charge of systems planning in the Advanced Machine Development Section.

Dr. Buchholz is a member of the Association for Computing Machinery, Chairman of the Publications Committee of the IRE Professional Group on Electronic Computers, and Editor of the Professional Group on Electronic Computers' Transactions.

❖

Harry E. Burke, Jr. (SM'51), a native of California, graduated from the University California, in Berkeley, in 1941. He received the M.S.E.E. degree from Stanford University in 1947.

H. E. Burke, Jr.

A course at the Navy Radar School at Bowdoin College and Massachusetts Institute of Technology was followed by five years' work installing and repairing submarine electronic equipment at New London, Conn., Pearl Harbor, Hawaii, and Perth, Australia. This war service was completed by a survey of the Japanese submarine equipment at Sasebo and Kure.

Since 1947 Mr. Burke has been with Consolidated Engineering, Pasadena, Calif. At present he is in charge of the Data Processing Systems Group of that organization.

❖

Arthur W. Burks

Arthur W. Burks was born in Duluth, Minnesota, on October 13, 1915. He received the B.A. degree in mathematics from DePauw University in 1936, and the M.A. and Ph.D. degrees in philosophy from the University of Michigan in 1937 and 1941 respectively.

He was an instructor of electrical engineering at the Moore School of the University of Pennsylvania from 1941 to 1946. Since that time he has been teaching logic and the philosophy of science at the University of Michigan where he is now Associate Professor of Philosophy.

Dr. Burks participated in the design of the ENIAC and the computer at the Institute for Advanced Study. Since 1948 he has been a consultant to the Burroughs Corporation. He is a member of the American Philosophical Association, Eta Kappa Nu Association, the Society of Sigma Xi and the Association for Symbolic Logic.

❖

Leonard J. Craig

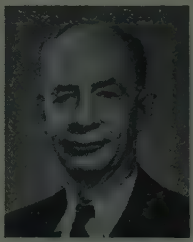
Leonard J. Craig (S'49–A'50) was born in Kansas City, Mo., on September 21, 1924. He started studying electrical engineering at the University of California at Los Angeles in 1942, but shortly after discontinued his studies to enter the U. S. Army. During his three years' service one year was spent in the Army Specialized Training Program for Engineering, the other two on active duty with the Cavalry.

Mr. Craig re-entered the University of California at Berkeley in 1946 and received the B.S. degree in electrical engineering in 1949. He is currently doing part-time graduate work at UCLA.

From 1949 to 1952 Mr. Craig was a member of the technical staff at the Hughes Aircraft Co. Research and Development Laboratories, where he participated in the design and development of missile-test and launch-programming equipment. He also did research and design of components for analog computers and fundamental research in magnetic amplifiers.

In 1952 Mr. Craig joined the Benson-Lehner Corp., where he is now employed as a research engineer for computer input-output and data-reduction equipment.

Mr. Craig is a member of the American Institute of Electrical Engineers.


L. P. Crosman

Loring P. Crosman (A'52) was born at Swampscott, Massachusetts, on July 23, 1892. He received the B.S. degree from Haverford College in 1915, where he was a member of the honorary Founder's Society. He joined the sales organization of the Monroe Calculating Machine Company in 1923. In 1926 he became Chief Inspector in that company's manufacturing operations and in 1929 became head of research and development of adding and bookkeeping machines. In 1941 the calculating and checkwriting machine development departments were added to his responsibilities. During World War II he also developed, under NDRC sponsorship, the Odograph map plotting machine with electronic control for use in vehicles.

After an intensive course in electronics at Columbia University, in 1943 Mr. Crosman joined Remington Rand Inc. in the tabulating machines laboratory, then located in Brooklyn, New York. In 1944 he started the electronic computer development which has resulted in the Remington Rand Type 409-2, transferring operations to the Laboratory of Advanced Research in Norwalk, Conn., in 1946, where he continues electronic computer research. Mr. Crosman is a charter member of the Association for Calculating Machinery.

❖

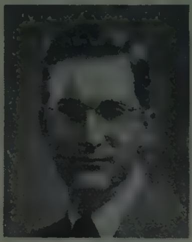
J. P. Eckert, Jr.

J. P. Eckert, Jr. (S'41–A'47) was born on April 9, 1919, in Philadelphia, Pa. He received the B.S. degree in electrical engineering from the Moore School of Electrical Engineering of the University of Pennsylvania in 1941, and the M.S. in electrical engineering in 1943.

While earning his M.S. Mr. Eckert taught engineering, science, and management defense training at the School. In 1943 he became chief engineer for the ENIAC project, and in 1945 was concerned with the design and construction of its successor, the EDVAC. In the summer of 1946 he taught electronic computing devices at the Moore School.

The following fall Mr. Eckert and Dr. John W. Mauchly formed a partnership, known as the Electronic Control Co., which in 1947 was incorporated as the Eckert-Mauchly Computer Corp. As chief engineer Mr. Eckert was responsible for the design and construction of the BINAC, and all-electronic computer, and the UNIVAC, a large-scale electronic digital computer designed to handle both numeric and alphabetic data. When the Corporation became a division of Remington Rand Inc. in 1950, Mr. Eckert became director of engineering.

In 1949 Mr. Eckert and Dr. Mauchly were awarded the Howard N. Potts Medal by the Franklin Institute.


R. D. Elbourn

Robert D. Elbourn (S'40–A'41–M'48) was born in Indianapolis, Ind., on October 5, 1919. He received the degrees BSEE in 1940 and MSEE in 1949 from Purdue University.

In 1940 and 1941 he worked on magnetic recording and on electronic instruments for C. G. Conn, Ltd., in Elkhart, Indiana. From 1941 to 1947 his work in the U. S. Naval Ordnance Laboratory in Washington, D. C., was chiefly on underwater sound in connection with the development of mines and torpedoes, though about one year was on the design of an electronic digital computer.

Since 1947 he has been in the Electronic Computers Section of the National Bureau of Standards where he studied digital magnetic recording, participated in the design of SEAC and now is studying improved circuits and components for digital computers.

Mr. Elbourn is a member of the AIEE, the Acoustical Society of America, the Association for Computing Machinery, Tau Beta Pi and Eta Kappa Nu.

❖

R. S. Erickson

Robert S. Erickson (A'48) was born in Kasson, Minn. on December 4, 1920. He received the B.E.E. degree from the University of Minnesota in 1943, and then served with the Signal Corps as a radar officer until 1946.

Since 1946, Mr. Erickson has been with Engineering Research Associates Division of Remington Rand Inc., where he has worked with digital computing equipment. He has been in charge of the development and construction of several large high-speed data-handling equipments, the latest being the ONR Logistics Computer. He is at present concerned with applying digital computer techniques to industrial data-handling problems.

Mr. Erickson is a registered professional engineer in the State of Minnesota. He is a member of the Association for Computing Machinery and the AIEE.

❖

C E. Frizzell

Clarence E. Frizzell (A'51) was born in Huntington, W. Va., on September 18, 1920. He joined IBM in 1940 as a Customer Engineer in the Time Equipment Division. In 1941 he started a 5 year tour with the Navy. After attending the Radio Materiel School NRL Bellevue, D. C., he was assigned to a USN Repair Ship as Chief Warrant Officer in charge of the Electronic Repair Laboratory. Later he served in the Electronics Laboratory, U. S. Navy Yard, Pearl Harbor.

Mr. Frizzell returned to IBM in 1945 as a Customer Engineer in the Electric Accounting Machine Division. In 1949 he was transferred to the Engineering Laboratory at Poughkeepsie as a Technical Engineer and in 1951 was made Project Engineer in charge of a group designing circuits and components for the 701.

Mr. Frizzell is a member of the Association for Computing Machinery, a member of the IRE Professional Group on Electronic Computers, and chairman, Membership Committee, Mid-Hudson Sub Section, IRE.

◆

Simon E. Gluck

Simon E. Gluck (A'49) was born on October 8, 1921, in New York, N. Y. He received the B.S. degree in chemical engineering from the Massachusetts Institute of Technology in 1943. From 1943 to 1946 he served as an officer in the U. S. Navy. Upon completion of the radar engineering course at Princeton and at M.I.T., he was assigned to a destroyer division in the Pacific theatre as Radar Maintenance Officer. His final naval assignment was as a member of an ordnance development unit at the Johns Hopkins Applied Physics Laboratory. In 1946 he joined the Digital Computer Staff in the Research Division of the Moore School of Electrical Engineering, University of Pennsylvania. His work has included logical and electronic design on the EDVAC and the MSAC, both electronic digital computers. Since 1950 he has served as Group Supervisor of the MSAC Project.

Mr. Gluck is a member of Sigma Xi, the Association for Computing Machinery, the Franklin Institute and the Philadelphia Chapter of the Professional Group on Electronic Computers.

◆

Harry J. Gray, Jr.

Harry J. Gray, Jr. (S'45–A'46) was born in St. Louis, Mo., on June 24, 1924. He entered Lehigh University in 1941, to be sent two years later to the University of Pennsylvania under the Navy V-12 program, where he received the degree of B.S. in electrical engineering in 1944. After commissioning as an Ensign, he studied Navy radio and radar at Bowdoin College and the Massachusetts Institute of Technology, subsequently serving on active duty in the Pacific until 1946.

Dr. Gray received the M.S. degree in 1947 and the Ph.D. degree in 1953 from the University of Pennsylvania, where he has been engaged in teaching electromagnetic field theory and further work on digital and pulse techniques. He is presently an Assistant Professor of electrical engineering at the University of Pennsylvania, and is a member of Tau Beta Pi, Eta Kappa Nu and Sigma Xi.

◆

S. Greenwald

Sidney Greenwald (A'50) was born in New York City on August 31, 1914. He was graduated from Brooklyn College in 1936 with a B.A. in physics and has since pursued graduate studies at George Washington University.

During the war Mr. Greenwald served as electronic officer in the Air Force. Afterward, he joined the staff of the Sperry Gyroscope Company, where he worked on radar fire-control equipment.

In 1947 Mr. Greenwald joined the Electronic Computers Laboratory of the National Bureau of Standards. During the development and construction of SEAC he was primarily responsible for the design of its arithmetic and control circuitry. More recently he has been engaged in work on the computer input-output equipment and electrostatic memory. He is presently in charge of the high-speed pulse circuitry group.

He is a member of the IRE Professional Group on Computers, and the Association for Computing Machinery.

◆

Donald L. Haas

Donald L. Haas (A'49) was born on February 14, 1922, in Strasburg, Ohio. He received the B.S. degree in electrical engineering in 1948 from the University of Akron after serving in the U. S. Army for three years.

From 1948 to 1951 Mr. Haas was employed at Mound Laboratory, Dayton, Ohio, as a research physicist.

Since 1951 Mr. Haas has been with the Goodyear Aircraft Corporation as a development engineer in the computer section.

◆

V. S. Haneman, Jr.

Vincent S. Haneman, Jr. (A'51) was born in Orange, N. J., on February 19, 1924. In 1947 he received the B.S. degree in aeronautical engineering from the Massachusetts Institute of Technology. Previous to this time he had been serving in the U. S. Air Force. In 1950 he received the MSE (Aero) degree from the University of Michigan.

After graduation in 1947, he became the assistant head of flight research of a Navy project at M.I.T. prescribing experiments and instrumentation for rocket and aircraft flights. From 1949 to 1951, he was a graduate student and research engineer as project head of several computer servo-control projects at the University of Michigan. While at the University of Michigan he conceived and was project engineer of the Automatic Wind Tunnel Data Reduction Project.

Captain Haneman, USAF, was recalled to active military service in September, 1951, to serve with the Computation Research Section, Flight Research Laboratory, Wright Air Development Center.

Captain Haneman is an Associate member of Sigma Xi, a member of the Institute of Aeronautical Science and the University of Michigan Science Research Club.

◆

Ruth C. Haueter

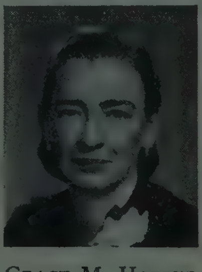
Ruth C. Haueter (A'50) was born in Pequot, Minn. on May 31, 1921. She received a B.A. degree in mathematics from the University of Wyoming in 1943.

Miss Haueter then entered the Navy as a WAVE and received training at the Harvard and M.I.T. Radar schools. Soon afterward she was assigned to the Bureau of Ships as an electronics officer on IFF equipment.

On her release to inactive duty Miss Haueter joined the staff of the Naval Research Laboratory, where she worked on a small relay computer. In 1947 she transferred to the National Bureau of Standards at Washington, D. C. and soon afterward became associated with the Electronic Computers Section. She was a key member of the staff that designed and developed the SEAC, her major contribution having been to the development of the memory selection circuits and the control and arithmetic units. Since 1950 she has worked mostly on input-output equipment, high-speed circuitry, and electrostatic memory.

Miss Haueter is a member of the PGEC, The Association for Computing Machinery and the Society of Women Engineers.

◆


Grace M. Hopper

Grace Murray Hopper was born in New York, N. Y., on December 9, 1906. She received the B.A. degree from Vassar College in 1928, and the M.A. (1930) and Ph.D. (1934) from Yale University. She also studied as a Vassar Faculty Fellow at New York University, and at the Massachusetts Institute of Technology.

From 1931 through 1944, Dr. Hopper was a member of the mathematics staff of Vassar College, rising to be associate professor of that subject. In 1944 she entered the WAVES, receiving her commission as a Mathematical Officer in the Navy's Bureau of Ordnance. During the following two years, she was associated with the Bureau's Computation Project at Harvard University. She was separated to inactive duty in 1946, but remained at Harvard University as a Research Fellow in Engineering Sciences and Applied Physics in the Computation Laboratory there.

In 1949, Dr. Hopper assumed the post of senior mathematician with the Eckert-Mauchly Computer Corp., remaining with that organization as senior programmer after it became a Division of Remington Rand. Since 1952, she has been a systems engineer with the Programming Development group of Remington Rand.

Dr. Hopper is the author of several papers on computer programming, and coauthor of certain of the Annals of the Computation Laboratory of Harvard University, and other volumes. She is a past Chapter president of the Society for Women Engineers, and vice-president of the Society for Industrial and Applied Mathematics, of whose Planning Committee she is now chairman. She is also a member of the American Institute of Electrical Engineers, the Association for Computing Machinery, the Reserve Officers' Association of the United States, the American Ordnance Association, the Franklin Institute of Philadelphia, and the Institute of Mathematical Statistics.

❖

Robert M. Howe was born in Oberlin, Ohio, on August 28, 1925. He received the B.S. degree in electrical engineering in 1945 from the California Institute of Technology, the A.B. in physics in 1947 from Oberlin College, the M.S. in physics in 1948 from the University of Michigan, and the Ph.D. in physics in 1950 from the Massachusetts Institute of Technology. From 1947–48 he was a research associate at the Engineering Research Institute, University of Michigan, where he did basic research on the design and application of electronic analog computers. From 1949–50 he carried on fundamental research in low pressure mercury arcs as a research assistant at the Research Laboratory of Electronics, M.I.T.

Robert M. Howe

In 1950 Dr. Howe returned to the University of Michigan in the Department of Aeronautical Engineering, where he is currently an assistant professor in automatic control, guidance of pilotless aircraft and missiles, and nuclear engineering. In addition, he is continuing research on electronic differential analyzers, flight simulators, and weapons systems.

Dr. Howe is a member of Phi Beta Kappa, Tau Beta Pi, Sigma Xi, the American Institute of Physics and the American Association for the Advancement of Science.

❖

Harry Douglas Huskey (A'49) was born in Whittier, N. C., on January 19, 1916. In 1937 he received the B.S. degree from the University of Idaho, and in 1940 and 1942 respectively, the M.A. and the Ph.D. degrees from Ohio State University.

Harry D. Huskey

During 1943–46 he was an Instructor at the University of Pennsylvania. It was during this time that he served as a consultant for the ENIAC.

In 1947 Dr. Huskey worked at the National Physical Laboratory, Teddington, England. There he did research in coding and logical design for digital computing machines, supervised the design, and began the actual construction of a pilot model of the ACE.

In 1948, he returned to the United States, to work for the National Bureau of Standards, Washington, D. C., and became Chief of the Machine Development Laboratory of the National Applied Mathematics Laboratories of the Bureau.

In December, 1948, he was transferred to the Institute for Numerical Analysis, a field station of the National Bureau of Standards located at Los Angeles. There he was responsible for the design and construction of the National Bureau of Standards Western Automatic Computer (SWAC). In 1950 he became Assistant Director in charge of Mathematical Services at the Institute and in September, 1952, he obtained a year's leave of absence to become Technical Director of the Computation Laboratory of Wayne University, Detroit.

Dr. Huskey helped to organize and was the first Chairman of the Professional Group on Electronic Computers in the Los Angeles area, and served as the first Vice-Chairman of the National Professional Group. At present he is a member of the Administrative Committee of the National Group and Editor of the Review Section of the group's quarterly publication, the TRANSACTIONS of the Professional Group on Electronic Computers.

He is a member of the Association for Computing Machinery, American Mathematical Society, Mathematical Association of America, AAAS, Industrial Mathematical Society, and Sigma Xi.

❖

Gilbert W. King was born on January 13, 1914, in Long Eaton, Derbyshire, England. He received an S.B. from MIT in 1933 and a Ph.D. in 1935. He was a National Research Fellow at California Institute of Technology 1935–37, Harvard University 1937 and Princeton University 1937–38; an Instructor in the Chemistry Department of Yale University 1938–39, Research Associate at MIT in 1939–41 and from 1946 to 1952. His major activities in the years 1941–52 were with Arthur D. Little, Inc., Cambridge, Massachusetts, except for a period of loan to the Office of Scientific Research and Development for work on Operational Analysis. For this work he received the Army-Navy Certificate of Appreciation. Other activities with the military have been as a member of the Beacon Hill Study Group and as a consultant for the Weapons System Evaluation Group (1952). He joined the International Telemeter Corporation in the fall of 1952.

G. W. King

He was Associate Editor of the *Journal of Chemical Physics* 1948–50, and Visiting Lecturer on chemistry at Harvard University 1947.

He is a Fellow of the American Academy of Arts and Sciences and of the American Physical Society; and a member of the American Chemical Society, the Netherlands Physical Society, the American Optical Society, the American Association for the Advancement of Science, the Association for Computing Machinery and the Operations Research Society of America.

His principal activities have been in molecular structure, as determined from infrared spectra, and the infrared spectroscopy of substances at extremely low temperatures. The theoretical phases of this work have centered around a series of papers on the interpretation of spectra of the "Asymmetric Rotor"; and a series on "Spectroscopy from the Point of View of Communication Theory." He has pioneered in the use of large-scale computing machines in the above fields, and in the application of the Monte-Carlo method to statistical mechanics.

His research and development in the commercial field has been varied, including basic studies of the reduction of iron ore, of the recording of information in digital form, and in operations research.

❖

Cornelius T. Leondes (S'48–A'53) was born on July 21, 1927, in Philadelphia, Pa. He received the B.S.E.E. from the University of Pennsylvania in February, 1949. At that time he joined the staff of Naval Air Development Center where he aided in the development of Sonic Homed Missiles and Proportional Turn Control Devices for autopilots.

C. T. Leondes

In the Fall of 1949, he returned to the University of Pennsylvania to pursue graduate studies. During the Summer of 1950 he joined the staff of the Research Division of the Burroughs Adding Machine Co., where he aided in the development of computer circuits. In the Fall of 1950 he returned to the University of Pennsylvania to continue his graduate studies. At the same time he joined the staff of the Research Division of the Moore School of Electrical Engineering, where he has remained since.

While a member of the staff at the Moore School, he has worked on the development of circuits for digital computers, non-linear techniques for servo-mechanisms, special-purpose computers and digital computers for real-time simulation problems.

Mr. Leondes received the degree of M.S.E.E. from the University of Pennsylvania in February, 1951. He is currently completing work toward an advanced degree.

Mr. Leondes is a member of the A.I.E.E., I.R.E., Tau Beta Pi, Sigma Tau, Eta Kappa Nu and Pi Mu Epsilon.

❖

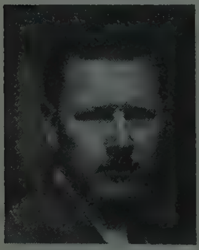
P. V. Levonian

Puzant V. Levonian (A'52) was born May 16, 1928, in Philadelphia, Pennsylvania. He received the B.S. degree in electrical engineering in 1949 from the Drexel Institute of Technology, and the M.S. degree in electrical engineering in 1953 from the University of Pennsylvania.

Since 1949 he has been a member of the Research Division of the Moore School of Electrical Engineering, University of Pennsylvania, where he was engaged in the logical and circuit design of electronic digital computers.

Mr. Levonian is a member of Phi Kappa Phi, Tau Beta Pi and Eta Kappa Nu societies.

❖



W. D. Lewis

W. D. Lewis (A'44) was born on January 6, 1915, in Augusta, Ga. He received the B.A. degree in communication engineering from Harvard University in 1935. In the same year he went as a Rhodes Scholar to Oxford University, England, from which he received the A.B. in mathematics in 1938. He then returned to Harvard to work for his Ph.D. in mathematical Physics, which he received in 1941.

Dr. Lewis has been a member of the technical staff of Bell Telephone Laboratories since July, 1941. Here his work has been primarily in the field of radar antennae, radio repeaters, microwave circuitry, and telephone switching. Since 1951 he has been Director of Switching Research.

❖

W. A. Malthaner

William A. Malthaner (SM'51) was born in Columbus, Ohio, in 1915. He received the B.E.E. degree from Rensselaer Polytechnic Institute in 1937. Immediately thereafter he joined Bell Telephone Laboratories, whree for several years he was concerned with circuit testing and development, including work on Number 1 Crossbar. He also devoted time to research on subscriber signaling arrangements and the associated central office switching systems. During World War II, Mr. Malthaner did government contract work on automatic fire control systems and fire control radar. Since 1945 he has been interested in new automatic telephone central office systems, subscriber dialing and interoffice signaling systems.

Mr. Malthaner is a member of Sigma Xi, Tau Beta Pi and an associate of the A.I.E.E.

❖

John W. Mauchly

John W. Mauchly (A'42) was born in Cincinnati, Ohio, on August 30, 1907. From 1925 to 1932 he studied electrical engineering and physics at Johns Hopkins University. He joined the staff of that University as assistant in physics in 1928, and became junior instructor in physics in 1930. In 1932, he received from Johns Hopkins the Ph.D. in Physics, and from 1932 to 1933 was the research assistant in spectroscopy there. During the summers between school terms, Dr. Mauchly was employed at the National Bureau of Standards and at the Department of Terrestrial Magnetism, Carnegie Institute at Washington.

From 1933 through 1941, Dr. Mauchly was professor of physics at Ursinus College. He resigned that post in 1941 to accept an appointment as instructor at the Moore School of Electrical Engineering, University of Pennsylvania. In 1943, while an assistant professor at the school, he proposed a large electronic calculator for expediting the various computational problems then being undertaken by manually-operated machines. Between 1943 and 1946, he collaborated with J. P. Eckert, Jr., on the design and construction of such a machine, the ENIAC. The ENIAC was the first automatic, completely electronic computer, and is still in operation at Aberdeen Proving Grounds.

In 1946, Dr. Mauchly and Mr. Eckert formed a partnership in Philadelphia known as the Electronic Control Company. The following year, this was incorporated as the Eckert-Mauchly Computer Corporation, with Dr. Mauchly as president. From this position, Dr. Mauchly was responsible for many aspects of the development of the BINAC and the UNIVAC System. The corporation became a division of Remington Rand, Inc., in 1950. Dr. Mauchly has subsequently devoted much time to one of his principal interests, the complex computational problems of meteorology.

In 1949, Dr. Mauchly and Mr. Eckert received the Howard N. Potts Medal from the Franklin Institute in Philadelphia, in recognition of their pioneer work in the electronic computer field. Dr. Mauchly is a past president of the Association for Computing Machinery, and a trustee of the Society for Industrial and Applied Mathematics. He is also a member of the American Physical Society, the American Institute of Electrical Engineers, the American Meteorological Society, the American Geophysical Union, the Institute of Mathematical Statistics, the American Statistical Association, the Franklin Institute of Philadelphia, Phi Beta Kappa, and Sigma Xi.

❖

W. A. McCool

William A. McCool (A'49) was born in Chambersburg, Pa., on June 17, 1915. He received the B.S. degree in 1937 and the M.S. degree in electrical engineering in 1948, both from the University of Maryland.

From 1937 to 1941, Mr. McCool was a test engineer with Air-Track Manufacturing Co., Bendix Radio Corp., and Westinghouse Electric and Manufacturing Co.

In 1941 Mr. McCool joined the Radio Division staff of the Naval Research Laboratory where, until 1948, he participated in the development of precision frequency measuring devices, low frequency direction-finders, and UHF signal generators. He also assisted in organizing and directing a program for basic radio-component evaluation which aided the Armed Forces in formulating many of the JAN specifications in use at the present time. In connection with this, Mr. McCool developed devices and techniques especially required for component evaluation, on three of which he holds patents.

Since 1948 Mr. McCool has been employed in the Mechanics Division of the Naval Research Laboratory, where he organized an analog computing center, and has made several notable contributions in the field of analog computation. He is also a lecturer in electrical engineering at the University of Maryland.

Mr. McCool is a member of Tau Beta Pi and Phi Kappa Phi.

❖

J. H. McGuigan

John H. McGuigan (A'42) was born in 1918, in Chicago, Ill. He attended Massachusetts Institute of Technology, receiving both the B.S. and M.S. degrees in 1941. He joined Bell Telephone Laboratories the same year and until 1945 was engaged in radar development work before transferring to transmission and the development of television transmission facilities. In 1946 he joined the Switching

Research Department, where he has been concerned with the development of signaling systems and magnetic drum recording.

Mr. McGuigan is a member of Sigma Xi, Eta Kappa Nu and Tau Beta Pi.

❖

C. A. Meneley

Carl A. Meneley (S'41–A'43–M'47–SM'53) was born at Virden, Ill., in 1912. After receiving the B.S. degree in electrical engineering from the University of Illinois in 1941. He joined the Research Division of RCA, transferring in 1942 to the newly established RCA Laboratories at Princeton, N. J. From 1941 through 1946 he assisted in the development of a naval fire-control radar, military equipment for speech coding and for the infrared detection of ships, and of a UHF television transmitter.

Mr. Meneley joined the Aerophysics Departments of Goodyear Aircraft Corporation in 1946 and became head of the Electronics Instruments Section in 1947. Major projects under his direction have included missile guidance, flight trainers, special purpose computers, and GEDA, a line of electronic differential analyzers. He is presently head of Electronic Systems Engineering.

Mr. Meneley is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.

❖

E. F. Moore

Edward F. Moore (A'53) was born on November 23, 1925, in Baltimore, Md. He received the B.S. degree in chemistry from Virginia Polytechnic Institute in 1947, and the M.S. and Ph.D. degrees in mathematics from Brown University in 1949 and 1950.

During 1950–51, Dr. Moore was an assistant professor of mathematics at the University of Illinois, associated with the electronic digital computer project there.

Since 1951 Dr. Moore has been a member of the technical staff of Bell Telephone Laboratories, doing theoretical work in the Switching Research Department.

Dr. Moore is a member of Sigma Xi, Phi Lambda Upsilon, Phi Kappa Phi, the National Speleological Society, the American Mathematical Society, and the Association for Computing Machinery.

❖

C. D. Morrill

Charles D. Morrill (A'48) was born in St. Louis, Mo., on October 31, 1919. He graduated from the University of Illinois with the B.S. degree in electrical engineering in 1941. From 1941 through 1945, he served in the Army Air Force as a communications and radar officer in the United States and the Central Pacific Area. Between 1946 and 1948, Mr. Morrill was with the Long Lines Division of the American Telephone and Telegraph Company, Chicago, Ill.

In 1948, Mr. Morrill joined the Aerophysics Department of the Goodyear Aircraft Corporation, Akron, O., where he has since been primarily engaged in the development, design and application of electronic differential analyzers. He is the author of several papers on analog computer applications and computing devices.

Mr. Morrill is a member of Eta Kappa Nu.

❖

S. M. Oster

Stanley M. Oster was born in Philadelphia, Pa., on January 27, 1926. He was graduated from the University of Pennsylvania in 1949 with the B.S. in mechanical engineering, and two years later received the B.S. in electrical engineering.

Mr. Oster first joined the staff of the Ballistics Research Laboratory, U. S. Army Ordnance Department, at Aberdeen Proving Grounds. Since 1951 he has been employed by the Eckert-Mauchly Division, Remington Rand Inc., where he is a member of the group responsible for the development of input-output devices for UNIVAC Systems. Mr. Oster's principal responsibility there is the development of high-speed magnetically-actuated braking and clutching devices.

Mr. Oster is a member of the American Society of Mechanical Engineers, the American Institute of Electrical Engineers, and the Pennsylvania Academy of Science.

❖

Max Palevsky

Max Palevsky was born in Chicago, Ill., on July 24, 1924. During World War II he served as electronics officer with the U. S. Air Corps in New Guinea and the Phillipine Islands. He received the Ph.B. and the B.S. degree in mathematics from the University of Chicago in 1946. For the next five years he did under-graduate and graduate work in philosophy at the University of Chicago and the University of California. In July, 1952, he joined the Computer Division of Bendix Aviation Corporation, where he now is engaged in the design of digital computers.

❖

J. A. Rajchman

Jan A. Rajchman (SM'46–F'53) was born in London, England, on August 10, 1911. He received his diploma in electrical engineering in 1934 and the degree of Doctor of Technical Sciences in 1938 from the Swiss Institute of Technology. In 1936 he joined the staff of the RCA Manufacturing Company as a research engineer and in 1942 was transferred to the RCA Laboratories in Princeton. He specialized in electron optics and computing devices. He is chiefly responsible for the development of the electron multiplier tube, co-recipient of the 1947 Levy Medal of the Franklin Institute for work on the betatron, developed many computing circuits and the selective electrostatic storage tube. He is now very active in the field of magnetic core memory and switching devices. He holds about 40 U. S. patents.

Dr. Rajchman is a member of the American Physical Society, the Council of the Association for Computing Machinery, and Sigma Xi.

❖

L. N. Ridenour

Louis N. Ridenour (SM'52) was born on November 1, 1911, in Montclair, N. J. He received the B.S. in physics from the University of Chicago in in 1932, and the Ph.D. from the California Institute of Technology in 1936. He was a Member of the Institute for Advanced Study in 1935–36; an Instructor of Physics at Princeton University 1936–38; and Assistant Professor, Associate Professor, and Professor of Physics at the University of Pennsylvania during the period 1938–47. On leave from Penn from 1941 to 1946, he was a Staff Member and Assistant Director of the Radiation Laboratory at Massachusetts Institute of Technology. During 1944 he served overseas as the chief radar advisor of the U. S. Air Forces in Europe; he was an Expert Consultant, Office of the Secretary of War from 1942 to 1945.

Upon returning to the Radiation Laboratory, Ridenour became Editor-in-Chief of the Radiation Laboratory Series of 27 technical volumes on radar and microwave electronics; he was the editor of Volume 1 of that Series: RADAR SYSTEM ENGINEERING. In the years 1947–51 he was Professor of Physics and Dean of the Graduate College at the University of Illinois. He took leave in 1950–51 to serve as Chief Scientist of the U. S. Air Force.

For his wartime work, Ridenour was awarded the President's Medal for Merit and the Bronze Star; in 1951 he was given the Citation of Honor Award of the Air Force Association.

He is a Fellow of the American Physical Society, and the A.A.A.S; a member of the Association for Computing Machinery (Councillor), the Operations Research Society of America, Sigma Xi, and Phi Beta Kappa.

Ridenour joined the International Telemeter Corporation as a consultant in September 1951, becoming Vice President, Engineering, and a member of the Board of Directors in July 1952. He is Visiting Professor of Engineering at the University of California, Los Angeles.

◆

J. E. Robertson

James E. Robertson (S'48–A'50) was born March 30, 1924 in Fairfax, Oklahoma. He received the degree of B.S. in Electrical Engineering from Oklahoma A. and M. College in 1947 and the degrees of M.S. and Ph.D. from the University of Illinois in 1948 and 1952, respectively.

During the period 1947–1950 Mr. Robertson held the positions of Research Assistant and Westinghouse Educational Foundation Fellow at the University of Illinois. He has been associated with the Digital Computer Laboratory of the University of Illinois since 1950, as a Research Assistant, Research Associate, and as a Research Assistant Professor of Electrical Engineering.

Dr. Robertson is a member of Eta Kappa Nu, Sigma Xi, and the Association for Computing Machinery.

◆

H. D. Ross, Jr.

Harold D. Ross, Jr. (S'48–A'50) was born in Mt. Morris, Ill., on August 5, 1922. He received the B.S. degree in electrical engineering from the Illinois Institute of Technology in 1944. From 1944 through 1946 he was employed by the Western Electric Co., where he was concerned with development of manufacturing and testing facilities for X-band and K-band magnetrons. He then engaged in graduate study at the University of Chicago and Northwestern University, receiving the M.S. degree in electrical engineering from the latter in 1949. While at Northwestern he was associated with the Microwave Laboratory, engaged in research on higher-mode propagation in waveguides and development of microwave antenna pattern measuring apparatus.

Since 1949 Mr. Ross has been with the Poughkeepsie Laboratory of the International Business Machines Corp. where he has participated in the development of several high speed electronic digital computers. He was responsible for the design of the arithmetic element of the Type 701 computer and currently, as project engineer, is engaged in the development of equipment for the armed forces.

Mr. Ross is a member of Tau Beta Pi, Eta Kappa Nu, and the Association for Computing Machinery.

◆

Morris Rubinoff

Morris Rubinoff (A'50) was born in Toronto, Canada, on August 20, 1917. He attended the University of Toronto, where he received the B.A., M.A. and Ph.D. degrees in 1941, 1942 and 1946, respectively. During World War II he participated in proximity fuse research at the University of Toronto and in England.

In 1946 Dr. Rubinoff joined the staff of Harvard University, as Instructor in Physics and Fellow in Applied Science at the Computation Laboratory. From 1948 to 1950 he assisted in the design of the Institute for Advanced Study electronic digital computer. In 1950 he transferred to his present position as Assistant Professor in Electrical Engineering at the University of Pennsylvania, where he is engaged in research on digital real-time simulation.

Dr. Rubinoff is a member of the Am. Phys. Soc., the A.I.E.E., the Am. Assoc. of Univ. Professors and Sigma Xi.

◆

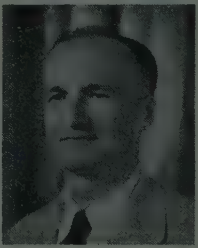
Arthur L. Samuel

Arthur L. Samuel (A'24–SM'44–F'45) was born on December 5, 1901, at Emporia, Kan. He received the A.B. degree from the College of Emporia in 1923, and S.B. and S.M. in electrical engineering from Massachusetts Institute of Technology in 1926. He was awarded the honorary degree of S.D. from the College of Emporia in 1946.

Dr. Samuel was employed by the General Electric Company intermittently from 1923 to 1927, and was an instructor in the electrical engineering department at M.I.T. from 1926 to 1928. He joined the technical staff of the Bell Telephone Laboratories in 1928. From 1931 to 1946 his principal interest was in the development of vacuum tubes for use at ultra-high frequencies. From 1946 to 1949 he was at the University of Illinois as professor of electrical engineering and director of the Electron Tube Research Laboratory.

Dr. Samuel became associated with International Business Machines Corporation in 1949 and is currently manager of research in the Poughkeepsie Engineering Laboratory. He is a licensed professional engineer in New York State, a member of Sigma Xi and the American Association for the Advancement of Science, and a fellow of the American Physical Society and of the AIEE.

◆



Robert Serrell

Robert Serrell (A'35–SM'44) was born in France of American parents in 1904. He obtained the E.E. degree from the Inst. Electrotechnique, Paris, France, 1926. He was engaged in the design of Television Transmitters at the Camden, N.J., plant of the RCA Manufacturing Co. from 1935 to 1940; in charge of Television Transmitter development with the Columbia Broadcasting System in New York in 1940 and 1941; Group Leader and Consulting Engineer at the Radio Research Laboratory of Harvard University from 1942 to 1945; in charge of Television Operations, C.B.S., 1944–1947. Since May 1947, Mr. Serrell has been engaged in research in Applied Mathematics and Electronic Computer Theory at the Princeton Laboratories of R.C.A. He is Chairman of the I.R.E. Electronic Computers Committee, and a member of Sigma Xi.

◆

C. E. Shannon

Claude E. Shannon (M'48–SM'49–F'50) was born in Petoskey, Mich., on April 30, 1916. He received the B.S. degree in electrical engineering from the University of Michigan in 1936, and the degrees of M.S. in electrical engineering and Ph.D. in mathematics from the Massachusetts Institute of Technology in 1940. He was a National Research Fellow in 1941 and, since then, has been with Bell Telephone Laboratories as a research mathematician, working in the fields of communication, theory, switching, and computing machines.

Dr. Shannon is a member of Sigma Xi and Phi Kappa Phi. He was awarded the Alfred Nobel Prize by the AIEE in 1940 and the Morris Leibmann Award by the IRE in 1941.

❖

Paul C. Sherertz

Paul C. Sherertz (S'42–A'45) was born in Soochow, China, on October 4, 1921. After receiving the B.S. degree in electrical engineering from Duke University in 1943, he was placed on active duty with the Navy and sent to the Naval Research Laboratory, where he was engaged in the design and operational evaluation of precision tracking radars and related electronic equipment.

Mr. Sherertz is now a member of the Operational Research Branch of the Naval Research Laboratory, and is currently doing research on electronic computers.

❖

Otto J. Smith

Otto J. M. Smith (M'44–SM'51) was born on August 6, 1917, in Urbana, Ill. He received in 1938 the B.S. degree in chemistry from Oklahoma Agricultural and Mechanical College and the B.S. degree in electrical engineering from the University of Oklahoma. He was a research assistant at the H. J. Ryan High Voltage Laboratory at Stanford University from 1938 until 1941, when he received the Ph.D. in electrical engineering.

Dr. Smith was an instructor in power and high voltage at Tufts College from 1941 to 1943; assistant professor of communications at Denver University 1943 and 1944; research engineer in the electronics department of the Westinghouse Research Laboratories in 1944 and 1945, and then chief electrical engineer of the Summit Research and Development Laboratory until 1947. He has been with the University of California since then, serving as Associate Professor since 1949.

Dr. Smith is a member of the A.I.E.E., American Chemical Society, American Physical Society, American Institute of Physics, American Association for the Advancement of Science, and American Society for Engineering Education. He is also associated with Sigma Xi, Phi Kappa Phi, Tau Beta Pi, Eta Kappa Nu, Phi Lambda Upsilon, Kappa Tau Pi, and Phi Eta Sigma.

❖

Robert E. Spero was born in New York, N. Y., on January 12, 1925. He attended Harvard University, receiving the B.S. degree in mathematics in 1945. In 1947 he received the M.A. degree in mathematics from Columbia University. He attended the Navy meterological training program at M.I.T. and served as an aerological officer in the Pacific during 1945 and 1946. In December of 1947, Mr. Spero joined the Sperry Gyroscope Company as an Assistant Project Engineer, where he participated in the development of a guided missile control computer. In 1948 Mr. Spero was promoted to the position of Project Engineer and continued his work in the field of guided missile computers. In 1949 he was assigned work in operations research in torpedo fire control. More recently, he has been concerned with the development of navigational and fire control computer systems of both analogue and digital types.

Robert E. Spero

❖

W. H. Thomas

W. H. Thomas was born on August 7, 1927. He received the B.S. degree in electrical engineering from Vanderbilt University in 1947.

Mr. Thomas has served as an electrical engineer for the Tennessee Valley Authority, Western Union Telegraph Co., and Headquarters, Air Materiel Command, Wright Field.

He joined IBM in 1952, and was assigned to the Computer Planning Group Here he has been concerned with the development of programs and programming techniques for scientific computers and data processing machines.

Mr. Thomas is a member of Tau Beta Pi.

❖

R. Thorensen

Ragnar Thorensen (S'42–A'47) was born on February 5, 1921 in Siglufjordur, Iceland. He received the B.S. degree in electrical engineering from the University of California, Berkeley, followed by the M.A. and Ph.D. from Stanford University in 1945 and 1949, respectively.

From 1946–1949 Dr. Thorensen was a research associate at Stanford, where he studied the nature of insulation breakdown in high-power pulse transformers.

In 1949 Dr. Thorensen joined the staff of the Electronics Lab., General Electric Co., Syracuse, N. Y. There he participated in the design and development of general-purpose large-scale automatic computers and special-purpose digital data-processing equipment.

In 1951, Dr. Thorensen became a member of the National Bureau of Standards, Applied Mathematics Division, and in 1952 was placed in charge of the development of electronic computers at the Bureau's Institute for Numerical Analysis, University of California, Los Angeles.

Dr. Thorensen is a member of Sigma Xi, AIEE, and ACM.

❖

Philip R. Vance

Philip R. Vance was born in Rock Island, Illinois, on December 2, 1922. He received the B.S. degree in electrical engineering from the Rose Polytechnic Institute in 1948, and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology in 1950.

Since 1950, Mr. Vance has been a development engineer with the Goodyear Aircraft Corporation, where he has worked on servomechanisms and analog computers. Mr. Vance is a member of Tau Beta Pi.

❖

H. Earle Vaughan

H. Earle Vaughan (SM'52) was born in Yonkers, N. Y., in 1912. He received the B.S. degree in civil engineering from Cooper Union in 1933, five years after joining Bell Telephone Laboratories' Transmission Research Department. He devoted several years to studies of voice operated devices and the effect of speech and noise on voice frequency signaling systems. In 1941 he turned to special Army and Navy projects, including anti-aircraft computers and fire control radar. Transferring to switching research in 1945, he has since been engaged in work on high-speed signaling devices, and is currently concerned with the development of future switching systems.

❖

J. H. Vogelsong

J. H. Vogelsong was born on October 30, 1925, in York, Pa. He received the B.S. degree in electrical engineering in 1949 from Lehigh University. During the summer before his senior year, Mr. Vogelsong was with the Bell Telephone Laboratories, assigned to trunk circuit testing, and he returned to the Laboratories in 1949, where he participated in the Communications Development Training

Program for three years. During the first year he also worked on a rotational basis with assignments in the switching systems development group, the switching apparatus development group and the transmission systems development group, in addition to an assignment in the switching research group of which he is now a member. He is currently engaged in the design of transistor circuits for use in a digital computer.

During World War II Mr. Vogelsong served with the U. S. Army Air Force. He is a member of Phi Beta Kappa, Tau Beta Pi, Eta Kappa Nu and Pi Mu Epsilon.

◆

Willis H. Ware (A'43–SM'49) was born in Atlantic City, N. J., on August 31, 1920, He received the B.S. degree from the University of Pennsylvania in 1941, and as a Tau Beta Pi Fellow, the S.M. degree from M.I.T. in 1942.

Willis H. Ware

From 1942–1946, he was employed by the Hazeltine Electronics Corporation for research and development in radar and IFF. In 1946, he became one of the original members of the staff of the Electronic Computer Project at the Institute for Advanced Study, Princeton, N. J. There he worked on the design and development of the large scale general purpose electronic digital computer which was later to set the pattern for the construction of several other "Princeton class machines." Simultaneously, he continued his graduate work at Princeton University from which he received the Ph.D. degree in 1951. In 1952, Dr. Ware joined the Rand Corporation, where he is continuing his work on digital machines.

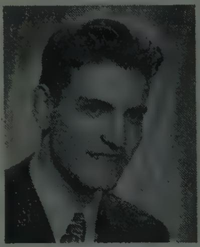
Dr. Ware is a member of Tau Beta Pi, Sigma Xi, Eta Kappa Nu and Pi Mu Epsilon, and serves as chairman of the Western Definitions Sub-Committee of the Electronic Computers Committee and on the paper procurement committee of the Professional Group on Electronic Computers of the IRE.

◆

David Wheeler was born in Birmingham, England on February 9, 1927 and attended Cambridge University, receiving his B.A. in 1948 and Ph.D. in 1951. He did research work in Cambridge Mathematical Laboratory, using the EDSAC. Since 1951 when he was awarded a research fellowship at Trinity College, he has been Visiting Assistant Professor of Mathematics at the University of Illinois and has been associated with the Digital Computer Laboratory of that University.

David Wheeler

Garland S. White (S'52) was born in Sudan, Texas, on April 6, 1928. He received the B.S. degree in 1952, and the M.S. degree in 1953, from the University of California at Berkeley.



Garland S. White

In 1951, he joined the Computer Laboratory at the University of California and was engaged in design work on electronic computers. Since July, 1953, he has been employed by Librascope Inc., of Glendale, California, as a Design Engineer.

Mr. White is a member of Tau Beta Pi, Eta Kappa Nu and an associate member of Sigma Xi.

◆

M. V. Wilkes was born in England on June 26, 1913. He went to St. John's College, Cambridge, in 1931, and was a Wrangler in the Mathematical Tripos of 1934. He worked on radio wave propagation at the Cavendish Laboratory and took the Ph.D. degree in 1938.

M. V. Wilkes

During World War II, Dr. Wilkes was engaged in radar development work and operational research, and at war's end was appointed Director of the University Mathematical Laboratory at Cambridge.

◆

Louis D. Wilson (M'46) was born in Philadelphia, Pa., on December 17, 1917. In 1941 he received the B.A. degree and in 1942 the M.A., both in physics from Temple University.

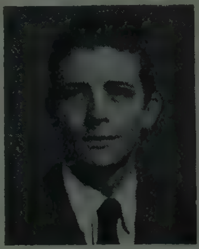
Louis D. Wilson

From 1942 to 1944 Mr. Wilson was a teaching fellow in physics at the Massachusetts Institute of Technology, and from 1944 to 1945 an instructor in electrical engineering.

He then became a research engineer at the Servomechanisms Laboratory, remaining until 1947. During this period he was concerned with the electrical design of the Whirl-wind computer, and was in charge of the development of arithmetic circuits.

Since 1947 Mr. Wilson has been with the Eckert-Mauchly Computer Corp., working on the logical design of the BINAC computer, the circuit design for the BINAC and UNIVAC computers, and also on the development of special input-output devices for use with the UNIVAC System. In 1951 he was named project engineer responsible for development of input-output devices.

Richard P. Witt (M'52) was born in Winchendon, Mass., on September 10, 1925. He received the B.S. degree in Metallurgical Engineering from Rensselaer Polytechnic Institute in 1944. He served as an engineering officer with the U. S. Navy until 1946. After release from the Navy he was employed as a Mechanical Engineer by the Goodspeed Machine Company at Winchendon, Mass. He entered the electronics field in 1947 with the Raytheon Mfg. Co. at Waltham, Mass., where he worked on the design of Guided Missiles and Electronic Computers. In 1948 he joined Melpar, Inc., of Alexandria, Va., and worked on high precision magnetic tape drives.

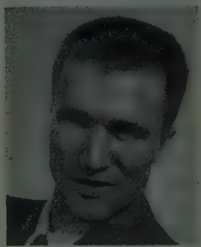


Richard P. Witt

Since 1949 he has been with the Electronic Computers Lab., National Bureau of Standards, working on the design of the mercury acoustic memory and the high-speed pulse circuitry for SEAC. In addition, he has been engaged in product engineering for the new NBS computer, the DYSEAC, and is presently in charge of its construction.

◆

Jesse B. Wright was born in Cambridge, Maryland, on August 14, 1920. He received from the University of Michigan in 1944 the B.S. degree, in 1945 the A.M. degree and in 1951 the Ph.D. degree, each in mathematics. His doctoral dissertation, which was on the foundations of geometry, was started in 1948 under an Office of Naval Research Fellowship.



Jesse B. Wright

Since 1949 Dr. Wright has been engaged in basic research on computing machinery at the University of Michigan under the sponsorship of the Burroughs Corporation. He is a member of Phi Kappa Phi, the Association for Computing Machinery and the American Mathematical Society.

◆

Everett C. Yowell was born in Cincinnati, Ohio, in 1920. He received the B.A. degree from the University of Cincinnati in 1941, and the M.A. and Ph.D. degrees from Columbia University in 1943 and 1948 respectively. He was Research Associate at the Thomas J. Watson Astronomical Computing Bureau from 1943 to 1946. Since 1948, he has been directing the activities of the computing group at the Institute for Numerical Analysis of the National Bureau of Standards.

E. C. Yowell

Institute News and Radio Notes

LAST AUTHORS CALL FOR IRE NATIONAL CONVENTION

The deadline for acceptance of papers for the 1954 IRE National Convention is November 16. B. R. Lester, Chairman of the Technical Program Committee, requests prospective authors submit the following information: (1) name and address, (2) title of paper, (3) a 100-word abstract, and additional information up to 500 words (both in triplicate). Address all material to Mr. Lester at IRE Headquarters, 1 East 79 St., New York 21, N. Y.

ALLEN B. DU MONT RECEIVES N. Y. SOCIETY AWARD

Allen B. Du Mont (M'31–F'31), president of Allen B. Du Mont Laboratories, Inc., received an award for distinguished service to the American people in the field of communications from the New York State Society of Professional Engineers at the Society's annual dinner held in New York City.

Mr. Du Mont organized his Laboratories in 1931 for the manufacture of cathode-ray tubes. He holds many patents, chiefly on cr tubes and television, and has written many technical papers on these subjects.

Mr. Du Mont is a Fellow of the American Institute of Electrical Engineers and the Television Society; a member of Sigma Xi; and is past president of Television Broadcasters Association, Inc. His Institute activities include serving on the Standardization, Standards, and Television Committees.

Calendar of COMING EVENTS

1953 IRE-RTMA Radio Fall Meeting, King Edward Hotel, Toronto, Ont., October 26–28

Conference on Radio Meteorology, University of Texas, Austin, November 9–12

IRE Kansas City Section Annual Electronics Conference, Hotel President, Kansas City, Mo., November 13 and 14

Microwave Radio Fall Symposium, Western Union Auditorium, New York, N. Y., November 5 and 6.

1954 Sixth Southwestern IRE Conference and Electronics Show, Tulsa, Okla., February 4–6

1954 IRE National Convention, Waldorf Astoria Hotel and Kingsbridge Armory, New York, N. Y., March 22–25

Society of Motion Picture & TV Engineers, 75th Annual Convention, Hotel Statler, Washington, D. C., May 3–7

ALBUQUERQUE-LOS ALAMOS SECTION RADIO ASTRONOMY LECTURES

The Albuquerque-Los Alamos Section is currently sponsoring a summer lecture series on radio astronomy jointly with the University of New Mexico.

Three lectures have been presented by Ralph Williamson, astronomical consultant of the Cornell Radio Astronomy Project and professor of astronomy at the University of Toronto, and currently a consultant at Los Alamos. The first lecture on the general subject was presented as one of the University's "Lectures Under the Stars." Dr. Williamson discussed "Solar Radio Astronomy" and "Stellar Radio Astronomy" in his other lectures.

A field trip to the U. S. Air Force Upper Air Observatory on Sacramento Peak was made in conjunction. Edward Schiffmacher demonstrated the Cornell radio telescopes and J. W. Evans the Harvard solar astronomical equipment.

If funds continue to be available, the Section hopes to make this lecture series an annual event.

CCIR ASSEMBLY HELD IN LONDON

The Seventh Plenary Assembly of the International Radio Consultative Committee (C.C.I.R.) was held in London, England, from September 3 through October 7. Approximately 300 representatives of 40 member countries attended this meeting to consider proposals submitted by the various countries on the technical radio problems before the Committee, and to formulate the course of its future work.

The C.C.I.R. is a committee of the International Telecommunication Union, advisory to the Union on Technical radio problems pertaining to its international regulatory work. The conclusions of the C.C.I.R. on these influence, in an important way, future actions and decisions of the I.T.U. on such matters as frequency allocation and international radio regulations.

The work of the C.C.I.R. is carried on, in the interim between Plenary Assemblies, by 14 Study Groups. Each Study Group is assigned a series of topics, which in the aggregate constitutes a broad coverage of the entire range of technical radio problems dealt with by the C.C.I.R. Typical subjects on which the United States, as a member country of the C.C.I.R., has submitted proposals to the Seventh Plenary Assembly, are: bandwidths of emissions, noise and sensitivity of receivers, bandwidths and signal-noise ratios in complete systems, tropospheric propagation curves, review of VHF ionospheric propagation, standard frequency transmissions and time signals, measurement of field strength, power relationships for modulated emissions, and disturbances in television receivers resulting from harmonics and other non-essential radiations from radio transmitters.

In the United States the preparatory work for the Assembly was conducted through groups of representatives of interested government agencies and of private telecommunication interests, set up under the auspices of the Department of State. The delegation of the United States to the Assembly was composed principally of government and private industry officials who have participated in the work of these preparatory groups.

JOINT COMPUTER CONFERENCE AND EXHIBITION

Information processing systems—reliability and requirements, is the theme of the Joint AIEE-IRE-ACM Computer Conference and Exhibition to be held at the Statler Hotel, Washington, D. C., December 8–10, 1953.

The program includes papers describing the reliability of existing large-scale electronic digital computing machines as well as other papers describing reliability requirements for certain necessary applications in the field of government, business, and industry. Inspection trips will permit actual demonstrations of the topics under discussion. A large exhibit area will bring together the products of more manufacturers for this conference than has ever been possible before.

Preliminary programs and reservation applications will be mailed shortly to all members of the sponsoring organizations which include the American Institute of Electrical Engineers, the IRE, and the Association for Computing Machinery. Others may request this information by writing L. R. Johnson, Registration Committee Chairman, 2018 Sycamore Drive, Falls Church, Va.

UNIVERSITY COURSES IN MACHINE COMPUTATION

A few of the universities having facilities and the machines available for laboratory work and training in machine computation are: the University of California, Los Angeles, Calif., SWAC; Columbia University, New York, N. Y., IBM 701; Harvard University, Cambridge, Mass., Mark I and IV; the University of Illinois, Champaign, Ill., ILLIAC; Massachusetts Institute of Technology, Cambridge, Mass., Whirlwind; the University of Michigan, Ann Arbor, Mich., MIDAC; and Wayne University, Detroit, Mich., Burroughs Computer.

Universities which have conducted intensive summer course are MIT, the University of Michigan, the University of Toronto and Wayne University.

Universities offering courses and in the process of providing computers are the University of California, the University of Pennsylvania, Purdue University and the University of Wisconsin.

MICROWAVE RADIO RELAY SYSTEMS SYMPOSIUM

A symposium sponsored by the Professional Groups on Communications Systems, Microwave Theory and Techniques, and Electron Devices is to be held on November 5 and 6, 1953, in the Western Union auditorium, 60 Hudson Street, New York, N. Y.

Technical sessions are to be held in the morning and afternoon of each day. Detailed registration information will be circulated to the members of the three Professional Groups sponsoring the symposium by early October.

A list of authors and their papers is as follows: W. P. Maginnis, Federal Telephone and Radio Co., "The Microwave System of the Michigan-Wisconsin Pipe Line Co."; H. A. Rhodes, Transcontinental Pipe Line Co., "The Microwave System of the Transcontinental Gas Pipe Line Co."; P. F. Godley, Paul Godley Co., "Various Microwave Radio Relay Systems"; Sidney Metzger, Federal Telecommunication Laboratories, "Microwave Radio Relay Link for Military Use"; G. W. Fox, Union Electric Co. of Missouri, "A 960 and 2000 mc Microwave System for Electric Utility Service"; Ed Dyke, Motorola, Inc., "A Microwave Relay System for Pipe Line Use"; J. J. Lenehan, Western Union Telegraph Co., "Microwave System for Trunk Service"; R. L. Halverson, Westinghouse Electric and Manufacturing Co., "Remote Control of Standby Engine Generator Sets Over a Microwave System"; G. A. Deschamps, Federal Telecommunications Laboratories, "Theoretical Aspects of Microstrip Wave Guides"; E. J. Rudisuhle, Lenkurt Electric Co., "The Application of Compandors to FM Radio Systems with Frequency Division Multiplexing"; N. B. Tharp, Westinghouse Electric and Manufacturing Co., "Double Sideband AM Frequency Division Multiplex for Use on Microwave"; J. R. Pierce, Bell Telephone Laboratories, "Microwave Amplifier Tubes for Relay Systems"; A. J. Vadasz, General Electric Co., "Use of the 2C39A UHF Triode in Microwave Communications"; W. W. Siekanowicz, RCA Victor Division, RCA, "Engineering a Medium Power Traveling Wave Amplifier for 2000 Mc. Relay Service"; Robert Olthuis, Sperry Gyroscope Co., "Considerations in Klystron Design for Microwave Relay Service"; A. C. Beck, Bell Telephone Laboratories, "Microwave Testing with Milli-Micro-Second Pulses"; and E. G. Lomas, PSC Applied Research Ltd., "A Method of Microwave Site Selection." The Canadian General Electric Co. will discuss microwave repeater site planning in undeveloped country.

TECHNICAL COMMITTEE NOTES

The **Standards** Committee convened on July 9 under the chairmanship of A. G. Jensen. The Ad Hoc Committee's report on reorganizing the Standards Committee's procedure on definitions work was reviewed in detail. The motion was made and carried unanimously that M. W. Baldwin, Jr., be made Chairman of the committee, with Messrs. E. Weber, J. G. Brainerd, R. F. Shea and C. H. Page serving as initial members. It is expected that the membership of the committee will change periodically, depending on the standards material under consideration. The new procedure is to be given a year's trial. If it proves impractical another approach to expediting the work will be tried. Recommendations made by the Electronic Computers Committee with respect to revisions to ASA C42 terms were approved. Proposed Standards in the Field of Linear Varying Parameter and Nonlinear Circuits: Definitions of Terms, as presented by the Circuits Committee, were discussed and adopted. Two proposed standards submitted by the Audio Techniques Committee; namely, Proposed Standards on Audio Techniques: Definitions of Terms, and Proposed Revisions to the 1942 Standards on American Recommended Practice for Volume Measurements of Electrical Speech and Program Waves were reviewed and minor modifications suggested. Both standards were adopted and will be published in the PROCEEDINGS.

Under the chairmanship of D. C. Ports the **Antennas and Waveguides** Committee met on June 10. The question of preparing an introduction to the proposed list of definitions for Standard Waveguide Terms was discussed. P. H. Smith with the aid of a subcommittee had prepared a tentative introduction. Copies were distributed and after some discussion and modification a form was adopted for presentation to the Standards Committee. A discussion of the actions to date by the Standards Committee in considering the proposed Waveguide definitions was held. The subject of Annual Review material was discussed as the result of a letter distributed by Col. J. Z. Millar, the new Annual Review Chairman. It was suggested that in recognition of the excellent work done by John Ruze in preparing the Antennas and Waveguides material for the 1952 Annual Review he would be well-qualified to again perform this work as the coordinator and representative of this committee on the Annual Review Committee. The committee agreed to assist Mr. Ruze in the preparation of the written text. The committee also took action on a number of Component definitions.

On June 11 the **Information Theory and Modulation Systems** Committee met under the chairmanship of W. G. Tuller. A tentative definition for "Information Rate" was arrived at by the committee. The term "Nyquist Interval" was discussed by the committee. It was agreed that committee members would attempt to bring definitions for this term to the next meeting. Nathan Marchand suggested the possibility of defining "inverse probability" and terms relating to this type of analysis. This brought up the whole question of the propriety of this group defining mathematical terms in the sense used in mathematics. J. G. Kreer agreed to request policy clarification from the Standards Committee on this point.

Committees of the Professional Group on Electronic Computers

JULY 1, 1953–JUNE 30, 1954

ADMINISTRATIVE COMMITTEE

J. H. Howard, *Chairman*
Burroughs Corp.
511 N. Broad Street
Philadelphia 23, Pa.

H. T. Larson, *Vice-Chairman*
Hughes Aircraft Co.
Florence & Teale Streets
Culver City, Calif.

J. R. Weiner, *Sec.-Treas.*
Remington Rand, Inc.
2300 W. Allegheny Avenue
Philadelphia 29, Pa.

S. N. Alexander
National Bureau of Standards
Washington 25, D. C.

M. M. Astrahan
IBM Engineering Lab.
Box 390
Poughkeepsie, N. Y.

J. H. Felker
Bell Telephone Labs.
Whippany, N. J.

D. H. Gridley
USN Research Lab.
Radio Div. III, Code 3621
Washington 25, D. C.

H. H. Goode
Univ. of Michigan
Willow Run Res. Center
Ypsilanti, Mich.

J. L. Hill
Remington Rand, Inc.
1902 W. Minnehaha Ave.
St. Paul W. 4, Minn.

H. D. Huskey
Wayne Univ.
5402 Second Ave.
Detroit 1, Mich.

W. L. Martin
Telecomputing Corp.
133 E. Santa Anita Ave.
Burbank, Calif.

R. E. Meagher
Univ. of Illinois
Urbana, Ill.

T. H. Meisling
Univ. of California
Berkeley 4, Calif.

T. A. Rogers
Univ. of California
Los Angeles, Calif.

N. H. Taylor
Mass. Inst. of Tech.
68 Albany Street
Cambridge 39, Mass.

STANDING COMMITTEES

Membership Committee:
I. L. Auerbach, *Chairman*
Burroughs Corp.
511 N. Broad Street
Philadelphia 23, Pa.

Meetings Committee:
W. L. Martin, *Chairman*
Telecomputing Corp.
133 E. Santa Anita Ave.
Burbank, Calif.

Publications Committee:
W. Buchholz, *Chairman*
IBM Engineering Lab.
Box 390
Poughkeepsie, N. Y.

Sectional Activities Committee:
W. K. Halstead, *Chairman*
R.C.A. Victor
Building 10-8
Camden 2, N. J.

AD HOC COMMITTEES

Awards:
E. G. Andrews, *Chairman*
Bell Telephone Labs.
463 West Street
New York 14, N. Y.

Bylaws Procedures
D. H. Gridley, *Chairman*
USN Research Laboratory
Radio Div. III, Code 3621
Washington 25, D. C.

PGEC 1954 National Convention Committee:
J. L. Hill, *Chairman*
Remington Rand, Inc.
1902 W. Minnehaha Ave.
St. Paul W. 4, Minn.

CHAPTER OFFICERS

Los Angeles
L. L. Kilpatrick, *Chairman*
N. American Aviation Inc.
12214 S. Lakewood Blvd.
Downey, Calif.

E. E. Bolles, *Secretary*
Hughes Aircraft Co.
Florence & Teale Streets
Culver City, Calif.

Philadelphia
J. M. Broomall, *Chairman*
Brown Instrument Co.
Wayne & Windrim Avenues
Philadelphia 44, Pa.

G. Palmer, Jr., *Secretary*
Technitrol Engineering Co.
2751 N. 4th Street
Philadelphia 33, Pa.

San Francisco
T. H. Meisling, *Chairman*
Univ. of California
Berkeley 4, Calif.

J. D. Noe, *Sec.-Treas.*
Stanford Research Institute
Menlo Park, Calif.

Washington, D. C.
C. V. L. Smith, *Chairman*
Office of Naval Research
Building T-3, Room 2715
Washington 25, D. C.

R. J. Slutz, *Secretary*
National Bureau of Standards
Washington 25, D. C.

SECTIONAL ACTIVITIES REPRESENTATIVES

Akron
C. D. Morrill
Goodyear Aircraft Corp.
Dept. 29
Akron 15, Ohio

Boston
B. M. Gordon
Lab. for Electronics, Inc.
11 Leon Street
Boston, Mass.

Detroit
H. D. Huskey
Wayne University
5402 Second Avenue
Detroit 1, Mich.

New York
R. F. Shaw
Underwood, Elec. Comp. Div.
160 Ave. of the Americas
New York 13, N. Y.

PGEC REPRESENTATIVES

The Joint AIEE-ACM-IRE Computer Committee

J. H. Howard, *Chairman*
M. M. Astrahan
J. D. Noe
W. L. Martin
J. R. Weiner

Radio Fall Meeting Program

SPONSORED BY IRE, RETMA, AND RTMA OF CANADA

KING EDWARD HOTEL, TORONTO, ONTARIO, CANADA—OCTOBER 26–28

Monday, 9:30 A.M., October 26

TELEVISION INTERFERENCE SYMPOSIUM

(Sponsored by the RETMA Engineering Department)

W. R. G. Baker, *presiding*

"The Industry Record to Date," L. M. Clement, Crosley Div., Avco Mfg. Corp.

"Spurious Radiations from Television Receivers," K. A. Chittick, RCA.

"Spurious Radiations from Television Transmitters," J. E. Keister, General Electric Co.

"Measurements and Standards for Control of Spurious Radiation," S. L. Bailey, Consulting Engineer

"Color TV and the Radio Amateur—A Cooperative Achievement in the Study of Spurious Radiation," E. I. Anderson, RCA Industry Service Labs. and George Grammer, American Radio Relay League

"Industry-wide Cooperation under the JTAC Spurious Radiation Program," D. G. Fink, Philco Corp.

2:00 P.M.

ELECTRONICS RELIABILITY SESSION

(Arranged by IRE Professional Group on Quality Control)

J. R. Steen, *presiding*

"Program on Reliability of Electronic Equipment," L. M. Clement, Crosley Div., Avco Mfg. Corp.

"Report on U.K. Project to Improve Valves for Military Applications," F. H. Powell, British Joint Services Mission

"The Panel on Electron Tubes Program for Coordinating Tube Reliability," L. S. Schwartz, P.E.T. Secretariat, New York Univ.

"Inspection Procedures for MIL-E-1B Reliable Electron Tubes," R. J. E. Whittier, Raytheon Mfg. Co.

"Those Unreliable Thermionic Tubes," W. R. Jones, Cornell Univ.

8:00 P.M.

Television Session

(Arranged by IRE Professional Group on Broadcast and Television Receivers)

E. W. Engstrom, *presiding*

"National Television System Committee Field Tests," Knox McIlwain, Hazeltine Electronics Corp.

Tuesday, 9:00 A.M., October 27

Color Television Session

(Arranged by the IRE Professional Group on Broadcast and Television Receivers)

R. B. Dome, *presiding*

"Gamma Correction and Color Fidelity," F. J. Bingley, Philco Corp.
"Operation of the Chromatron on NTSC, Standards," Don Gow and Roger Dorr. Chromatic Television Laboratories Inc.
"The D. C. Quadricorrelator," Donald Richman, Hazeltine Electronics Corp.
"Color Decoder Simplifications Based on a Beam Deflection Tube," R. Adler and Charles Heuer, Zenith Radio Corp.
"Pulsed Envelope Detection of Color Signals," (with demonstration) K. Schlesinger, Motorola Inc.

2:00 P.M.

Monochrome and UHF Session

(Arranged by the IRE Professional Group on Broadcast and Television Receivers)

D. D. Israel, *presiding*

"Improving the Transient Response of Television Receivers," Jack Avins, RCA
"Instrumentation for Experimental Investigation of Automatic Frequency Control Systems," W. J. Gruen, General Electric Co.
"A Planar Triode Amplifier for UHF Television," S. C. Peek and Byron Stokes, Sylvania Electric Products Inc.
"A Transistor Personal Broadcast Receiver," L. E. Barton, RCA

Tuesday Evening

Radio Fall Meeting Dinner

(Sponsored by the RTMA of Canada)

Wednesday, 9:30 A.M., October 28

Electron Devices Session

(Arranged by IRE Professional Group on Electron Devices)

G. A. Espersen, *Presiding*

"A Color Picture Tube of Advanced Design," N. F. Fyler, W. E. Rowe, and C. W. Cain
"Investigation of VHF Television Amplifier Tubes," W. Y. Pan, RCA
"Picture Tubes for Color Television," C. G. Lob, General Electric Co.
"The Double Base Diode—A Semi-Conductor Thyratron," R. A. Aldrich and I. A. Lesk, General Electric Co.

2:00 P.M.

Electron Devices Section II

(Arranged by IRE Professional Group on Electron Devices)

J. S. Saby, *Presiding*

"Application Considerations for RCA Commercial Transistors," R. M. Cohen, RCA
"A P-N-P Triode Alloy Junction Transistor for R.F. Amplification," J. I. Pankove and C. W. Mueller, RCA
"The Transistor as a Network Element," J. T. Bangert, Bell Telephone Labs.
"Some Applicational Aspects of Tetrode Transistors," L. Dwork, C. Huang, and W. Palmer, Sylvania Electric Products Inc.
"A Hermetically Sealed PNP Alloy Diffusion Transistor for Medium Power Applications," C. H. Zierdt, General Electric Co.

Conference on Radio Meteorology

THE UNIVERSITY OF TEXAS, AUSTIN, TEXAS—NOVEMBER 9–12

Sponsored by the American Meteorological Society, the Professional Group on Antennas and Propagation of the IRE, the Radar Weather Conference, National Commission II on Tropospheric Propagation of the URSI, and the Joint Commission on Radio Meteorology of the International Scientific Union

All sessions of the Conference on Radio Meterology will be held in the auditorium of Batts Hall on the campus of The University of Texas, Austin, Texas.

Hosts for the Conference will be the Central Texas Branch of the American Meteorological Society and the Austin-San Antonio Section of the Institute of Radio Engineers.

Registration fees, which will include a copy of the Proceedings, will be $4.00. The price of the Proceedings alone will be $3.00. Barbecue fees have been set at $1.50 per person. Further information may be obtained by writing to the Conference on Radio Meteorology, Box 8026, University Station, Austin, Texas.

The daily program is as follows.

Monday 9:00 A.M., November 9

Welcome to Delegates

Dr. Logan Wilson, President, The University of Texas, *Introduced by* A. W. Straiton, Director Electrical Engineering Research Laboratory, University of Texas

Session 1: Tropospheric Propagation
Chairman, J. B. Smyth, U. S. Navy Electronics Laboratory

Monday, 2:00 P.M., November 9

Session 2: Tropospheric Propagation

Chairman, W. E. Gordon, School of Electrical Engineering, Cornell University

Monday, 8:30 P.M., November 9

Social Evening

(Mezzanine Floor, Driskill Hotel)

Tuesday, 9:00 A.M., November 10

Session 3: Refractive Index Meteorology

Chairman, T. J. Carroll, Lincoln Laboratory, M.I.T.

Tuesday, 11:30 A.M., November 10

Session 4: Atmospheric Scattering and Turbulence

Chairman, H. G. Booker, Prof. of Electrical Engineering, Cornell University

Tuesday, 2:00 P.M., November 10

Session 4: *Continued*

Tuesday, 3:00 P.M., November 10

Session 5: Thunderstorm and Tornado Atmospherics

Chairman, L. A. Pick, Evans Signal Laboratory

Tuesday, 8:00 P.M., November 10

Session 6

Chairman, David Atlas, Geophysics Research Div., Air Force Cambridge Research Center

Wednesday, 9:00 A.M., November 11

Session 7: Cloud and Precipitation Physics

Chairman, H. R. Byers, Chairman, Dept. of Meteorology, University of Chicago

Wednesday, 2:00 P.M., November 11

Session 8: Cloud and Precipitation Physics

Chairman, A. F. Spilhaus, Dean, Institute of Technology, University of Minnesota

Wednesday, 3:30 P.M., November 11

Session 9: Radar Rainfall Determination

Chairman, A. C. Bemis, Weather Radar Research, M.I.T.

Wednesday, 6:45 P.M., November 11

Texas Barbecue: Place to be announced

Thursday, 9:00 A.M., November 12

Session 10: Operational Uses of Weather Radar

Chairman, G. E. Stout, Illinois State Water Survey

Thursday, 2:00 P.M., November 12

Session 11: Operational Uses of Weather Radar

Chairman, J. S. Marshall, Assoc. Prof. of Physics, McGill University, Canada

SUMMARIES OF TECHNICAL PAPERS

1. TROPOSPHERIC PROPAGATION WELL BEYOND THE HORIZON —A REVIEW

Thomas J. Carroll
(M.I.T.)

Reliable propagation of VHF and microwaves from high power transmitters to distances of several hundred miles beyond optical range has been demonstrated by an ever increasing number of experiments during the last ten years. Taken collectively, these experiments demonstrate conclusively that the fields, though weak, are very much stronger and more reliable than had been predicted from standard theory. Three explanations have been offered in recent years. (a) The extra field may conceivably come from scattering by the blobby structure of the air of the troposphere, caused by the turbulent fluctuations of air density or humidity. (b) Deviations of the earth's surface from smooth sphere of theory have been suspected, and the effect of a knife edge obstacle has been especially carefully worked out. (c) The effect of molecular scattering by the dielectric composing the atmosphere has been more completely calculated (sometimes called "partial internal reflection"), and rather startling similarity with experiment has been demonstrated for a model atmosphere consisting of a finite linearly stratified air layer 10 km thick. A provisional estimate of the roles of the three complementary and not incompatible explanations can be made. The great probable importance of these weak fields well beyond the horizon to radio technology can be said to come from their omnipresence at all times and places, and in all frequency bands, for systems employing sufficiently high power and antenna gain.

2. PROPAGATION CHARACTERISTICS OF 0.86 CENTIMETER RADIO WAVES

C. W. Tolbert and A. W. Straiton
(The University of Texas)

Recent developments in generating equipment for 8.6 millimeter radio waves have made possible the propagation of this wavelength over considerable distances. On path lengths up to 50 miles, the signal level was in general agreement with the free space value corrected for absorption due to water vapor and oxygen in the atmosphere.

Signal fluctuations appeared to be controlled by the amount of inhomogeneity of the index of refraction of the atmosphere.

Steady signals with small loss due to water droplets were experienced in fog, but severe attenuation was caused by rain showers.

3. SOME MEASUREMENTS OF FADING AT A WAVELENGTH OF 8 MM OVER A VERY SHORT SEA PATH

D. G. Kiely
(Admiralty Signal and Radar Establishment, England)

In this paper are described the results of a pilot experiment designed to investigate the magnitude of super-refraction effects in the 8 mm band.

Records of signal fading on a one-mile over-sea path with a low transmitter (15′) and a high receiver (100′) indicate that these effects are very large and may have serious operational consequences when paths of several miles are concerned.

Fades due to refraction effects are summarized. Other fading observations by different workers using radar equipment confirm the order of magnitude of these figures.

4. CALCULATED CENTIMETER-MILLIMETER WATER VAPOR ABSORPTION AT GROUND LEVEL

T. F. Rogers
(Air Force Cambridge Research Center)

Water vapor is one of the two major absorption constituents in the earth's lower atmosphere at centimeter and millimeter wavelengths. As such, it places a fundamental limitation on the exploitation of these short radio wavelengths, and a quantitative estimate of expected absorption coefficients is desired. Extensive and detailed calculations of the water molecule resonant frequencies and line peak intensities have been made on a quantum-mechanical basis for H_2O^{16}, H_2O^{18}, and $H^1D^2O^{16}$ isotopic species in their naturally occurring abundances for $\lambda \geqq 0.5$ millimeter. Applying the Van Vleck-Weisskopf equation for collision-broadened lines to these individual resonant frequencies and that portion of the far infra-red spectrum which extends down into this region, the entire water vapor absorption spectrum has been calculated for the average—1%—vapor concentration found at ground level in the temperate zone. While the low abundance H_2O isotopes introduce a further irregularity of the absorption-wavelength dependence, the departures from the earlier calculations by Van Vleck are not of first order, and it is now believed that all important contributions have been accounted for. The accuracy of the calculations will be discussed as will also the effect of the more prominent features upon propagation losses.

5. CHARACTERISTIC EFFECTS OF ATMOSPHERIC STRATIFICATION ON AIR-TO-AIR RADIO PROPAGATION

Paul B. Taylor
(Wright Air Development Center)

Frequent soundings with an airborne radio refractometer in the Ohio Valley show that the occurrence of thin strata of air of abnormal refraction is very common. These strata may be found up to at least twelve thousand feet altitude, but mostly below nine thousand feet. Emphasis in the present paper is on layers between three thousand and nine thousand feet. Analytic treatment of the gradient of the refraction has progressed to the point where the characteristic effects of these layers on radio propagation may be derived analytically. Examples of typical layers will be shown. Their effects on radio propagation will be deduced and compared with the air-to-air radio transmissions actually observed simultaneously with the refractometer soundings.

6. IMPORTANT MODES IN THE TROPOSPHERE TREATED AS A LINEARLY GRADED LAYER OF DIELECTRIC

Thomas J. Carroll and Rose M. Ring
(M.I.T.)

The weak average fields propagated from high power transmitters to distances of several hundred miles beyond the horizon can be satisfactorily calculated if the troposphere be treated as a linearly graded layer of dielectric. The calculation, for fixed antenna heights, involves a number of modes, but fortunately, the only important ones are those with phase velocities nearly the same as that of radiation following the "stretched string path" around the earth bulge, through the terminals. The wave functions may be conveniently requested in the complex plane in the manner of Freehafer. One reason why conventional 4/3 earth diffraction curves become bogus deep in the diffraction region can be understood.

7. RAIN CLUTTER MEASUREMENTS WITH C.W. RADAR SYSTEMS OPERATING IN THE 8 MM WAVELENGTH BAND

D. G. Kiely
(Admiralty Signal and Radar Establishment, England)

A program of millimeter wave propagation experiments is described. The objects of this program were to investigate the extent of rain clutter using 8 mm C.W. Radar Systems with both a single antenna (common T and R) and dual antennas (separate T and R) and to investigate the reduction of this clutter by orthogonal polarization techniques. Details of the methods of measurement, equipments used and of the experimental observations are given.

Results show: (1) that there is a very major difference in level between clutter measured with a single and with a dual antenna system, (2) that clutter is not very dependent on rainfall rate and (3) that there is a well defined maximum useful antenna separation beyond which little reduction of rain clutter is achieved.

In an Appendix some data on the world distribution of rainfall is presented as the results of a collateral investigation to assist in determining the operational significance of the measured rain clutter figures.

8. FIELD STRENGTH DETERMINATION BY RAY TRACING TECHNIQUES FOR HORIZONTALLY STRATIFIED LAYERS

B. M. Fannin
(The University of Texas)

Measurements by refractometers mounted

in aircraft indicate that over practically all areas there commonly exist layers (usually below 10,000 ft.) in which the refractive index vs. height profile differs markedly from the almost constant lapse rate expected for a well mixed atmosphere. Microwave propagation can be greatly affected by the presence of these layers. Theoretical contours of constant field strength have been drawn for a group of simple refractive index vs. height profiles (trilinear) with the layer thickness, the layer strength, and the location of the transmitter relative to the layer systematically selected. It is hoped that these plots will give the meteorologist a better insight into the operational characteristics of radar, a tool becoming very extensively used in his field, and also into some of the types of meteorological data that are of great value to those faced with the propagation problem.

9. THE ANOMALOUS PROPAGATION OF THE LONGER VHF WAVES

Francis H. Northover
(Memorial University, St. Johns, Canada)

Anomalous propagation of meter waves, which is occasionally observed, cannot be explained, as in the case of centimeter waves, by the effects of surface inversions but it is now established that it can be caused by a single strong and sharp elevated inversion.

It has, however, been recently noted that, when such a sharp inversion is not present, the long distance field, although much weaker, is still quite often many orders of magnitude larger than the value appropriate to a homogeneous atmosphere, even when attempts are made to allow for the effect of surface inversions.

It is shown in the present paper that this phenomenon could be caused by the occurrence together of several relatively weaker high level inversions.

10. FACTORS INFLUENCING PROPAGATION OF VHF WAVES IN THE DIFFRACTION ZONE

W. G. Albright and R. N. Ghose
(University of Illinois)

Signal strengths measured in the diffraction zone, with propagation over essentially a smooth earth, are classified into five distinct groups dependent on the amplitude of the signal and its rate of change. These groups are:

1. relatively constant signal
2. oscillating signal about a median
3. slow fading signal
4. median fading signal
5. fast fading signal

Each group is analyzed both from meteorological considerations and propagation conditions and an attempt is made to describe the type of propagation contributing to the signal pattern.

An investigation is also made to determine the effect on propagation of a layer of finite thickness whose dimensions are comparable to a wavelength and whose conductivity is relatively large. This simulates the condition of a cloud, with a high concentration of water vapor, on the propagation path. A theoretical analysis is made of the condition and the results compared to experimental data.

11. A REVIEW OF THE NATIONAL BUREAU OF STANDARDS TROPOSPHERIC PROPAGATION RESEARCH PROGRAM IN THE 100–1000 MC REGION

Jack W. Herbstreit
(National Bureau of Standards)

The National Bureau of Standards has been conducting a comprehensive study of tropospheric propagation within the United States in the 100–1000 mc region. This program has included studies of terrain and meteorological effects on transmission loss both within and beyond the line of sight. Experimental transmission loss measurements by universities and other contracting groups over a wide range of climatic conditions have supplemented the extensive experimental program of study at the National Bureau of Standards Cheyenne Mountain Field Station at Colorado Springs, Colorado. Considerable progress has been made in advancing theoretical explanations for the experimental results in terms of modification of smooth earth diffraction theory to include the effects of irregular terrain, climatic conditions, knife edge diffraction, and scattering by a turbulent atmosphere.

12. PROLONGED SPACE-WAVE FADEOUTS OF THE 1046 MC CHEYENNE MOUNTAIN EXPERIMENT

Bradford R. Bean
(National Bureau of Standards)

During the first year of continuous operation of the Cheyenne Mountain propagation experiment the 1046 mc receiving locations within the radio horizon have exhibited fadeouts in excess of 20 db below the monthly median level and lasting from a minute up to several hours. The occurrence of these fadeouts has been found to coincide with widespread nocturnal super-refraction as evidenced by enhanced signals beyond the line-of-sight and ground modification of the refractive index profile.

13. THE METEOROLOGICAL INSTRUMENTATION AT THE CHEYENNE MOUNTAIN FIELD STATION

M. C. Thompson and K. O. Hornberg
(National Bureau of Standards)

The Cheyenne Mountain Field Station of the National Bureau of Standards at Colorado Springs, Colorado, is conducting a radio meteorology program to obtain meteorological data along the path over which radio propagation measurements are concurrently being made. The major fixed field installation is in operation and is located at Haswell, Colorado, approximately on the radio horizon 96 miles from Cheyenne Mountain. This installation consists of a 500-foot tower instrumented to measure vertical profiles of refractive index, temperature, relative humidity, wind direction and velocity, continuously and unattended. The discussion will center on the characteristics of the instruments involved, their installation and behavior under field conditions and the data obtained. The instruments in use to date include both commercially available and special types.

14. SUMMARY AND PRELIMINARY ANALYSIS OF TROPOSPHERIC REFRACTIVE INDEX MEASUREMENTS

C. M. Crain and J. R. Gerhardt
(The University of Texas)

The development of the microwave refractometer as a new and sensitive instrument for the determination of certain meteorological and radio propagation characteristics of the atmosphere is briefly reviewed. Earlier simultaneous observations of temperature and refractive index fluctuations near the earth's surface have given evidence on the scale and intensity of turbulence in the surface layers and on the turbulent transfer of heat and moisture vapor. Later models of the refractometer have been adapted for aircraft observation to obtain refractive index profiles and fluctuations from near the surface up to 25,000 feet. The tropospheric measurements to date have been made over many U. S. coastal and interior regions over a wide range of climatic conditions. Current observation programs will extend refractometer coverage to Alaskan and Florida sites with some flights scheduled for elevations up to 40–50,000 feet or more. These refractive index distributions will be briefly summarized and preliminary analyses will shed light on the geographical, climatological and altitude variations of the distributions and on their interpretation in terms of effects on radar propagation and of advances in our knowledge of the meteorology of the troposphere.

15. THE MONTHLY REFRACTIVITY GRADIENT FOR THE UNITED STATES AND ITS APPLICATION TO PREDICTING THE GEOGRAPHICAL AND ANNUAL TREND OF VHF TRANSMISSION LOSS

Bradford R. Bean and
Frances M. Meany
(National Bureau of Standards)

Climatic maps of monthly average refractivity gradient are presented for the United States for the hours 0300 and 1500 G.C.T. These maps are shown to follow a regular climatic pattern. The refractivity gradients as obtained from individual monthly maps are then correlated with the monthly median transmission loss of all available VHF propagation paths. The usefulness of this approach for the prediction of VHF transmission loss is described.

16. A RADIO CLIMATOLOGY SURVEY OF THE U. S.

Leslie W. Cowan
(Third Weather Group, Ent Air Force Base)

Parameters are defined to present the features of prominent nonstandard layers in the atmosphere and the relation of these parameters to physical processes in the atmosphere is indicated.

Data obtained from airborne microwave refractometer measurements in or near Washington, California, Rhode Island, New Jersey and Ohio are analyzed to determine the characteristics of nonstandard layers. A similar analysis is presented for the 0300Z radiosonde observations over a five-year period at fifteen selection stations in the U. S. Comparisons are made of these data.

Interpretation of these data by ray theory using differential analyses and analytical techniques is discussed briefly.

17. PREDICTION OF DIURNAL FIELD STRENGTH PATTERNS BY SYNOPTIC METHODS

Frank R. Bellaire and William A. Arvola

(U. S. Navy Electronics Laboratory)

Predicted vs. actual diurnal patterns of hourly median field strength for a 100 mc Dallas-Austin link are presented. Methods of selecting typical diurnal field strength patterns based on types of synoptic situations during a control month are discussed. Predictions of diurnal field strength patterns are made for following months considering the synoptic type existing over the link hour by hour.

18. VERIFICATION OF SURFACE-DUCT PROPAGATION PREDICTIONS

L. J. Anderson and E. E. Gossard

(U. S. Navy Electronics Laboratory)

Refractive index profiles within a surface duct over the sea are deduced from measurements at two levels using the Deacon model. The effect of such profiles are then determined using Schelkunoff's method.

Predictions of whether or not trapping should occur are verified using experimental data at 3, 10 and 25 cm wavelengths. British data taken over Cardigan Bay are used for overwater ducts and similar procedures are applied to overland data taken by the Navy Electronics Laboratory in Arizona.

19. RADAR FORECASTING ON LAKE ONTARIO

A. D. Hood and Lorne H. Doherty

(National Research Council, Canada)

Preliminary attempts to forecast radar performance on Lake Ontario on a synoptic weather basis are described. The work is based on some eighteen months of observations with a 3-centimeter radar which moves continuously in the height range 8 feet to 220 feet above lake level. Photographs are taken of the PPI display approximately every ten feet of travel. During trapping conditions echoes are obtained from the opposite shoreline at ranges between 30 and 50 miles. The low ducts (less than 50 feet) obtained during times of neutral equilibrium are compared with predictions based on the logarithmic distribution of mean wind speed. The higher ducts associated with stable equilibrium are compared with predictions based on the power law theory of diffusion. The possibilities of supplying merchant shipping on the Great Lakes with a regular radar forecasting service is discussed.

20. RADIO SCATTERING FROM A TURBULENT ELEVATED LAYER

W. E. Gordon

(Cornell University)

Airborne refractometer observations indicate that turbulent elevated layers occur frequently. Within the layer the scale is observed to be somewhat larger and the intensity many times the values of these quantities observed above or below the layer. The scattered power from the layer received at certain distances may easily equal or exceed that from an atmosphere without a layer. The effect of turbulent elevated layers on fixed paths is to increase the range of scattered power observed, whereas for a moving receiver the scattered power as a function of distance is of the form observed by Megaw over the North Sea.

21. REFLECTION OF PULSES FROM ATMOSPHERIC DIELECTRIC VARIATIONS

Donald M. Swingle

(Evans Signal Laboratory)

For normal-incidence reflections of electromagnetic waves in the atmosphere it is shown that a simple integral approach yields a reasonable formulation of the r-f echo. It is found that a plane-wave reflected by a discontinuity in dielectric-constant gradient produces an echo proportional to its time-integral. This formulation is restricted to media similar to the atmosphere having a total change of dielectric constant much less than its minimum value.

22. A METEOROLOGICAL STUDY OF "ANGELS" AT 1.25 CM

Vernon G. Plank

(Air Force Cambridge Research Center)

"Angels" echoes as observed on a vertical pointing 1.25 cm radar are analyzed statistically to determine the meteorological factors correlatible with their existence, their concentration and the altitudes to which they extend. It is found that typical "angels" are most likely on days having pronounced wind shear throughout a convective lower layer; however, either wind shear or adequate solar radiation appears alone sufficient. Maximum "angel" altitudes are observed to coincide well with the top of the mixing zone.

Certain atypical situations are cited and insect activity as a possible "angel" producer is discussed in the light of known insect habits.

23. DIFFUSION OF A SMOKE PUFF AS A TURBULENCE MEASURE IN THE ATMOSPHERE

Eiichi Inoue

(National Institute of Agricultural Sciences, Tokyo, Japan)

Assuming that the modern similarity theory of turbulence can be applied to the atmosphere, the turbulent diffusion of a smoke puff floating in the atmosphere is dealt with theoretically in this paper. The visible outline of a floating smoke puff is considered particularly. The mass rate ϵ of turbulent energy dissipation in the atmosphere is shown to be the most important factor which causes the variation in the scale of the visible outline with time, and some possibilities of estimating ϵ at a great height in the atmosphere by means of the observations of diffusing smoke puffs are presented. Discrepancies between the present results and those obtained from O. G. Sutton's semi-empirical theory are also made clear.

24. STRUCTURE OF TWO AND THREE-DIMENSIONALLY ISOTROPIC TURBULENCE IN THE ATMOSPHERE

Y. Ogura and K. Yakoda

(Tokyo University, Tokyo, Japan)

The purpose of the present paper is to make clear the several statistical properties of two- and three-dimensionally isotropic turbulence in the atmosphere. Especially the interrelations between the many statistical quantities observed in the atmosphere, e.g. gustiness of wind, scale of turbulence, correlation coefficients, etc., and the observing procedure or the sensibility of observing instruments are discussed. Making use of the statistical law thus obtained, poly-dimensional turbulent diffusion of the matter emitted from a point source is studied.

25. CORRELATION BETWEEN SFERICS AND TORNADO INCIDENCE

H. L. Jones

(Oklahoma A and M College)

The Tornado Laboratory at Oklahoma A. and M. College, Stillwater, Oklahoma, was operated continuously during the 1953 tornado season. This season began early in February and extended to the middle of July. A number of unique instruments were developed for the 1953 tornado season. Results obtained by the use of these instruments presented a number of interesting relationships between sferic incidence and the intensity of severe storms.

26. CORRELATION OF THUNDERSTORM ATMOSPHERICS MEASUREMENTS

Joseph Weil and M. M. Newman

(University of Florida; Lightning and Transients Research Institute)

This paper presents general instrumentation and operational planning of the Sferics triangulation program including correlated measurements at the Lightning and Transients Research Institute at Minneapolis, Minnesota, the University of Florida, and the New Mexico Institute of Mining and Technology.

An important point in the correlated measurements is to have synchronized timing at the three stations. At each laboratory a basic frequency standard is used for "free-running" initiation of the oscillograph sweeps in between intervals of timing coordination as may be possible from WWV or from artificial lightning discharges triggered at the L & T laboratory. Timing procedures are presente in order that other laboratories may correlate measurements, so that distinct atmospherics including "Whistlers" can be identified at many different locations.

27. RECORDING AND CLASSIFICATION OF THUNDERSTORM ATMOSPHERICS BY COUNTER TECHNIQUES

M. M. Newman, J. R. Stahmann and J. R. Anderson
(Lightning and Transients Research Institute)

A direct counter approach to classifying sferic pulse components has been developed which indicates component pulses in terms of numbers per second exceeding a given value of rate of rise, crest and also per cent of time above or below a given interference level. The output as indicated on the meter is also plotted versus level on a specially built up recorder.

The distribution in time is also given by an associated oscillograph channel. The advantage of the counter technique is that it gives a direct classification of waveforms in terms of polarity, typical duration, rates of rise and crest values, typical time spacings and average duration of static burst.

A simplified instrument for counting nearby lightning strokes in terms of the magnitudes of the electric and magnetic field components is also discussed.

28. ATMOSPHERIC WAVEFORMS AND THE LOCATION OF THUNDERSTORMS

E. T. Pierce and T. W. Wormell
(Cavendish Laboratory, England)

Regular night-time atmospherics consist either of a series of peaked pulses fitting the concept of successive ionospheric reflections, or of a smooth quasi-sinusoidal oscillation which does not obey the simple reflection picture. Records taken at Cambridge, England, show that regions producing quasi-sinusoidal waveforms do not generate peaked atmospherics and vice versa, and that all quasi-sinusoidal waveforms originate from the S.W. at distances exceeding 1600 km. Observations near the eastern coast or center of the U.S.A. would assist in establishing the cause of these curious geographical effects.

The general problem of thunderstorm location from the characteristics of atmospherics is discussed.

29. THE LIGHTNING DISCHARGE PROPAGATION MECHANISM EFFECT ON ATMOSPHERICS WAVEFORMS INCLUDING "WHISTLERS"

M. M. Newman
(Lightning and Transients Research Institute)

The discharge channel characteristics are among the most important factors in determining the nature of atmospherics. The channel resistivities, surge impedances, and propagation velocities involve non-linear variations which lead to interesting stepped currents. Equivalent electrical circuits were developed for the channel and calculations were made assuming the channel resistance to vary inversely with the charge that passed through. Calculated current variations were in surprisingly close agreement with magnitudes and separations of successive current peaks shown by Schonland's photographic records. Also it was worked out mathematically that spacings of component pulses could vary in such a way as to produce a "Whistler" type noise, and thus perhaps accounting for some of the "Whistler" type atmospherics.

30. LIGHTNING IDENTIFICATION ON THE PPI

Donald M. Swingle
(Evans Signal Laboratory)

What are believed to be the first PPI photographs including sferics information are presented. This technique permits the detailed location of regions of electrical activity among the radar storm echoes. Approaches to improved presentation techniques are discussed. The advantages of this technique to the operating meteorologist and flight control personnel are stressed.

31. INFORMATION OBTAINABLE FROM QUANTITATIVE MEASUREMENTS OF RADAR ECHOES FROM PRECIPITATION

P. M. Austin
(M.I.T.)

The general characteristics of radar echoes from precipitation are discussed. The relation of the intensity of the radar signal to the number, size, shape and composition of the precipitation particles is pointed out, as well as the dependence of the time variations of the signal upon the motions of the scattering particles.

Consideration is also given to meteorological interpretation and deductions such as: measurements of rainfall intensity, observations concerning the growth and melting of snowflakes and indications of wind shear and turbulence.

32. CLOUD PHYSICS—A REVIEW

S. E. Reynolds
(New Mexico School of Mining and Technology)

Research in cloud physics in recent years has been devoted primarily to the study of the physical processes leading to cloud precipitation. These studies, of course, have contributed also to our understanding of stable clouds. Therefore it is convenient, and seems not too restrictive, for this paper to be concerned primarily with the discussion of precipitation processes.

Observations leading to the recognition that the necessity for the Bergeron ice crystal mechanism is lacking for certain types of precipitation over much of the earth's surface are described. The development of precipitation particles without the involvement of ice is well confirmed in tropical regions as well as at the middle latitudes in both coastal and inland areas. The role that condensation nuclei play in determining the character of a cloud and thus its susceptibility to various precipitation processes is discussed. Rare, large hygroscopic nuclei appear to be important in the development of coastal precipitation. The extensive studies of the nature, concentration and behavior of natural and artificial ice-forming nuclei are briefly reviewed and the growth processes of ice crystals are discussed. The development of precipitation by droplet coagulation is discussed and compared to the ice crystal mechanism. Much of the material is related to the possibilities for controlling precipitation.

Thunderstorm electrical properties determined principally by the precipitation processes in convective clouds are discussed briefly.

Very excellent lapse time films illustrating physical processes in clouds have been prepared by V. J. Schafer and others. Some of these films will be shown.

33. FORMATION OF SNOW CRYSTALS

Ukichiro Nakaya
(Snow, Ice and Permafrost Research Institute)

Twenty years of investigations on natural and artificial snow crystals carried out at Hokkaido University are summarized. The mode of growth of snow crystals is shown by a lapse time movie through a microscope, by producing various shapes of crystals in a cold chamber. The relation between the shape of crystal and the external conditions is studied by the use of artificial snow, and it was found that the shape is determined by the ambient temperature and the degree of supersaturation, the former being the controlling factor. This result is explained by assuming that snow crystals are developed in the atmosphere saturated with respect to water.

Electron-microscopic studies on the nucleus of snow were also carried out. One solid nucleus was almost always observed at the central portion of a snow crystal. In the other part of the crystal numerous smaller nuclei were observed whose dimensions were of the order of those of condensation nuclei. From the data of the electron-microscopic studies and those of the condition of formation of snow crystals, it is suggested that minute water droplets of 1_μ of so play an important role in the process of snow crystal growth.

34. APPLICATION OF RADAR TO CLOUD PHYSICS RESEARCH IN HAWAII

David S. Johnson
(Pineapple Research Institute, Hawaii)

Two ten centimeter wavelength, mobile radar units are being used in a study of natural rain formation and cloud modification experiments in Hawaii. Lapse time movies of the radar screen indicate the general character of rainfall from warm clouds in Hawaii. Simultaneous radar and raindrop size distribution observations indicate some limitations in the use of ten centimeter radar in Hawaiian cloud studies and reemphasize differences between the character of rainfall in this region compared to that described for other areas. Radar movies made during a cloud seeding experiment are presented.

35. MEASUREMENTS OF RADAR SIGNAL INTENSITY AT DIFFERENT LEVELS IN STEADY SNOW

P. M. Austin and R. Wexler
(M.I.T.; Harvard University)

Measurements of the radar signal intensity from different levels in precipitation have been made since January 1953 with a pulse integrator attached to a CPS-9 radar. In steady precipitation a fixed azimuth and range, generally about 10 miles, is chosen, while the angle of elevation of the antenna is varied in steps of one or two degrees.

Results indicate that in steady snow the cloud liquid water content is very small and that the ice crystals grow at a supersaturation intermediate between ice and water. Near the 0°C level coalescence of ice crystals frequently takes place. Nonsteady conditions frequently occur which are caused by showers or by a more rapid growth of ice crystals in a layer of relatively high liquid water content.

36. RADAR EVIDENCE OF A GENERATING LEVEL FOR SNOW

K. L. S. Gunn
(McGill University, Canada)

A study of vertical section radar records and upper air data for 22 days of snow at Montreal in the winter of 1951–52 reveals that well defined snow trails occur on days when the air aloft is stable. In these situations, snow develops in discrete generating elements, of considerable lifetime, which exist in a layer of middle cloud. The top of this cloud is less than 2000 ft. above a frontal surface on these stable days. On days when the warm air is unstable, the trail patterns are not so well defined, and the cloud top is farther from the frontal surface.

37. LOWERING OF THE BRIGHT BAND DURING HEAVY RAIN

R. Wexler and J. Honig
(Harvard University; M.I.T.)

Cooling of the layer of air near the ground by falling melting snow is shown to be responsible for the transformation of heavy rain into a snow storm over portions of southern New England on April 13, 1953. From the rain intensity and the rate of cooling of the surface temperature at several stations, the depth of the layer of air is computed.

38. QUANTITATIVE 1.25 CM OBSERVATIONS OF RAIN AND FOG

D. Atlas, R. J. Donaldson, W. H. Paulsen, R. C. Cunningham and A. C. Chmela
(Air Force Cambridge Research Center)

1.25 cm radar-weather observations were conducted at Round Hill, Massachusetts. A brief preliminary report is made of the four phases of these studies: fog, rain, angels, and radar calibration.

The fog observations included measurements of radar reflectivity, optical transmission, drop size distribution, and liquid water content. Rain intensities and $Z = \Sigma N d^6$ (corrected for Mie scattering) were computed from drop size data. Echoes from light rain agree with theory; those from heavier rain are a few db low. Echoes from fog and optical transmission through it will be discussed. Calibration of the radar system was accomplished by suspending conducting spheres of various sizes in the radar beam. Intricacies of the method and unexpected results will be discussed.

39. MOISTURE CONTENT, DISTRIBUTION AND RADAR REFLECTIVITY IN THUNDERSTORMS

R. K. Moore, H. A. Oltman, A. T. Marrs, and D. M. Gragg
(Sandia Corporation)

Measurements were made aloft of the distribution of drop sizes in thunderstorms, using a shadowgraph technique. Moisture content as high as 28 grams per cu m was deduced from the drop size data; this was nearly always in excess of 5 grams per cu m. Values of radar cross-section index from 1100 to 7800 mm^6 per cu m were also deduced. Although the moisture content is an order of magnitude higher than that which was reported by ground observers, the radar cross-section index is lower. A graphical technique for determining the distribution function in a form suitable for extrapolation is also described in this paper.

40. DEVELOPMENT DURING FALL OF RAINDROP SIZE DISTRIBUTIONS

J. S. Marshall
(McGill University, Canada)

It has been assumed that the size distributions of raindrops as they originate in cumulonimbus or at the melting level are like those observed at the ground, but more consistent. Their subsequent development by rain-drop-coalescence, cloud accretion and evaporation has been calculated: it modifies the distributions and the resultant Z/R relation only moderately, and well within the limits of accuracy of most observations. In the case of showers, wind shear can separate out the drops according to size. The resultant error in measurement of rainfall by radar should usually diminish greatly when averaged either over a few minutes or a few miles.

41. SOME OBSERVATIONS FROM PHOTOGRAPHS OF FALLING RAINDROPS

Douglas M. A. Jones and Lawrence A. Dean
(Illinois State Water Survey)

Data are presented for the lengths of the major and minor axes and the orientation of the major axis with respect to the horizontal. Photographs from the raindrop camera are included as illustrations. This project is being sponsored by U. S. Signal Corps Engineering Laboratories under contract No. DA36-029-sc-42446.

42. THE DEFORMATION OF LARGE RAINDROPS

James E. McDonald
(The University of Chicago)

The physical processes capable of producing the characteristic deformation of raindrops of diameter greater than about 3-mm are examined quantitatively and it is shown that surface tension forces, internal hydrostatic pressures, and external aerodynamic pressures are the controlling factors. In thunderstorm regions of very high electric charge density, surface charges on the drops can also influence drop shape, but only for charge magnitude approaching the limit set by the dielectric strength of air. Internal circulations assumed by Lenard to control drop deformation are shown to be of negligible importance, though present.

The aerodynamic pressure distribution around large drops is computed by a method based on analyses of high-speed drop photographs due to Magono. It is shown that the deduced pressure profiles constitute strong evidence confirming the validity of the drop-shape hypothesis employed, in that they imply the existence of separation of the boundary layer capable of explaining the reasonance phenomenon discovered by R. Gunn, yield an integrated vertical force in good agreement with measured drop weight, and yield an integrated horizontal force in good agreement with the total surface tension force acting around a meridional curve.

The relation of deformation to breakup is examined and the associated implications for radar cloud-physical studies are discussed.

43. OPTICAL TRANSMISSION THROUGH RAINFALL

David Atlas
(Air Force Cambridge Research Center)

The optical extinction coefficient σ due to rain is found to be related to the rain intensity R by $\sigma \cong 0.25 R^{0.65}$(kg^{-1}) in Bergeron type rainfall and $\sigma \cong 1.2 R^{0.33}$ in warm orographic rainfall. If the threshold of contrast is taken as 0.055, and rain is the only significant obstruction to visibility, the daytime visual range may be estimated from $V \cong 11.6 R^{-0.65}$(km) in Bergeron type rain and $V \cong 2.4 R^{-0.33}$ in warm orographic rainfall. Both the coefficient and the exponent in the σ-R relationship appear to be fairly sensitive to variations in the nature of the drop-size distribution. Provided that other scattering media such as haze and dust can be accounted for, optical transmission measurements in rainfall should be helpful in characterizing its spectrum and possibly its origin. The use of optical transmission in radar rainfall studies, and the variation of the $Z-R$ relation with drop-size distribution will also be discussed.

44. MEASUREMENT AND DETECTION OF RAINFALL BY RADAR AT ATTENUATING WAVELENGTHS

Walter Hitschfeld
(McGill University, Canada)

A new explicit equation is derived for the rate of rainfall in terms of the received power and range, with full allowance for attenuation. Error analysis shows that if attenuation is present, the radar-measured rainfall depends so sensitively on the calibration of the set, that attenuating wavelengths are not generally suitable for rain *measurements*. Only if the measurements are made at points where the attenuation is smaller than at the rain gauge used in the calibration, can a satisfactory degree of precision be attained.

A study of the performance of 3 and 5.6 cm low-power radars of otherwise identical characteristics show similarly that the shorter wavelength is probably not even suitable in the practical problem of *detection* of rain through intervening rain.

45. VARIANCE OF AREAL-MEAN THUNDERSTORM RAINFALL ESTIMATES

J. C. Neill
(Illinois State Water Survey)

In quantitative radar-rainfall studies, a method is needed for judging the accuracy of areal-mean rainfall values which are computed from radar data. This study was designed to provide a standard for rating the radar-rainfall values in terms of equivalent raingage densities. A systematic sampling scheme was used in selecting raingage total storm rainfall amounts from 48 gages which were distributed over a 96-square-mile area. Areal-mean rainfall estimates were obtained from samples of size 2, 3, 4, 6, 8, 12, 16, and 24 gages for 16 thunderstorms during July, August, and September 1952. The standard errors of these estimates about the 48-gage mean rainfall were computed. A regression equation was determined which expresses the relationship between the expected standard error, the mean rainfall from 48 gages, and the number of gages included in each estimate. The study provides an estimate of the standard error to be expected in the measurement of areal-mean thunderstorm rainfall with systematic samples of different numbers of gages. The magnitude of these standard errors is used as a basis for rating the difference between radar areal-mean rainfall and the areal-mean from a raingage network. This study was accomplished through the sponsorship of the Signal Corps Engineering Laboratories on Contract No. DA-36-039-SC-42446.

46. RELIABILITY OF RADAR AREAL RAINFALL MEASUREMENTS

F. A. Huff and J. C. Neill
(Illinois State Water Survey)

A 3-cm radar set, employing an automatic gain reduction device, was used to collect storm rainfall data over a network of 50 rain gages in a 96-square-mile area in Central Illinois during 1951–53. The radar-indicated areal-mean rainfall was calculated from one-minute isoecho contour maps drawn from 35-mm photographs of the PPI scope. Rainfall intensity values for the isoecho contours were obtained by substitution in the theoretical radar-rainfall formula of Marshall, Langille, and Palmer.

The areal-mean rainfall computed from the network of 50 rain gages was used as the best estimate of the true surface rainfall. Deviations of the radar-indicated rainfall from the raingage-computed rainfall were then calculated. These deviations were compared with the standard deviations of mean rainfall estimates from various gage densities, in order to express the reliability of the radar-indicated rainfall amounts in terms of equivalent raingage density for 96 square-miles.

This study has been jointly sponsored between the Illinois State Water Survey and U. S. Army Signal Corps Engineering Laboratories under contract No. DA-36-039 SC 42446.

47. OPERATIONAL UTILIZATION OF RADAR STORM OBSERVATIONS

Myron Ligda
(M.I.T.)

While use of radar storm reports in aircraft operations has received much attention, the subject of rarep use in surface military operations has been largely neglected.

Some possible uses of rareps in combat operations are suggested. Upon examination, it is found that there are many military activities which would be influenced by short range, highly accurate precipitation forecasts which could be provided by radar observation. Some possible field networks are suggested together with codes which could be used.

48. THE RADAR STORM DETECTION PROGRAM OF THE WEATHER BUREAU

Vaughn D. Rockney
(U. S. Weather Bureau)

The first installation by the Weather Bureau of radar storm detection equipment was made at Wichita, Kansas in April 1947. Since that time, a network of radar storm detection stations has been established by the Weather Bureau, in some cases with the aid of co-operators, in the midwest and along the Gulf and Atlantic Coasts. The extent of the network and plans for future expansion will be shown and a wide variety of operational uses will be discussed.

49. THE PRESENT STATUS OF THE AN/CPS-9* PROGRAM

E. L. Williams and J. R. Blakely
(Raytheon Manufacturing Co.)

The AN/CPS-9 is an X band radar system specifically designed for the detection and location of moisture-laden storms. Raytheon Mfg. Co. is currently building 56 systems for various branches of the Armed Services, two of which are complete and have been turned over to the Signal Corps. Completion of the remaining 54 systems is scheduled for August 1954 with the first production system to be delivered late in 1953.

* Work being performed under Signal Corps Contract DA-36-039-sc-5622.

50. A REVIEW OF RESULTS OF OPERATIONAL TEST OF RADAR CLOUD INDICATING EQUIPMENT

D. M. Swingle
(Evans Signal Laboratory)

The results of a full year of operation of radar cloud indication equipment in which the radar was compared to an experienced weather observer are reviewed briefly. The equipment is found to add large numbers of higher cloud observations.

51. RADAR ECHOES IN TORNADO SITUATIONS

J. C. Freeman, Jr.
(Texas A and M College)

Radar echoes from the storms associated with two tornado situations in Texas in the spring of 1953, show that three tornadoes were associated with very large and "hard" cloud echoes. In at least one case a "tail" such as the one shown by Stout was observed. In all of these cases the large echoes were in a region of observable convergence in the surface winds. A tentative theory of the formation of such a region of convergence and tornado development in it is shown.

52. SUMMARY AND RESULTS OF FIRST TEXAS TORNADO WARNING CONFERENCE

Archie M. Kahan
(Texas A and M College)

The Texas Tornado Warning Conference held at Texas A. & M. College on June 24, 1953 had two aims: (1) the inventorying of existing facilities for the establishment of a more effective Tornado Warning System and (2) establishment of a co-ordinating committee. Organization of existing radar sets into an effective operating network developed as an immediate goal. The Texas Tornado Warning Committee was established to exploit existing facilities in the saving of life and property and to encourage the installation of additional radar sets to fill in gaps in the network or replace less suitable equipment.

53. THE PHYSICAL PROCESSES IN THE DEVELOPMENT OF TORNADOES AND CONSEQUENCES WHICH INFLUENCE THEIR DISSIPATION

Fritz O. Rossmann
(Air Force Missile Test Center)

The purpose of this paper is to present a new theory concerning the physical process in the development of tornadoes simultaneously with a proposal of their destruction.

Criteria determining both the origin of tornadoes and their dynamic forces are developed through physical insight and computation of their wind velocities. The physical theory is founded on numerous observations of specific cases in the United States where, in recent years, an unusually large number of tornadoes occurred. It will be demonstrated that there is no updraft in the funnel of a tornado, as is generally assumed, but that there is a strong downdraft caused by moist-labile conditions and stabilized by the revolving motion of the air mass in the tornado funnel. This seems to present the only way to evolve a theory of tornadoes without finding any contradictions in conditions and facts characterizing the shape and destructive powers of tornadoes anywhere in the world. It is the critical stabilized condition which, if abruptly altered, causes the tornado to dissipate.

Following this point of view, it becomes evident that a means might be developed to attack and destroy tornadoes at their weakest and most vulnerable spot. This matter will be presented by Colonel Rollins H. Mayer in his paper on "A Proposal for Research on the Possibility of the Destruction of Tornadoes with Missiles Guided by Weather Radar."

54. A PROPOSAL FOR RESEARCH ON THE POSSIBILITY OF THE DESTRUCTION OF TORNADOES WITH MISSILES GUIDED BY WEATHER RADAR

Rollins H. Mayer
(Air Force Missile Test Center)

The primary purpose of this paper is to stimulate an interest in the possibility of destroying tornadoes with weather radar guided missiles simultaneously initiating a movement to gather the necessary support for the practical achievement of a national tornado-damage-prevention net.

Statistics show that within the past twenty years approximately one billion dollars property damage, more than eight thousand deaths, and over one hundred thousand persons have been injured as a result of tornadoes. If only a five per cent reduction in tornado damage could be realized, a great advancement in science will have been made and the welfare of mankind promoted.

The idea of destroying tornadoes with missiles guided by weather radar is currently being jointly investigated by Dr. Fritz Otto Rossmann, former German University of Munich professor, now Upper Air Physicist, Air Force Missile Test Center, and Colonel Rollins Harry Mayer (USAFR) Electronic Scientist, Air Force Missile Test Center. The feasibility of launching a detonation into a tornado by means of a guided missile for the purpose of its destruction is discussed and an analysis of the associated problems of tornado forecasting, detection, warning, tracking, interception, and safety is made. In addition, a proposal for a national tornado-damage-prevention-net is submitted.

It is jointly concurred by Dr. Rossmann and Colonel Mayer that a practicable tornado destructor might be realized in the near future.

55. THE USE OF RADAR STORM OBSERVATIONS FOR WEATHER FORECASTING

Myron Ligda
(M.I.T.)

In late years little direct progress has been made on utilization of radar storm observations for weather forecasting purposes. However, excellent progress toward organization of the AN/CPS-9 radar network has greatly stimulated interest in this particular field of radar meteorology. Many questions have arisen concerning the utility of radar storm observations for the 6–24 hour forecast interval.

An attempt is made to answer some of these questions. The observations which can be made with radar which are of possible use to the forecaster are considered. The problems of network operation are discussed and some suggestions for possible solutions of some of these problems are offered.

56. RADAR IN SINGLE STATION ANALYSIS

Glenn E. Stout
(Illinois State Water Survey)

Data are presented to show the utility of radar in providing detailed information in the analysis of precipitation patterns over areas of 30,000 square miles. Other possible applications of radar weather data is indicated. The interpretation of scope patterns requires an understanding of meteorology, especially precipitation processes.

57. THE FREQUENCY OF RADAR STORM ECHOES AS A FUNCTION OF POSITION

William J. Richards
(Evans Signal Laboratory)

An objective analysis of the relative frequency of occurrence of radar storm echoes in each of twelve equal-area regions distributed about the Signal Corps Engineering Laboratories' AN/CPS-9 (Belmar, N. J.) is presented. Data for 1948 to 1953 are included. The diurnal, ocean-land contrast, prevailing flow patterns, season and synoptic conditions are discussed. This report essentially constitutes a basic radar-climatology for the Belmar N. J. area.

58. THE VARIABILITY OF THE MOTION OF RADAR PRECIPITATION LINES

Donald M. Swingle and
William J. Richards
(Evans Signal Laboratory)

The radar storm detection records made by the Signal Corps Engineering Laboratories (Belmar, N. J.) and the Massachusetts Institute of Technology (Cambridge) from 1946 to 1953 have been examined to determine the variability of half-hour speed of movement of precipitation lines as seen on the P.P.I. The implications of the observed variability for forecasting from the P.P.I. are discussed. An effort was made to place only a small amount of time and sophistication on the interpretation of photographs in order to simulate reasonably adverse operating conditions.

59. MESOMETEOROLOGICAL ANALYSIS OF COLD FRONT PASSAGE USING RADAR WEATHER DATA

Donald M. Swingle and
Louis Rosenberg
(Evans Signal Laboratory)

All available weather data for an area of radius 400 miles surrounding the Evans Signal Laboratory, Belmar, N. J., are analyzed in conjunction with storm detection radar (AN/CPS-9) data obtained by the Signal Corps Engineering Laboratories on 19 July 1951. Detailed mesometeorological analysis is made of the radar data, the occurrence and motion of squall lines, discontinuity zones and pressure patterns. A number of squall lines suggestive of the Tepper pressure jump lines are located and followed on hourly maps of the area. It is shown that a single radar can considerably improve short term (2–6 hours) forecasts for the local region, while the desirability of more adequate storm detection data transmission is shown.

60. RADAR OBSERVATIONS OF THE SEA-BREEZE FRONT

D. Atlas, W. H. Paulsen, R. J. Donaldson
A. C. Chmela and V. G. Plank
(Air Force Cambridge Research Center)

The sea-breeze front has been detected with 1.25 cm radar on several occasions at Round Hill, Massachusetts. Simultaneous with the radar observations, measurements of the sea-breeze discontinuity were taken with a microwave refractometer and numerous meteorological instruments.

The echoes are similar to angels, arising from sharp discontinuities in refractive index between sea-breeze air and land-breeze air. On the horizontal radar beam, the sea-breeze frontal echoes are incoherent and have the appearance of heavy streamers of snow. Upon passage of the front, the vertical beam detects the inversion, echoes from which are closely packed and coherent, similar to ordinary angels. This difference provides qualitative information on the scale of the individual reflecting elements relative to the pulse length.

61. THE RADAR AS A TURBULENCE SENSING PROBE

Aaron Fleisher
(M.I.T.)

A general relation between the statistics of the wind and the statistics of the weather signal is stated. Solutions for the first two probability densities of the wind are exhibited along with some examples of measured distributions of gustiness.

Computer Publications

A limited number of Joint Computer Conference Proceedings of the Transactions of the IRE Professional Group on Electronic Computers are available from the IRE at the prices listed below.

The three volumes of Joint Computer Conference Proceedings represent one of the most comprehensive sources of information on electronic computers, covering the entire field—digital and analog, design, construction, and application.

The June, 1953, issue of the PGEC Transactions, the only issue for which extra copies are still on hand, contains original papers on regenerative loops in analog computers, electrical delay lines, and the design of flip-flops.

Please send your order to: L. G. Cumming, Technical Secretary, The Institute of Radio Engineers, 1 East 79th St., New York 21, N Y.

Publication	Content	Price
Joint AIEE-IRE Computer Conference Proceedings, (Published February 1952)	REVIEW OF ELECTRONIC DIGITAL COMPUTERS, Papers and Discussions presented at the Joint AIEE-IRE Computer Conference, Philadelphia, Pa., Dec. 10–12, 1951 (114 pages)	$3.50
Joint AIEE-IRE-ACM Computer Conference Proceedings (Published March 1953)	REVIEW OF INPUT AND OUTPUT EQUIPMENT USED IN COMPUTING SYSTEMS, Papers and Discussions presented at the Joint AIEE-IRE-ACM Computer Conference, New York, N. Y., Dec. 10–12, 1952 (142 pages)	$4.00
Joint AIEE-IRE-ACM Computer Conference Proceedings (Published June 1953)	PROCEEDINGS OF WESTERN COMPUTER CONFERENCE, Los Angeles, Calif., Feb. 4–6, 1953, 22 papers and discussions on computers and their application (231 pages)	$3.50
Transactions of the PGEC, June, 1953	(27 pages)	$1.35 for IRE members $2.70 non-members

Institute Committees—1953

Executive

J. W. McRae, *Chairman*
W. R. G. Baker, *Vice Chairman*
Haraden Pratt, *Secretary*
S. L. Bailey
A. N. Goldsmith
W. R. Hewlett
D. B. Sinclair

Constitution and Laws

R. A. Heising, *Chairman*
I. S. Coggeshall
J. B. Coleman
A. W. Graf
R. F. Guy
H. R. Zeamans

Professional Groups

W. R. G. Baker, *Chairman*
L. C. Van Atta, *Vice Chairman*
B. B. Bauer
L. M. Clement
W. L. Everitt
A. W. Graf
R. A. Heising
J. H. Howard
D. D. Israel
G. F. Metcalf
W. M. Rust, Jr.
P. C. Sandretto
Harner Selvidge
Ernst Weber
(Professional Group Chairmen Ex-Officio)

Finance

W. R. G. Baker, *Chairman*
S. L. Bailey
W. R. Hewlett
A. V. Loughren
J. W. McRae, Ex-officio
D. B. Sinclair

Awards

Ernst Weber, *Chairman*
R. M. Bowie
J. F. Byrne
L. T. DeVore
J. F. Morrison
D. E. Foster
A. B. Oxley
J. D. Reid
W. M. Rust, Jr.
J. E. Shepherd
A. F. Van Dyck
H. W. Wells

Admissions

H. P. Corwith, *Chairman*
E. W. Bemis
H. S. Bennett
*T. M. Bloomer
*H. A. Brown
C. M. Burrill
*E. T. Dickey
*V. J. Duke
E. E. Ecklund
*Leonard Goldstone
*R. E. Gray
C. A. Hachemeister
H. R. Holloway
M. B. Kline
F. S. Mabry
*F. L. Marx
*H. G. Miller
D. M. Pasek
D. C. Pinkerton
G. B. Riley
*N. B. Ritchey
H. R. Terhune
*J. D. Winer

* Alternates.

Membership

W. C. White, *Chairman*
Kipling Adams
F. W. Albertson
A. R. Beach
T. H. Clark
A. W. Keen
A. B. Oxley
D. B. Sinclair
G. R. Town
L. C. Van Atta
(Chairmen of Section Membership Committees Ex-Officio)
(Regional Directors Ex-Officio)

Public Relations

Lewis Winner, *Chairman*
E. L. Bradgon
W. C. Copp
H. E. Fry
E. K. Gannett
R. F. Guy
T. R. Kennedy, Jr.
H. S. Renne
Bruce Robertson
E. C. Thompson
(Chairmen of Section Publicity Committees Ex-Officio)

Sections

Irving Wolff, *Chairman*
(Chairmen of Sections Ex-Officio)

Education

J. D. Ryder, *Chairman*
R. G. Anthes
G. R. Arthur
V. A. Babits
C. G. Brennecke
W. L. Cassell
C. C. Chambers
D. H. Ewing
R. M. Fano
C. L. Foster
A. W. Graf
A. E. Harrison
H. E. Hartig
R. W. Hickman
G. B. Hoadley
G. L. Hollander
A. H. Howell
F. S. Howes
Glenn Koehler
A. W. Melloh
H. A. Moench
P. H. Nelson
J. M. Pettit
Albert Preisman
L. R. Quarles
L. R. Ragazzini
H. J. Reich
V. C. Rideout
F. R. Stansel
W. N. Tuttle
D. L. Waidelich
L. E. Williams
D. G. Wilson
A. H. Wing, Jr.

Policy Advisory

J. D. Ryder, *Chairman*
K. C. Black
W. H. Doherty
Ferdinand Hamburger, Jr.
T. A. Nunter
F. B. Llewellyn
A. V. Loughren
A. W. Straiton

Nominations

W. H. Doherty, *Chairman*
I. S. Coggeshall
A. W. Graf
A. B. Oxley
J. R. Ragazzini
D. B. Sinclair
A. W. Straiton
F. E. Terman

Tellers

Vincent Learned, *Chairman*
W. F. Bailey
J. F. Craib
J. H. Mulligan, Jr.
A. K. Wing, Jr.

BOARD OF EDITORS

A. N. Goldsmith, *Chairman*

F. W. Albertson
W. S. Bachman
G. M. K. Baker
W. L. Barrow
R. R. Batcher
J. H. Battison
B. B. Bauer
H. S. Black
Ralph Bown
R. S. Burnap
O. H. Caldwell
C. W. Carnahan
C. C. Chambers
L. M. Clement
J. D. Cobine
J. W. Coltman
M. G. Crosby
R. C. Curtis
R. L. Dietzold
R. B. Dome
W. G. Dow
W. L. Everitt
W. G. H. Finch
D. G. Fink
I. A. Getting
L. J. Giacoletto
A. W. Graf
F. W. Grover
E. A. Guillemin
A. V. Haeff
D. B. Harris
L. B. Headrick
E. W. Herold
J. K. Hilliard
C. J. Hirsch
R. G. E. Hutter
J. K. Johnson
L. F. Jones
H. S. Knowles
J. B. H. Kuper
S. C. Lawrence
D. G. Little
F. B. Llewellyn
E. D. McArthur
Knox McIlwain
Nathan Marchand
G. F. Metcalf
E. L. Nelson
D. O. North
K. A. Norton
H. F. Olson
G. D. O'Neill
R. M. Page
H. O. Peterson
G. W. Pickard
Haraden Pratt
C. A. Priest
J. R. Ragazzini
Simon Ramo
H. J. Reich
F. X. Rettenmeyer
H. H. Scott
Stuart Seeley
V. W. Sherman
L. C. Smeby
C. E. Smith
Newbern Smith
J. A. Stratton
G. C. Sziklai
W. C. Tinus
K. S. Van Dyke
E. K. Van Tassel
Ernst Weber
H. A. Wheeler
J. R. Whinnery
W. C. White
L. E. Whittemore
J. B. Wiesner
Irving Wolff
H. A. Zahl
V. K. Zworykin

ADMINISTRATIVE COMMITTEE OF THE BOARD OF EDITORS

A. N. Goldsmith, *Chairman*

G. M. K. Baker
H. S. Black
R. M. Bowie
R. S. Burnap
R. L. Dietzold
L. J. Giacoletto
F. B. Llewellyn
Knox McIlwain
K. A. Norton
F. X. Rettenmeyer
Newbern Smith
G. C. Sziklai
H. A. Wheeler
L. E. Whittemore
H. A. Zahl

PAPERS REVIEW

G. F. Metcalf, *Chairman*

M. A. Acheson
H. A. Affel
W. J. Albersheim
D. B. Anderson
V. A. Babits
Ross Bateman
P. H. Betts
F. J. Bingley
D. S. Bond
B. B. Brown
D. R. Brown
Kenneth Bullington
R. P. Burr
J. K. Clapp
S. B. Cohn
H. V. Cottony
F. W. Cunningham
L. T. DeVore
A. R. D'Heedene
M. J. Di Toro
H. D. Doolittle
O. S. Duffendack
W. A. Edson
Joseph Feinstein
E. H. Felix
L. M. Field
J. W. Forrester
V. H. Fraenckel
R. L. Freeman
E. G. Fubini
H. P. Gates, Jr.
W. M. Goodall
A. J. Grossman
O. B. Hanson
A. E. Harrison
Walter Hausz
T. J. Henry
W. R. Hewlett
Gunnar Hok
C. N. Hoyler
P. K. Hudson
W. H. Huggins
Henry Jasik
E. C. Jordan
A. G. Kandoian
Martin Katzin
R. W. P. King
C. R. Knight
W. E. Kock
J. J. Lamb
M. T. Lebenbaum
Meyer Leifer
C. V. Litton
A. B. Macnee
W. P. Mason
R. E. Mathes
J. O. Mesa
H. R. Mimno
J. A. Morton
Garrard Mountjoy
A. F. Murray
J. R. Nelson
C. H. Page
R. C. Palmer
H. W. Parker
W. H. Pickering
Albert Preisman
C. F. Quate
H. E. Roys
John Ruze
W. E. Ryan
J. D. Ryder
A. L. Samuel
H. A. Samulon
R. K. F. Scal
L. S. Schwartz
Samuel Seely
Harner Selvidge
R. F. Shea
R. T. Silberman
Richard Silberstein
David Sillman
George Sinclair
J. E. Smith
W. M. Smith
A. E. Smoll
R. L. Snyder, Jr.
Harold Staras
J. R. Steen
G. R. Sugar
C. S. Szegho
H. P. Thomas
C. E. Torsch
Bertram Trevor
L. C. Van Atta
S. N. Van Voorhis
J. M. Watts
R. C. Webb
J. R. Weiner
K. R. Wendt
M. S. Wheeler
O. C. Woodyard
Victor Young
H. R. Zeamans

Special Committees

ARMED FORCES LIAISON COMMITTEE

G. W. Bailey, *Chairman*

IRE-IEE INTERNATIONAL LIAISON COMMITTEE

F. S. Barton
Ralph Bown
R. H. Davies
Willis Jackson
F. B. Llewellyn
C. G. Mayer
R. L. Smith-Rose
J. A. Stratton

PROFESSIONAL RECOGNITION

G. B. Hoadley, *Chairman*

C. C. Chambers
H. F. Dart
W. E. Donovan
C. M. Edwards

Technical Committees

May 1, 1953–April 30, 1954

20. STANDARDS COMMITTEE

A. G. Jensen, *Chairman*
M. W. Baldwin, Jr. *Vice Chairman*
L. G. Cumming, *Vice Chairman*
E. Weber, *Vice Chairman*

K. E. Anspach
J. Avins
R. R. Batcher
W. R. Bennett
J. G. Brainerd
F. T. Budelman
H. Burkhard
C. A. Cady
P. S. Carter
A. G. Clavier
J. L. Dalke
A. W. Friend
F. J. Gaffney
W. D. Goodale, Jr.
R. A. Hackbusch
P. J. Herbst
J. G. Kreer
E. A. Laport
W. P. Mason
J. Z. Millar
G. D. O'Neill
C. H. Page
W. M. Pease
W. J. Poch
D. C. Ports
P. C. Sandretto
R. Serrell
R. F. Shea
R. E. Shelby
N. Smith
W. G. Tuller

SUBCOMMITTEES

20.4 Television Co-ordination

M. W. Baldwin, Jr., *Chairman*

J. E. Keister

20.5 Definitions Co-ordinating

M. W. Baldwin, Jr., *Chairman*

P. S. Carter
P. J. Herbst
J. G. Kreer, Jr.
E. A. Laport

20.8 Basic Terms

J. G. Brainerd, *Chairman*

M. W. Baldwin, Jr.
C. H. Page

1. ANNUAL REVIEW

J. Z. Millar, *Chairman*

2. ANTENNAS AND WAVEGUIDES

D. C. Ports, *Chairman*
P. H. Smith, *Vice Chairman*

P. S. Carter
J. M. DeBell
G. A. Deschamps
J. E. Eaton
H. A. Finke
A. Gardner Fox
S. Frankel
A. G. Giordano
H. Jasik
O. E. Kienow
R. L. Mattingly
John Ruze
G. Sinclair

SUBCOMMITTEES

2.2 Waveguide and Transmission Line Definitions

P. H. Smith, *Chairman*

G. Deschamps
H. Jasik
R. L. Mattingly

2.3 Antennas and Waveguides West Coast Subcommittee

S. Fraenkel, *Chairman*

E. T. Jaynes
S. Kerber
T. Moreno
N. Schrock
S. Sensiper
S. Silver
R. S. Wehner

3. AUDIO TECHNIQUES

C. A. Cady, *Chairman*
D. E. Maxwell, *Vice Chairman*

H. W. Augustadt
W. Lindsay Black
D. H. Castle
J. K. Hilliard
F. L. Hopper
I. M. Kerney
R. A. Miller
L. D. Runkle
W. E. Stewart

SUBCOMMITTEES

3.1 Definitions of Audio Systems and Components Excluding Recording

H. W. Augustadt, *Chairman*

J. A. Green
H. D. Harris
F. L. Hopper

3.2 Methods of Measurement of Audio Systems and Components Excluding Recording

W. L. Black, *Chairman*

W. W. Dean
I. G. Easton
R. H. Edmondson
I. M. Kerney
D. E. Maxwell
W. E. Stewart

4. CIRCUITS

W. R. Bennett, *Chairman*
S. J. Mason, *Vice Chairman*

J. T. Bangert
J. G. Brainerd
A. R. D'Heedene
T. R. Finch
R. M. Foster
W. H. Huggins
H. L. Krauss
J. G. Linvill
W. A. Lynch
P. F. Ordung
E. H. Perkins
E. J. Robb
W. N. Tuttle
F. H. Williams

SUBCOMMITTEES

4.1 Transistor Circuitry

J. G. Linvill, *Chairman*

T. R. Finch
A. W. Lo
S. J. Mason
J. J. Suran
L. Weinberg
F. H. Williams

4.2 Linear Lumped-Constant Passive Circuits

R. L. Dietzold, *Chairman*

J. G. Brainerd
A. R. D'Heedene
R. M. Foster
H. Krauss
C. H. Page
W. N. Tuttle

4.3 Circuit Topology

R. M. Foster, *Chairman*

R. L. Dietzold
S. Goldman
E. A. Guillemin
J. Riordan

4.4 Linear Varying-Parameter and Non-Linear Circuits

W. R. Bennett, *Chairman*

J. G. Kreer, Jr.
C. H. Page
J. R. Weiner

4.5 Time-Domain Network Analysis and Synthesis

W. H. Huggins, *Chairman*

S. Goldman
W. H. Kautz
J. G. Linvill
S. J. Mason
D. F. Tuttle, Jr.

4.7 Linear Active Circuits Including Networks with Feedback and Servomechanism Circuits

W. A. Lynch, *Chairman*

H. Lauer
J. G. Linvill
J. M. Manley
E. H. Perkins
J. R. Ragazzini
C. F. Rehberg

4.8 Circuit Components

A. R. D'Heedene, *Chairman*

4.9 Fundamental Qualities

H. L. Krauss, *Chairman*

P. F. Ordung
J. D. Ryder

6. ELECTROACOUSTICS

W. D. Goodale, Jr., *Chairman*
B. B. Bauer, *Vice Chairman*

Michel Copel
H. C. Hardy
A. S. Hegeman, Jr.
W. F. Meeker
H. F. Olson
R. J. Rockwell
V. Salmon
E. S. Seeley
P. S. Veneklasen

7. ELECTRON DEVICES

G. D. O'Neill, *Chairman*
R. M. Ryder, *Vice Chairman*

A. E. Anderson
E. M. Boone
R. S. Burnap
W. J. Dodds
G. A. Espersen
W. R. Ferris
M. S. Glass
T. J. Henry
M. E. Hines
R. B. Janes
S. F. Kaisel
J. W. Kearney
G. Ross Kilgore
I. E. Mouromtseff
L. S. Nergaard
H. L. Owens
P. A. Redhead
A. C. Rockwood
W. G. Shepherd
R. W. Slinkman
C. M. Wheeler

SUBCOMMITTEES

7.2 Cathode-Ray and Television Tubes

R. B. Janes, *Chairman*

K. A. Hoagland
R. G. Stoudenheime

7.3 Gas Tubes

H. L. Thorson, *Chairman*

J. H. Burnett
W. A. Depp
E. J. Handley
R. A. Herring
D. E. Marshall
W. C. Schmitt
W. W. Watrous
W. M. Webster
H. H. Wittenberg

7.3.1 Task Group on Methods of Test for TR and ATR Tubes

K. Garoff, *Chairman*

H. F. Baker
I. Birnbaum
T. R. Bristol
W. R. Hayter
H. Heins
F. McCarthy
L. W. Roberts
M. S. Wheeler

7.4 Power Output High-Vacuum Tubes

C. E. Fay, *Chairman*

J. W. Clark
H. D. Doolittle
T. A. Elder
G. A. Espersen
J. W. Greer
I. E. Mouromtseff
E. E. Spitzer
C. Veronda
W. G. Wagener
C. M. Wheeler
A. K. Wing

7.4.1 Magnetron Working Group Under POHVT

G. A. Espersen, *Chairman*
R. R. Moats, *Secretary*

N. Alstad
R. S. Briggs
H. W. Cole
T. P. Curtis
M. S. Glass
B. Kumpfer
E. C. Okress
S. Weston

7.6 Small High-Vacuum Tubes

T. J. Henry, *Chairman*

E. M. Boone
R. C. Hergenrother
M. E. Hines
E. H. Hurlburt
I. Meth
W. T. Millis
W. G. Shepherd
R. W. Slinkman

7.6.2 Task Group on Traveling-Wave Tubes

M. E. Hines, *Chairman*

H. D. Arnett
W. J. Dodds
L. M. Field
R. G. E. Hutter
J. R. Pierce
S. E. Webber

7.6.3 Task Group on Noise Under SSHVT

R. M. Ryder, *Chairman*

J. J. Freeman
W. A. Harris
D. O. North
E. K. Stodola

7.7 Solid State Devices

A. E. Anderson, *Chairman*

J. B. Angell
S. J. Angello
C. B. Brown
W. C. Dunlap
J. R. Flegal
R. W. Grantham
J. Kurshan
H. L. Owens
W. J. Pietenpol
B. J. Rothlein
H. Sacher
E. J. Sees

7.7.2 Semiconductors—Methods of Test

W. J. Pietenpol, *Chairman*

D. A. Alsberg
A. Coblenz
L. J. Giacoletto
H. F. Heath
C. L. Rouault

7.7.3 Semiconductors—Definitions

S. J. Angello, *Chairman*

R. B. Adler
J. M. Early
B. J. Rothlein
J. S. Schaffner
K. Uhler

7.7.4 Methods of Test

J. J. Ebers, *Chairman*

A. W. Berger
B. N. Slade
R. L. Trent
J. Weisman
R. L. Wooley

7.11 Test Methods for High-Vacuum Microwave Tubes

G. A. Esperson, *Chairman*

E. M. Boone
J. H. Bryant
H. W. Cole
L. M. Field
M. S. Glass
A. E. Harrison
M. E. Hines
R. A. LaPlante
R. R. Moats
C. R. Moster
W. G. Shepherd
S. Weston

7.11.1 Task Group on Non-Operating Characteristics of Microwave Tubes

G. A. Esperson, *Chairman*

B. Arfin
E. M. Boone
M. S. Glass
E. D. Reed
S. Weston

7.11.2 Task Group on Operating Measurements of Microwave Oscillator Tubes

R. R. Moats, *Chairman*

R. S. Briggs
T. P. Curtis
C. Dodd
G. I. Klein
B. D. Kumpfer
R. A. LaPlante
E. C. Okress
R. Unger

CONSULTANTS

G. E. Hackley
A. E. Harrison
O. C. Lundstrom
E. D. McArthur
W. G. Shepherd

7.11.3 Task Group on Operating Measurements of Microwave Amplifier Tubes

H. W. Cole, *Chairman*

C. Dodd
H. Hersh
R. G. E. Hutter
A. W. McEwan
C. R. Moster
R. W. Peter
S. E. Webber

CONSULTANTS

J. H. Bryant
M. Chodorow
C. C. Cutler
L. M. Field
A. E. Harrison
M. E. Hines
C. R. Learned
L. D. Smullin
D. Watkins

Ad Hoc Committee To Make Critical Review of Organization of Committee 7

M. E. Hines, *Chairman*

R. S. Burnap
L. S. Nergaard
G. D. O'Neill
R. M. Ryder

8. ELECTRONIC COMPUTERS

R. Serrell, *Chairman*
D. R. Brown, *Vice Chairman*

S. N. Alexander
R. D. Elbourn
M. Middleton, Jr.
C. D. Morrill
G. W. Patterson
J. A. Rajchman
N. Rochester
C. V. L. Smith
R. L. Snyder, Jr.
W. H. Ware
C. R. Wayne
J. R. Weiner
C. F. West
Way Dong Woo

SUBCOMMITTEES

8.3 Static Storage Elements

J. Rajchman, *Chairman*

A. O. Black
T. H. Bonn
H. R. Brownell
T. C. Chen
E. Gelband
M. K. Haynes
C. G. Horstman
M. Littmann
A. Nyman
W. M. Papian
E. A. Sands
N. B. Saunders
D. H. Toth

8.4 Definitions (Eastern Division)

N. Rochester, *Chairman*

R. D. Elbourn
L. C. Hobbs
R. P. Mayer
G. W. Patterson
J. R. Weiner

8.5 Definitions (Western Division)

W. H. Ware, *Chairman*

H. T. Larson
W. E. Smith
W. S. Speer
L. D. Stevens
R. Thorensen

8.6 Magnetic Recording for Computing Purposes

S. N. Alexander, *Chairman*

9. FACSIMILE

H. Burkhard, *Chairman*
A. G. Cooley, *Vice Chairman*

I. H. Franzel
J. Hackenberg
F. A. Hester
J. V. Hogan
S. A. Lawson
K. R. McConnell
P. Mertz
K. W. Pfleger
M. Rehm
C. J. Young
R. J. Wise

10. INDUSTRIAL ELECTRONICS

J. L. Dalke, *Chairman*
E. Mittelmann, *Vice Chairman*

G. P. Bosomworth
J. M. Cage
E. W. Chapin
J. E. Eiselein
C. W. Frick
G. W. Klingamen
H. R. Meahl
J. H. Mennie
P. E. Ohmart
H. W. Parker
S. I. Rambo
W. Richter
W. C. Rudd
E. H. Schulz
C. F. Spitzer
W. R. Thurston
M. P. Vore
J. Weinberger

SUBCOMMITTEES

10.1 Definitions for Induction and Dielectric Heating

C. F. Spitzer, *Chairman*

G. P. Bosomworth
J. M. Cage
J. Dalke
E. Mittelmann
W. Richter

10.2 Dielectric Measurements

J. Dalke, *Chairman*

G. W. Klingaman
H. R. Meahl
J. H. Mennie
F. C. Spitzer

10.4 Methods of Measurement

E. Mittlemann, *Chairman*

J. M. Cage
J. L. Dalke
S. I. Rambo
E. H. Schulz
W. R. Thurston

11. INFORMATION THEORY AND MODULATION SYSTEMS

W. G. Tuller, *Chairman*
J. G. Kreer, Jr., *Vice Chairman*

P. L. Bargellini
W. R. Bennett
T. P. Cheatham, Jr.
W. B. Davenport, Jr.
L. A. DeRosa
P. Elias
D. D. Grieg
J. V. Harrington
H. W. Kohler
E. R. Kretzmer
V. D. Landon
N. Marchand
L. A. Meacham
W. Palmer
D. Pollack

12. NAVIGATION AIDS

P. C. Sandretto, *Chairman*
H. R. Mimno, *Vice Chairman*

W. B. Burgess
H. Davis
R. E. Gray
H. I. Metz
W. Palmer
L. M. Sherer

SUBCOMMITTEES

12.2 Standard DF Measurements

E. D. Blodgett, *Chairman*
J. Kaplan, *Vice Chairman*
J. L. Allison, *Secretary*
R. Silberstein, *Alternate Secretary*

A. D. Bailey
H. I. Butler
L. M. Harding
J. J. Kelleher
H. R. Mimno
W. M. Richardson
F. M. Kratokvil
A. A. Kunze
J. T. Lawrence
J. A. Solga
J. O. Spriggs
C. A. Strom, Jr.
S. R. Thrift
J. H. Trexler

12.3 Measurement Standards for Navigation Systems

F. Moskowitz, *Chairman*
S. B. Fishbein, *Secretary*

P. Adams
S. Anderson
R. Battle
P. Hansel
M. Leifer
G. Litchford
J. T. MacLemore
J. S. Prichard
P. C. Sandretto
P. W. Siglin
V. Weihe

14. PIEZOELECTRIC CRYSTALS

W. P. Mason *Chairman*
H. Jaffe, *Vice Chairman*

W. G. Cady
J. K. Clapp
W. A. Edson
I. E. Fair
W. D. George
E. Gerber
S. Roberts
P. L. Smith
R. A. Sykes
K. S. Van Dyke

15. RADIO TRANSMITTERS

P. J. Herbst, *Chairman*
H. Goldberg, *Vice Chairman*

T. E. Ahlstadt
J. Battison
T. J. Boerner
M. R. Briggs
A. Brown
H. R. Butler
W. R. Donsbach
L. K. Findley
T. M. Gluyas, Jr.
J. B. Heffelfinger
A. E. Kerwien
L. A. Looney
J. F. McDonald
S. M. Morrison
J. Ruston
H. B. Seabrook
G. W. Sellers
B. Sheffield
N. B. Tharp
I. R. Weir

SUBCOMMITTEES

15.1 FM Transmitters

J. Ruston, *Chairman*

J. Bose
J. R. Boykin
N. Marchand
P. Osborne
H. P. Thomas

15.2 Radio-Telegraph Transmitters up to 50 MC

B. Sheffield, *Chairman*

H. R. Butler
J. L. Finch
J. F. McDonald
F. D. Webster
I. R. Weir

15.3 Double Sideband AM Transmitters

J. B. Heffelfinger, *Chairman*

R. B. Beetham
L. K. Findley
L. A. Looney

15.4 Pulse-Modulated Transmitters

H. Goldberg, *Chairman*

R. Bateman
L. L. Bonham
W. F. Cook
H. Kohler
G. F. Montgomery
A. E. Newlon
W. K. Roberts
B. D. Smith

15.5 Single Sideband Radio Communication Transmitters

A. Brown, *Chairman*

M. R. Briggs (ex-officio)
J. P. Costas
H. E. Goldstine
L. Kahn
E. A. Laport
J. B. Singel

15.6 Television Broadcast Transmitters

T. M. Gluyas, Jr., *Chairman*

F. J. Bias
E. Bradburd
P. J. Herbst (ex-officio)
L. A. Looney
J. Ruston

16. MOBILE COMMUNICATION SYSTEMS

F. T. Budelman, *Chairman*
A. Whitney, *Vice Chairman*

A. V. Dasburg
D. B. Harris
C. M. Heiden
C. N. Kimball, Jr.
N. Monk
D. E. Noble
J. C. O'Brien
D. Talley
G. Teommey
R. W. Tuttle

17. RECEIVERS

J. Avins, *Chairman*
J. D. Reid, *Vice Chairman*

K. A. Chittick
L. E. Closson
D. E. Hartnett
K. W. Jarvis
J. K. Johnson
W. R. Koch
C. O. Marsh, Jr.
I. J. Melman
G. Mountjoy
F. R. Norton
L. Riebman
L. M. Rodgers
S. W. Seeley
R. F. Shea
W. O. Swinyard
F. B. Uphoff
R. S. Yoder

SUBCOMMITTEES

17.3 Single Sideband Receivers

K. Jarvis, *Chairman*
D. E. Norgaard

17.4 Spurious Radiation

R. F. Shea, *Chairman*

J. Avins
E. W. Chapin
K. A. Chittick
H. E. Dinger
A. B. Glenn
W. R. Koch
T. S. Loeser
R. A. Maher
F. L. Pampel
L. M. Rodgers
E. H. Schrot
H. Schwarz
S. W. Seeley
C. G. Seright
W. B. Smith
J. W. Stratman
W. O. Swinyard
H. J. Tyzzer
R. S. Yoder

17.5 Annual Review Material

L. M. Harris, *Chairman*

17.8 Task Group to Review I.E.C. Proposal on Standardization of Measurements of Receivers for AM Broadcast Transmissions

W. O. Swinyard, *Chairman*

H. Adler
W. F. Cotter
R. DeCola
J. K. Johnson
C. O. Marsh
E. R. Pfaff
S. C. Spielman
R. Yoder

17.9 Automatic Frequency Control

F. B. Uphoff, *Chairman*
J. R. Locke

19. SOUND RECORDING AND REPRODUCING

A. W. Friend, *Chairman*
L. Thompson, *Vice Chairman*
M. S. Corrington, *Vice Chairman*

S. J. Begun
S. M. Fairchild
R. M. Fraser
C. J. Lebel
J. H. McGuigan
A. P. G. Peterson
H. E. Roys
H. Schecter
C. F. West
R. E. Zenner

SUBCOMMITTEES

19.1 Magnetic Recording

A. P. G. Peterson, *Chairman*

W. H. Erickson
J. H. McGuigan
W. W. Wetzel
R. E. Zenner

19.2 Mechanical Recording

L. Thompson, *Chairman*

W. S. Bachman
S. M. Fairchild
T. Lindenberg
A. R. Morgan
R. C. Moyer
F. W. Roberts
M. X. Royston
R. H. Schlegel
A. S. R. Toby

19.3 Optical Recording

R. M. Fraser, *Chairman*

Price Fish
E. Miller
C. Townsend

Task Group C.C.I.R. Task Group of IRE Committee 19

H. R. Roys, *Chairman*

W. S. Bachman
R. M. Fraser
A. W. Friend
R. C. Moyer
L. Thompson

21. SYMBOLS

K. E. Anspach, *Chairman*
H. R. Terhune, *Vice Chairman*

F. M. Bailey
A. G. Clavier
W. J. Everts
W. A. Ford
R. T. Haviland
O. T. Laube
C. D. Mitchell
C. Neitzert
M. B. Reed
A. C. Reynolds, Jr.
M. P. Robinson
M. S. Smith
H. P. Westman

SUBCOMMITTEES

21.2 Graphical Symbols for Semiconductors

C. D. Mitchell, *Chairman*

T. R. Finch
R. A. Henle
F. J. Lingel
R. F. Merrithew
W. H. Miller
M. P. Robinson
A. D. Shaw
E. H. Ulm
J. G. Weissman
H. J. Woll

21.3 Subcommittee on Functional Representation of Control, Computing and Switching Equipment

A. C. Reynolds, Jr., *Chairman*

T. G. Cober
C. W. Frank
J. W. Gorgas
H. F. Herbig
G. W. Hobbs
H. P. Kraatz
F. T. Meyer
E. W. Olcutt
J. S. Osborne
S. W. Roberts
F. J. Roehm
G. M. Sokol

21.4 Subcommittee on Abbreviations, Letter Symbols, and Graphical Symbols for Feedback Control Systems

F. M. Bailey, *Chairman*

H. Freeman
V. J. Louden
T. F. Mahoney

21.5 Subcommittee on New Proposals and Special Assignments

M. P. Robinson, *Chairman*

21.6 Annual Review

H. P. Westman, *Chairman*

22. TELEVISION SYSTEMS

R. E. Shelby, *Chairman*

W. F. Bailey
M. W. Baldwin, Jr.
R. M. Bowie
A. H. Brolly
J. E. Brown
K. A. Chittick
C. G. Fick
D. G. Fink
P. C. Goldmark
R. N. Harmon
J. E. Hayes
J. L. Hollis
A. G. Jensen
I. J. Kaar
R. D. Kell
P. J. Larsen
H. T. Lyman
L. Mautner
J. Minter
A. F. Murray
D. W. Pugsley
M. Silver
D. Smith
M. E. Strieby
A. Talamini
W. T. Wintringham

SUBCOMMITTEES

22.1 Definitions

M. W. Baldwin, Jr., *Chairman*

A. V. Bedford
J. W. Christensen
S. Helt
C. J. Hirsch
D. L. MacAdam
H. A. Samulon
E. Sieminski
R. E. Waggener
W. T. Wintringham

22.2 Television Picture Element

R. M. Bowie, *Chairman*

W. E. Bradley
S. Helt
M. Leifer
P. Mertz
H. A. Samulon
O. H. Schade

23. VIDEO TECHNIQUES

W. J. Poch, *Chairman*
A. J. Baracket, *Vice Chairman*

S. W. Athey
J. Battison
K. B. Benson
E. M. Coan
S. Doba, Jr.
V. J. Duke
G. L. Fredendall
J. R. Hefele
J. L. Jones
L. L. Lewis
C. G. Pierce
B. F. Tyson

SUBCOMMITTEES

23.2 Utilization, Including Video Recording: Methods of Measurement

R. L. Garman, *Chairman*

S. W. Athey
K. B. Benson
J. M. Brumbaugh
V. J. Duke
G. Gordon
L. D. Grignon
S. Kraemer
H. Milholland
H. J. Schlafly

23.3 Video Systems and Components: Methods of Measurement

A. J. Baracket, *Chairman*

I. C. Abrahams
R. Betts
R. DeBaun
G. L. Fredendall
J. R. Hefele
A. Lind
J. F. Wiggin

23.4 Video Signal Transmission: Methods of Measurement

J. L. Jones, *Chairman*

J. M. Barstow
K. B. Benson
R. D. Chipp
S. Doba, Jr.
L. R. Moffett
R. M. Morris
K. E. Mullenger
R. S. O'Brien
C. A. Rosencrans
E. H. Schreiber
B. F. Tyson

24. WAVE PROPAGATION

N. Smith, *Chairman*

E. W. Allen, Jr.
S. L. Bailey
A. R. Beach
H. G. Booker
C. R. Burrows
T. J. Carroll
A. B. Crawford
A. Earl Cullum, Jr.
H. E. Dinger
W. S. Duttera
R. E. Fontana
I. H. Gerks
M. C. Gray
D. E. Kerr
M. Kline
R. K. Moore
M. G. Morgan
K. A. Norton
H. O. Peterson
G. Sinclair
R. L. Smith-Rose
A. W. Straiton
A. H. Waynick
J. W. Wright
T. A. Wright

SUBCOMMITTEES

24.1 Standards and Practices

H. O. Peterson, *Chairman*

W. S. Duttera
F. M. Greene
G. Sinclair
J. W. Wright

24.2 Theory and Application of Tropospheric Propagation

T. Carroll, *Chairman*

H. G. Booker
A. B. Crawford
M. C. Gray
A. W. Straiton
R. P. Wakeman

24.3 Theory and Application of Ionospheric Propagation

M. G. Morgan, *Chairman*

R. Bateman
K. L. Bowles
R. A. Helliwell
C. W. McLeish
J. H. Meek

24.4 Definitions and Publications

G. Sinclair, *Chairman* (resigned)

A. B. Crawford
J. E. Eaton
E. G. Fubini
I. H. Gerks
H. Jansky
M. Katzin
D. E. Kerr

24.6 Radio Astronomy

C. R. Burrows, *Chairman*

A. E. Covington
F. T. Haddock, Jr
J. P. Hagen

24.7 Terrestrial Radio Noise

H. Dinger, *Chairman*

25. MEASUREMENTS AND INSTRUMENTATION

F. J. Gaffney, *Chairman*
P. S. Christaldi, *Vice Chairman*

J. L. Dalke
H. Dinger
G. D. Fredendall
W. D. George
W. J. Mayo-Wells
G. A. Morton
C. D. Owens
A. P. G. Peterson
J. G. Reid, Jr.
J. R. Steen

SUBCOMMITTEES

25.1 Basic Standards and Calibration Methods

W. George, *Chairman*

S. L. Bailey
G. L. Davies
F. J. Gaffney

25.2 Dielectric Measurements

J. Dahlke, *Chairman*

C. A. Bieling
F. A. Muller

25.3 Magnetic Measurements

C. D. Owens, *Chairman*

W. Cairnes
G. S. Fay
P. H. Haas
E. J. Smith

25.4 Audio-Frequency Measurements

A. P. G. Peterson, *Chairman*

R. Grimm
R. A. Long

25.5 Video Frequency Measurements

G. L. Fredendall, *Chairman*

J. Fisher
R. Palmer
H. A. Samulon
W. R. Thurston

25.6 High Frequency Measurements

R. V. Lowman, *Chairman*

R. A. Braden
I. G. Easton
C. J. Franks
F. J. Gaffney
G. B. Hoadley
E. W. Houghton
D. Keim
B. M. Oliver
B. Parzen

25.8 Interference Measurements

H. E. Dinger, *Chairman*

F. H. Dickson
C. W. Frick
F. M. Greene
R. M. Showers
A. H. Sullivan, Jr.

25.9 Measurement of Radio Activity

G. A. Morton, *Chairman*

R. L. Butenhoff
D. L. Collins
L. F. Curtiss
L. W. Davison
F. D. Lewis
A. Lovoff
M. A. Schultz
W. W. Schultz

25.10 Oscillography

P. S. Christaldi, *Chairman*
M. J. Ackerman, *Vice Chairman*

R. R. Batcher
M. E. Clark
E. Durbin
R. Feldt
E. R. Haberland
H. M. Joseph
J. H. Mulligan, Jr.
A. L. Stillwell
H. Vollum

25.11 Statistical Quality Control

J. R. Steen, *Chairman*

J. Dorfman
B. Hecht
R. F. Rollman

25.13 Telemetering

W. J. Mayo-Wells, *Chairman*

J. L. Blackburn
J. F. Brinster
R. E. Colander
A. P. Gruer
R. L. Harding
C. H. Hoeppner
M. V. Kiebert
F. W. Lehan
E. E. Lynch
M. G. Pawley
W. E. Phillips
G. M. Thynell
F. L. Verwiebe
G. F. C. Weedon
W. A. Wildhack

25.14 Electronic Components

J. G. Reid, Jr., *Chairman*

G. B. Devey
J. C. P. Long
J. H. Muncy
A. W. Rodgers
N. H. Taylor
A. E. Zbodysz

26. FEEDBACK CONTROL SYSTEMS

W. M. Pease, *Chairman*

G. A. Biernson
V. B. Haas, Jr.
R. J. Kochenburger
W. K. Linvill
J. C. Lozier
E. A. Sabin
P. Travers
J. E. Ward
R. B. Wilcox
S. B. Williams

26.1 Terminology for Feedback Control Systems

J. C. Lozier, *Chairman*

M. R. Aaron
G. R. Arthur
V. Azgapetian
J. O. Edson
T. Flynn
L. Goldman
C. F. Rehberg
F. Zweig

INSTITUTE REPRESENTATIVES IN COLLEGES—1953*

*Agricultural and Mechanical College of Texas: H. C. Dillingham
*Akron, University of: P. C. Smith
*Alabama Polytechnic Institute: R. M. Steere
*Alberta, University of: J. W. Porteous
*Arizona, University of: H. E. Stewart
*Arkansas, University of: W. W. Cannon
*British Columbia, University of: L. R. Kersey
*Brooklyn, Polytechnic Institute of (Day Division): L. Goldstone
*Brooklyn, Polytechnic Institute of (Evening Division): Appointment later
*Brown University: J. P. Ruina
*Bucknell, University of: George Irland
*California Institute of Technology: J. N. Thurston
*California State Polytechnic College: Clarence Radius
*California, University of: H. J. Scott
California, University of at Los Angeles: E. F. King
*Carnegie Institute of Technology: G. H. Royer
*Case Institute of Technology: J. D. Johannesen
*Cincinnati, University of: A. B. Bereskin
*Clarkson, College of Technology: Joseph Salerno
*Colorado, University of: W. G. Worcester
*Columbia University: Lawrence O'Neill
*Connecticut, University of: V. B. Haas, Jr.
*Cooper Union: J. B. Sherman
*Cornell University: True McLean
Dartmouth College: M. G. Morgan
*Dayton, University of: Appointment later
*Delaware, University of: H. S. Bueche
*Denver, University of: R. C. Webb
*Detroit, University of: Thomas Yamauchi
*Drexel Institute of Technology: R. T. Zern
Duke University: H. A. Owen
*Fenn College: K. S. Sherman
*Florida, University of: S. P. Sashoff
*George Washington University: W. H. Gossard
*Georgia Institute of Technology: B. J. Dasher
Harvard University: E. L. Chaffee
*Illinois Institute of Technology: R. M. Leger
*Illinois, University of: P. H. Schwarzlose
*Iowa State College: G. A. Richardson
*Iowa, State University of: L. A. Ware
*John Carroll University: J. L. Hunter
*Johns Hopkins University: Ferdinand Hamburger, Jr.
*Kansas State College: J. E. Wolfe
*Kansas, University of: D. G. Wilson
*Kentucky, University of: N. B. Allison
*Lafayette College: F. W. Smith
*Lehigh University: D. E. Mode
*Louisiana State University: L. V. McLean
*Louisville, University of: S. T. Fife
*Maine, University of: Appointment later
*Manhattan College: T. P. Canavan
Manitoba, University of: R. G. Anthes
*Marquette University: Appointment later
*Maryland, University of: G. F. Corcoran
*Massachusetts Institute of Technology: E. A. Guillemin, W. H. Radford
Massachusetts, University of: C. S. Roys

---

* Colleges with approved Student Branches.

McGill University: F. S. Howes
*Miami, University of: F. B. Lucas
*Michigan College of Mining and Technology: R. J. Jones
*Michigan State College: I. O. Ebert
*Michigan, University of: L. N. Holland
*Minnesota, University of: Leroy Anderson
*Mississippi State College: P. T. Hutchison
*Missouri School of Mines and Metallurgy: R. E. Nolte
*Missouri, University of: G. V. Lago
*Montana State College: R. C. Seibel
*Nebraska, University of: Charles Rook
Nevada, University of: I. J. Sandorf
*Newark College of Engineering: D. W. Dickey
*New Hampshire, University of: A. L. Winn
*New Mexico College of Agriculture and Mechanic Arts: H. A. Brown
*New Mexico, University of: Appointment later
*New York, College of the City of: Harold Wolf
*New York University: Sidney Shamis
*North Carolina State College: G. B. Hoadley
*North Dakota Agricultural College: E. M. Anderson
*North Dakota, University of: Clifford Thomforde
*Northeastern University: G. E. Pihl
*Northwestern University: A. H. Wing, Jr.
*Notre Dame, University of: H. E. Ellithorn
*Ohio State University: R. A. Neubauer
*Ohio University: D. B. Green
*Oklahoma Agricultural and Mechanical College: A. L. Betts
Oklahoma, University of: C. L. Farrar
*Oregon State College: A. L. Albert
*Pennsylvania State College: J. N. Warfield
*Pennsylvania, University of: D. F. Hunt
*Pittsburgh, University of: John Brinda, Jr.
*Pratt Institute: David Vitrogan
*Princeton University: N. W. Mather
*Purdue University: R. P. Siskind
Queens University: H. H. Stewart
*Rensselaer Polytechnic Institute: H. D. Harris
*Rhode Island, University of: R. S. Haas
Rice Institute: C. R. Wischmeyer
Rose Polytechnic Institute: H. A. Moench
*Rutgers University: J. L. Potter
*St. Louis University: G. E. Dreifke
*San Diego State College: D. C. Kalbfell
*San Jose State College: Harry Engwicht
Santa Clara, University of: H. P. Nettesheim
*Seattle University: Appointment later
*South Carolina, University of: Appointment later
*South Dakota School of Mines and Technology: Appointment later
*Southern California, University of: G. W. Reynolds
*Southern Methodist University: Paul Harton
*Stanford University: H. P. Blanchard
*Stevens Institute of Technology: A. C. Gilmore, Jr.
*Syracuse, University of: Herbert Hellerman
*Tennessee, University of: E. D. Shipley
*Texas, University of: H. W. Smith
*Texas Technological College: H. A. Spuhler
*Toledo, University of: R. E. Weeber
*Toronto, University of: George Sinclair
*Tufts College: A. H. Howell
*Tulane University: J. A. Cronvich
United States Naval Post Graduate School: G. R. Giet
*Utah State Agricultural College: Clayton Clark
*Utah, University of: C. L. Alley
*Vermont, University of: W. L. Steinmann
*Villanova College: Appointment later
*Virginia Polytechnic Institute: R. R. Wright
*Virginia, University of: J. C. Mace
*Washington, University of: H. M. Swarm
*Wayne University: D. V. Stocker
Western Ontario, University of: E. H. Tull and J. H. Blackwell
*West Virginia University: R. C. Colwell
*Wisconsin, University of: Glenn Koehler
Witwatersrand, University of: G. R. Bozzoli
*Worcester Polytechnic Institute: H. H. Newell
*Wyoming, University of: W. M. Mallory
*Yale University: J. G. Skalnik

INSTITUTE REPRESENTATIVES ON OTHER BODIES—1953

Council of the American Association for the Advancement of Science: J. C. Jensen
ASA Standards Council: Axel G. Jensen; Ernst Weber, L. G. Cumming, alternates
ASA Electrical Standards Board: L. G. Cumming, A. G. Jensen, F. B. Llewellyn
ASA Graphic Standards Board: A. G. Clavier; K. E. Anspach, alternate
ASA Sectional Committee (C16) on Radio (Sponsored by IRE): S. I. Bailey, Chairman; L. G. Cumming, Secretary; A. G. Jensen, J. Avins
ASA Sectional Committee (C39) on Electrical Measuring Instruments: Wilson Aull, Jr., F. J. Gaffney
ASA Sectional Committee (C42) on Definitions of Electrical Terms: M. W. Baldwin, Jr., A. G. Jensen, Haradon Pratt, J. G. Brainerd
ASA Subcommittee (C42.1) on General Terms: J. G. Brainerd
ASA Subcommittee (C42.6) on Electrical Instruments: Ernst Weber; F. J. Gaffney, alternate
ASA Subcommittee (C42.13) on Communications: J. C. Schelleng
ASA Subcommittee (C42.14) on Electron Tubes: L. S. Nergaard
ASA Sectional Committee (C60) on Standardization on Electron Tubes: L. S. Nergaard, C. E. Fay
ASA Sectional Committee (C61) on Electric and Magnetic Magnitudes and Units: S. A. Schelkunoff, J. W. Horton, E. S. Purington
ASA Sectional Committee (C63) on Radio-Electrical Coordination: John Dalke
ASA Sectional Committee (C67) on Standardization of Voltages—Preferred Voltages—100 Volts and Under: J. R. Steen
ASA Sectional Committee (YI) on Abbreviations: H. T. Haviland; H. R. Terhune, alternate
ASA Sectional Committee (Y10) on Letter Symbols and Abbreviations for Science and Engineering: A. G. Clavier; H. R. Terhune, alternate
ASA Sectional Committee (Y10.14) on Nomenclature for Feedback, Control Systems; W. M. Pease, J. R. Ragazzini, W. A. Lynch
ASA Sectional Committee (Y14) on Standards for Drawing and Drafting Room Practices: Austin Bailey; K. E. Anspach, alternate
ASA Sectional Committee (Y15) on Preferred Practice for the Preparation of Graphs, Charts and Other Technical Illustrations: H. R. Terhune; M. P. Robinson, alternate
ASA Sectional Committee (Y32) on Graphical Symbols and Designations: Austin Bailey; A. F. Pomeroy, alternate
ASA Sectional Committee (Z17) on Preferred Numbers: A. F. Van Dyck
ASA Sectional Committee (Z24) on Acoustical Measurements and Terminology: W. D. Goodale, Jr.; H. F. Olson, alternate
ASA Sectional Committee (Z57) on Sound Recording: H. E. Roys; A W. Friend, alternate
ASA Sectional Committee (Z58) on Standardization of Optics: E. Dudley Goodale; L. G. Cumming, alternate
International Radio Consultative Committee—Executive Committee of U. S. Delegation: A. G. Jensen; L. G. Cumming, alternate
International Scientific Radio Union (URSI) Executive Committee: S. L. Bailey
Joint IRE-AIEE Committee on High Frequency Measurements: R. W. Lowman, R. A. Braden, I. G. Easton, F. J. Gaffney, G. B. Hoadley, H. W. Houghton, B. Parzen, David Y. Keim, C. J. Franks, B. M. Oliver
IRE-AIEE Committee on Noise Definitions: A. W. Friend, S. Goldman, Jerry Minter, LeRoy Moffett
Joint IRE-AIEE-NEMA Co-ordination Committee on Commercial Induction and Dielectric Heating Apparatus: John Dalke; George P. Bosomworth, alternate
Joint IRE-RTMA-SMPTE-NARTB Committee for Inter-Society Coordination (Television): A. G. Jensen; M. W. Baldwin, alternate
U. S. National Committee, International Electrotechnical Commission, Advisers on Symbols: Austin Bailey; A. F. Pomeroy, alternate
U. S. National Committee, International Electrotechnical Commission, Advisers on Electrical Measuring Intruments: Wilson Aull; F. J. Gaffney, alternate
U. S. National Committee of the International Electrotechnical Commission: F. B. Llewellyn, A. G. Jensen, L. G. Cumming

IRE People

Henry C. Forbes (A'20–M'29–SM'43–F'48), president of Forbes & Wagner Inc., Silver Creek, N. Y., has passed away.

Mr. Forbes was born in Rockland, Mass., on February 27, 1899. He received the B.S. degree in electrical engineering from the University of Minnesota in 1922 and the E.E. degree in 1923.

In 1923 Mr. Forbes became assistant to the chief engineer of Cutting and Washington Radio Corp., Minneapolis, Minn., and in 1924, the Colonial Radio Corp. of Long Island City, N. Y. From 1924 to 1926 he was chief engineer with the Zenith Radio Corp. of Chicago.

Mr. Forbes then joined the Westinghouse Electric and Manufacturing Co. as a section engineer, working in East Pittsburgh, Pa. and Chicopee Falls, Mass. Here he was in charge of the engineering and design of special receivers for commercial and government service, including audio equipment and special equipment for aircraft and railroad applications.

Dr. B. Richard Teare, Jr. (A'41–SM'45–F'51), dean of graduate studies at Carnegie Institute of Technology, has been appointed dean of the College of Engineering and Science. He had been serving as associate dean.

Dr. B. R. Teare

Dr. Teare joined the Carnegie faculty in 1939, and was named Buhl Professor of electrical engineering in 1943, responsible for organizing a graduate program. In 1950 he was appointed dean of graduate studies.

A native of Menomonie, Wis., Dr. Teare received the B.S. and M.S. degrees from the University of Wisconsin in 1927 and 1928. While teaching at Yale University he received his Ph.D. in 1937.

Dr. Teare joined the General Electric Company in Schenectady in 1929. After spending four years training, he became an instructor at Yale.

During the war years Dr. Teare worked in the Naval Ordnance Laboratory and on research at Carnegie Tech for the NDRC, the Office of Scientific Research and Development, the Army Air Forces and the office of Naval Research.

Dr. Teare is a registered engineer in the states of Pennsylvania and Connecticut, and the author of several papers on engineering education. He was the recipient of the George Westinghouse Award in 1947.

Dr. Teare is a fellow of the AIEE, and a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

Dr. Seymour B. Cohn (S'41–A'44–M'46–SM'51) has joined the Aircraft Radiation Systems Laboratory of the Stanford Research Institute.

S. B. Cohn

Formerly with Sperry Gyroscope Co., Dr. Cohn was a research engineer in the Microwave Instruments and Components Department. He had been with them since 1948.

Dr. Cohn was born in Stamford, Conn. on October 21, 1920. He received the B.S. degree in electrical engineering from Yale University in 1942, and from Harvard University the M.S. degree in communication engineering in 1946 and the Ph.D. in engineering sciences and applied physics in 1948, the latter on a National Research Council Fellowship. He holds the 1942 Lamphier Award from Yale University.

From 1942 to 1945 Dr. Cohn was a special research associate in the Radio Research Laboratory of Harvard, serving partly as a technical observer for the Laboratory with the U. S. Army Air Force in the Mediterranean Theater.

◆

Dr. Oscar Norgorden (A'43) electronic scientist at the Naval Research Laboratory, Washington, D. C., died recently in Hokkaido, Japan. He was in Japan in connection with a communication project of interest to the Department of Defense, for which he had the planning responsibility.

A native of LeRoy, Minn., Dr. Norgorden was born on January 2, 1909, received his B.S. degree in 1931 from the University of Minnesota, and his Ph.D. from the same university in 1936. He was a member of Sigma Xi, Tau Beta Pi, and Eta Kappa Nu.

He joined the Naval Research Laboratory in 1936. Although primarily a mathematical physicist, his research interests at NRL were chiefly in communications antennas, systems analysis and associated fields. He was a member of Research and Development Board technical committees and also served as a consultant in electromagnetic radiation to various Naval and other national agencies.

Dr. Norgorden was a member of the American Physical Society, the Washington Philosophical Society, the American Association for the Advancement of Science, and the U. S. Naval Institute.

Neal McNaughten (A'44–M'45) has joined the RCA Victor Division of the Radio Corporation of America as administrator of the broadcast market planning section of the Engineering Products Department. He will supervise long-range planning of the company's broadcast business.

Before joining RCA Mr. McNaughten had been director of engineering for the National Association of Radio and Television Broadcasters since 1949. He became associated with the NARTB in 1948 as assistant director.

Born in Pueblo, Colo. in 1911, Mr. McNaughten studied at the University of Colorado. He entered broadcasting as operator at KRGV in Weslaco, Texas, becoming chief engineer in 1934.

In 1941 Mr. McNaughten became a monitoring officer for the Federal Communications Commission, serving in Puerto Rico, Denver, and Allegan, Mich. In 1943 he was made assistant chief of the FCC's Treaty Section, and a member of the President's Interdepartmental Radio Advisory Committee. In 1945 he was promoted to chief of the Standard Allocation Section and participated in the Atlantic City International Telecommunications Conference.

Mr. McNaughten has served on various professional committees, and is currently chairman of the Committee on Broadcasting, and the U. S. Preparatory Group of International Radio Consultative Committee.

◆

M. Clifford Agress (M'51) is now President and Sales Manager of A. J. F. Industries, Inc.

A graduate of Pratt Institute in 1939, during the last war, Mr. Agress was chief engineer of Penn Boiler and Burner Manufacturing Co. in the Electric Power Division. Formerly he was affiliated with Lloyd Rogers and Co. He also maintained his own consulting engineering firm in New York.

Mr. Agress joined A. J. F in 1945, where, as Chief Engineer, he was in charge of design and development of various components, plant layout, development of machines and equipment, and quality control.

Mr. Agress is a member of the Illuminating Engineering Society, the American Engineering Society, and is a member and former director of the Kings County Chapter of the New York State Society of Professional Engineers.

◆

J. R. Steen (M'36–SM'43–F'50) has been appointed to the Committee on Preferred Voltages—100 Volts and Under, of the American Standards Association, representing the IRE. This committee has developed a list of preferred voltages and are working on their distribution.

Mr. Steen holds the position of director of quality control for Sylvania Electric Products, Inc. He joined Sylvania in 1931. A graduate of the University of Wisconsin in 1923, he was formerly associated with the General Electric Company, the Grigsby-Grunow Company, and the Bell Telephone Laboratories.

Mr. Steen is also a member of the ASA Committee on the Standardization of Electron Tubes.

Books

Thermionic Vacuum Tubes by W. H. Aldous and Sir Edward Appleton

Published (1952) by John Wiley & Sons, Inc., 440 Fourth Ave., New York 16, N. Y. 151 pages+4-page index+4-page reference+vii pages. 98 figures. 6×4½. $2.50.

W. H. Aldous is a member of a research staff at the General Electric Company Research Laboratories, Wembly, England; Sir Edward Appleton is principal and vice chancellor at the Edinburgh University.

This small monograph on electron tubes is one of the excellent series of Menthuen's Monographs on Physical Subjects, and has been completely revised and brought up-to-date in the light of modern tube practice. The earlier edition was very well received internationally, and this later monograph will undoubtedly prove equally popular.

The authors have provided an excellent discussion of the applications of modern tubes as amplifiers, rectifiers, frequency multipliers and oscillators. Of special interest is the treatment of space charge control tubes at ultra high frequencies.

There is an excellent list of references at the conclusion of the monograph for the use of those who would like to pursue the subject further.

We are glad to recommend this small monograph to tube engineers in all fields.

SCOTT HELT
DuMont Laboratories, Inc.
Passaic, N. J.

How to Improve the Utilization of Engineering Manpower. Prepared by the National Society of Professional Engineers.

52 pages+3-page index. Size 6×9. Price: Single copies, $2.00.

A summary report entitled, "How to Improve the Utilization of Engineering Manpower" has been issued by the Conference Board for Industry of the National Society of Professional Engineers. It is the second of a series of summary reports started in 1951. It pools the experience of more than 495 companies employing engineers.

The information contained in the report is intended primarily to help industry use its engineers most effectively. The subject matter is well organized and easy to read.

Briefly, the contents include discussion of the following points:

a. Indoctrination of engineers.
b. Making the existing engineering staff more effective.
c. The use of supporting personnel.
d. Are engineers' talents being wasted?
e. Auxiliary sources of engineering talent.
f. Engineering turnover—causes and results.
g. Preparing the engineers of the future.

The chapter on point (d) hardly does justice to the subject. The use of engineers for drafting, report writing and many other subprofessional activities is widespread in a number of organizations and should be discouraged. Unless emphasis of this nature is included in the treatment of point (d) the reader may pass it over too lightly.

The source of future engineers is the high schools. If our economy is to overcome the current large deficit of engineers and meet the increasing demands of the future, the practicing engineer and organizations employing engineers must co-operate to encourage promising individuals in the high schools. This has been discussed under (g) but needs further emphasis.

The subject of this report has been treated by other authors. With the exception of the comments on points (d) and (g), it can be considered an up-to-date and useful presentation of an important matter.

JOHN L. CALLAHAN
RCA Laboratories
New York, N. Y.

Vacuum-Tube Oscillators by William A. Edson

Published (1953) by John Wiley & Sons, Inc., 440 Fourth Ave., New York 16, New York, and Chapman & Hall, Limited, London, England. 450 pages+17-page index+14-page bibliography+xv pages. 261 figures. 5¾×9. $7.50.

William A. Edson is visiting professor, Department of Electrical Engineering, and research associate, Electronics Research Laboratory, Stanford University.

This new book treats in detail all sorts of harmonic and relaxation oscillators using conventional vacuum tubes, transistors, and other short-transit-time devices. It does not cover long-transit-time, or microwave, tubes.

Within its very wide scope, the book proceeds from fundamentals straight through to detailed, practical discussions of particular topics and circuits. Some of the matters covered are: cyclograms, van der Pol's equation, Nyquist's stability criterion, resonators, quartz crystals, magneto-striction, thermistors, intermittent operation, parasitics, relaxation oscillators and multivibrators, frequency control, synchronization of oscillators, frequency multiplication and division, noise, modulation, long line effects.

The book is well organized and clearly written. It could serve well either as a text for a course introducing the subject, or as a reference for one who, acquainted with general principles, wants specific guidance which goes deeper than mere handbook lore.

Only a man who had spent as much time on the subject as Dr. Edson has could adequately criticize this book in detail. I found little to quarrel with in it, and nothing to which I could object very seriously.

J. R. PIERCE
Bell Telephone Laboratories, Inc.
Murray Hill, N. Y.

NEW BOOKS

English-French Dictionary, of Terms Relative to Electrotechnique, Electronic and Joint Applications by H. Piraux

Published (1952) by Editions Eyrolles 61, Boulevard St. Germain, 61. Paris 5, France. 265 pages +31 pages of drawings and tables. 6¼×9½. Price: 1, 850 fr.

H. Piraux is an electrical engineer in charge of technical courses at S. A. Philips.

This new dictionary contains over 20,000 words or expressions with their French translation, often the popular or slang translation in addition to the proper one. It is devoted to electrical engineering and the parent techniques of electronics, radio, television, acoustics, optics, lighting, movie, telegraphy, telephony, nucleonics. As far as possible standardized words are used, of the Comité Electro-technique Français, the American Standards Association, IRE, and the British Standards Institution. There are about fifty measure conversion drawings giving length, width, volume, capacity, weight, pressure, energy, strength, temperature, and photometric and caloric measure tables.

Faster than Thought edited by B. V. Bowden

To be published by Sir Isaac Pitman & Sons, Ltd., Parker St., Kingsway, London WC2, England. 337 pages+2-page index+73-page appendices and glossary+xix pages. 18 figures. Size: 6×9.

B. V. Bowden is an engineer with Ferranti, Ltd., Manchester England.

We are accustomed to seeing pictures of sleekly streamlined modern electronic computers with similarly endowed, female operators poised at the controls. It is surprising then to find a book on these machines starting off with a handsome, old-fashioned portrait of a nineteenth-century lady mathematician. The reader will find many more surprises; for the editor, who wrote a good part of the volume himself, displays a wit and a literary skill most uncommon in current technical literature. Indeed, one of the shortcomings of the book is that not all the other contributors to this "Symposium on Digital Computing Machines" share Dr. Bowden's gift of exposition.

Ferranti, Ltd., is the first firm in England to produce a large-scale electronic computer commercially. The Ferranti computer is a redesigned version of the computer at the University of Manchester which it now replaces, so that the terms Manchester and Ferranti have almost become synonymous among computer people. This is, however, only one of several important computer developments in England, and Bowden's aim was to introduce the reader to Britain's accomplishments in this new field, and thereby to erect a monument to British ingenuity and skill. This purpose is frankly stated, and one cannot quarrel with it. The British have pioneered in many phases of automatic computing. An Englishman, Charles Babbage, over a hundred years ago foresaw most of the basic principles on which present-day computers are based. At a time when several groups in the U. S. drew plans for electronic computers using the latest stored-program techniques, and machines still largely on paper received much publicity, the computer group at Cambridge University quietly finished their own machine of this type, the EDSAC, ahead of everyone else. The Manchester machine was the first to use electrostatic storage. In general, Britain's economic plight forced the British computer designers to make a little go a long way, and they pioneered the use of clever programs to replace expensive hardware. On the theory that Americans know how to toot their own horns, our accomplishments are barely mentioned outside of one short chapter.

Some readers might be irked by such provincialism, but Bowden's book is a real contribution to computer literature on either

Books

side of the Atlantic. Its scope is quite extensive. Its three parts cover the principles, design, and applications of digital computers. Part 1 starts with a brief history of computation (with a side trip into racehorse breeding). and goes on to describe the circuit components, organization, construction, maintenance, and programming of a typical machine (the Manchester-Ferranti). Part 2 consists of eight chapters describing most of the major computer projects in England, each computer being discussed by engineers from that project. In Part 3 there are eleven chapters on the application of computers to such diverse subjects as logical problems, crystallography, meteorology, engineering calculations, government and business problems, and—who could resist—games. Each of these chapters is written by an authority in the particular field. The final chapter is devoted to "Thought and Machine Processes."

This is a most ambitious coverage, and nobody will be surprised to find that it is far from complete. In particular, one finds the early chapters on what goes into computers quite disappointing; the later chapters on the complete machines and their applications, which occupy more than half of the book, are generally much better written. In his zeal to philosophize on computers, Bowden has failed to lay an adequate technical foundation for the later chapters. Readers who know the technical material will probably find it elementary, whereas those who do not know it—those who would most profit from an elementary course on circuits and techniques—are advised by the editor to skip the circuit chapter. Had more care been exercised in explaining the basic operation of computer circuits, the book would have been much more valuable.

There are a number of misstatements and omissions in the circuit chapter. For instance, on page 33 there is an erroneous statement that the absence of a signal conveys no information in the Morse code (indeed, a poor example of a "two element" code). On page 40 is found the most unsatisfactory explanation: "Both the diode and the triode . . . can pass electric current in one direction only, and . . . (they) differ merely in the method for controlling that current." Is "direction" obvious in a 3-element tube? Nothing is said about amplification. The term "cathode follower" is used just once (p. 51), and an explanation of this important device seems to be missing completely. A delay element seen fleetingly in a diagram on page 53 goes unnoticed; in a different context it later (page 57) reappears apologetically as being "rather more complicated to understand." This turns out to be an understatement; the circuit and its brief explanation are so far above the technical level of the rest of the chapter as to be ridiculously out of place. The circuit chapter is not helped one bit by an unnecessary and lengthy excursion into Boolean algebra which is not used to explain a single circuit.

The remainder of Part 1 shows some improvement, but one wishes that the treatment of machine organization had been less verbal and more specific. More of the elementary block diagrams should have been used. The chapter on programming would have been much sounder if an honest-to-goodness program had been included with complete definitions of one set of instructions. The enterprising reader could then at least have figured out things for himself. There is, however, a lot of excellent material in the early chapters when the authors comment realistically on machines as a whole, on their idiosyncrasies and operating characteristics. They point out that more experience in programming and operating is needed, and that the design of computers has yet a long way to go.

It is hoped that in future editions the wide gap left between the treatment of computer elements and the discussion of computers as such will be closed. The present discussion, half-heartedly referring to the Manchester computer, is too vague. This reviewer would prefer a frank discussion of one machine even if it should take twice as much space as now.

The chapters in Part 2 on existing computer projects in England, by contrast, provide much valuable material, aptly illustrating the existence of many widely different methods of approach. It is interesting to note that only two of the eight British computers mentioned are decimal, and none have been designed specifically for commercial problems. This probably accounts for Bowden's failure to bring out the important fact that over half the American computers he describes are decimal, and that the UNIVAC moreover employs alphabetic coding. The significance of these features for large-scale data-handling does not yet seem to be appreciated in England. The lack of enthusiasm for magnetic tape reflected in Bowden's comments is also in sharp contrast to the attitude in the U. S.

The chapters on applications in Part 3 form a series of essays which, to many readers will be the most interesting part of the book. (Alas, there is one exception which the reader may discover for himself.) A wide variety of scientific, engineering, and commercial subjects are, of necessity, discussed rather briefly, but they leave the reader with a real appreciation of the usefulness of computers. He will hardly be able to come closer to the subject except by more detailed study of the fundamentals so sadly neglected in earlier chapters, or by actual contact with a computer.

This reviewer particularly liked Bowden's own comments on the complexity of business applications introduced by the conflict between logical machines and not-so-reasonable human beings. As they are now designed, computers are much better at mathematical equations than at calculating payroll deductions. "It always outrages pure mathematicians when they encounter commercial work for the first time to find how difficult it is," writes Bowden. And again:

"It is a tribute to the skill and the aesthetic sense of physicists and mathematicians that the equations which they have produced to describe natural phenomena are relatively simple and straightforward. Sir James Jeans went so far as to assert that the Almighty must be a mathematician Himself, or otherwise natural phenomena could not be described in such beautiful mathematical terms. This argument takes us rather out of our depth, but we hope we shall not be accused of impiety if we remark that it is clear that no such feeling for beauty inspires the Board of Inland Revenue."

The chapter on games gives examples of machine and man playing chess, checkers, and nim. They appear in this peculiarly retrogressive order. We are relieved to find that in the contest of machine versus man, man is still ahead unless the machine has a sure bet as in nim. But Bowden jumps with particular relish, and with some verbosity we fear, into the debate on whether machines can think. His position is somewhat different from that of other writers.* He admits that the answer depends entirely on the definition of thinking, a poorly understood subject at best. Bowden, it seems, would prefer to include in the definition some of the better-understood and simpler processes involved in clerical judgment; otherwise, "it will be hard to exclude the performance of the machine and admit that the ordinary man ever thinks at all." Surely, no such offense was intended by the Loyal Opposition.

We must also take note of the Appendix which contains a most interesting contemporary account of Babbage's Analytic Engine with extensive notes by the Countess of Lovelace, the aforementioned lady mathematician. In devoting 70 pages to this out-of-print paper written in 1842, Bowden is performing a real service. It is indeed humbling to be reminded of how few can recognize the value of far-sighted ideas conceived by a genius ahead of his time—Lady Lovelace was among those few. Nevertheless, in his pre-occupation with scholarly historical research, Bowden appears to have overlooked the fact that there *are* some concepts in modern computers which Babbage forgot to mention, such as putting the instructions into the general "store."

If the reader expected a group of computer designers to write a badly needed, up-to-date text on computer engineering, he will be disappointed. Instead Bowden and his many collaborators (we apologize for not listing their names) have produced an interesting and timely commentary on the power and the foibles of present-day digital computers. Bowden's sense of humor his writing skill, and his many historical and literary references give this work a zest which may be unique among modern technical books. It makes good reading for anybody who is active in the computer field or who would like to know more about it. The reader may not learn from his book exactly what makes a computer tick, but he will discover in it many things that will tickle his imagination—and his ribs. This reviewer, at least, enjoyed himself.

W. Buchholz
IBM Engineering Laboratory
Poughkeepsie, N. Y.

---

* See, for example, M. V. Wilkes, pp. 1230–1234 of this issue.

Books

Principles of Color Photography by R. M. Evans, W. T. Hanson, Jr. and W. L. Brewer

Published (1953) by John Wiley & Sons, Inc., 440 Fourth Ave., New York 16, N. Y. 672 pages +25-page indexes +23-page bibliography +xi pages. 302 figures. Size: 5¾×9. $11.

R. M. Evans is director of Color Technology Division, W. T. Hanson, Jr. is color photography division head of the Research Laboratories, and W. L. Brewer is supervisor of the physical standards and services section of the Color Technology Division, all of Eastman Kodak Company.

It is likely that a poll of radio engineers would show photography, and in particular color photography, high on the list of their outside interests. This indeed is fitting, for Clerk Maxwell not only developed the theoretical background for electrical communication, but he also made the first demonstration of photography in colors. In recent years, the television engineer has learned that his professional task of producing better pictures can be improved if he makes use of the experience accumulated in the older field of photography. And, with the imminence of nation-wide television in color, little could be more timely than the appearance of Evans, Hanson, and Brewer's "Principles of Color Photography."

A little more than a decade ago (in 1942), Dr. C. E. K. Mees, a member of the same Laboratories as the present authors, published his monumental reference book, "The Theory of the Photographic Process." In its more restricted field, "Principles of Color Photography" is a similar presentation of current knowledge, present-day theories, and the limitations of available photographic processes. As such, it obviously will be of little interest to the casual reader. To the television engineer, interested in learning about color films and their intrinsic limitations, and about color reproduction in general, however, this book will prove a valuable source of information. This, even though there is a specific disclaimer of knowledge of any royal road to the production of the "best" color picture, and it is pointed out that colorimetric principles serve only as a starting point in the quest for such a picture. These authors have been successful in bringing together in one book all of the varied material pertinent to the fundamental study of color photography. Following a review of the response of the eye under the simple conditions of colorimetry, color specification and color measurement are discussed. After this presentation of fundamentals, the problems of viewing an original scene and a photograph of it are introduced by examining the several visual phenomena which make such viewing conditions different from the conditions of colorimetry. Building again from a study of the fundamentals of the photographic process, the authors treat the mechanisms for producing and measuring colored images. By idealizing both the visual process and the photographic process, sufficiently simple relations are obtained to permit study of the production of color photographs, and of duplicating or of copying such photographs.

One would hardly expect an all-inclusive test of this sort to be a presentation of much new material. As the presence of an extended bibliography and as frequent reference to it indicates, this book is intended to be just what it is—an orderly presentation of the facts and principles known to underlie color photography. However, the reader should be warned that this is not the book for casual reference; it must be read, and reread, with care if its full scope is to be appreciated.

This book is remarkably free of mechanical errors for a first edition. The only one which troubled this reviewer was the omission of parentheses from equation (15.4*d*) on page 560. However, he was disappointed that a modern book on this subject does not contain a single color plate.

W. T. WINTRINGHAM
Bell Telephone Laboratories, Inc.
Murray Hill, N. J.

Filter Design Data for Communication Engineers by J. H. Mole

Published by John Wiley & Sons, Inc., 440 Fourth Ave., New York 16, N. Y., 246 pages +4-page index +xvi pages. 127 figures, and charts, 56 tables. Size: 9¾×6. $7.50.

As implied by its title, this book is principally a collection of tables, curves, and formulas useful in the design of wave filters, and the accompanying text is reduced to the minimum necessary to an understanding of the design procedure.

The book is concerned almost exclusively with the design of filters on the Zobel image-attenuation basis, but within these limits the design information is extensive and detailed. The m values required to give Tchebycheff behavior in the attenuation band are given for a large number of multiple-section filters for the entire range of possible characteristics so that a complete filter can be designed with a minimum of effort to meet given requirements on image attenuation.

The limitation of the method is that the information is not directly applicable to meet given requirements on insertion loss. Unfortunately the insertion loss is usually the quantity with which the design engineer is most directly concerned, and the values of m required to give Tchebycheff behavior of the insertion loss may differ considerably from those for attenuation constant, particularly for the simpler filter types which are most frequently used. Although formulas are given for the reflection and interaction losses, which can be combined with the image attenuation to obtain the insertion-loss, the correction is still too difficult to permit the optimum design on an insertion loss basis to be obtained with a reasonable amount of effort.

A final chapter in the book discusses Tchebycheff behavior of pass-band loss, but this is restricted to simple half-section and full-section filters and to two coupled circuits, for which algebraic expressions for the insertion-loss can be written down readily. For the more complicated filters discussions of behavior in the pass band is restricted to impedance matching, and here the designs to give Tchebycheff insertion loss are not considered.

In spite of these limitations the book will prove useful to engineers concerned with filter design until data based on insertion-loss methods become more generally available.

W. N. TUTTLE
General Radio Company
Cambridge, Mass.

Teamwork in Research edited by G. P. Bush and L. H. Hattery

Published (1953) by the American University Press, 1901 F Street, N.W. Washington 6, D. C. 186 pages +4-page index +xii pages. 5 figures. 6×9. $4.00.

George P. Bush is associate professor of public administration at the American University. Lowell H. Hattery is associate professor of political science and public administration at the University.

This volume is adapted from the Proceedings of the Third Institute on Administration of Scientific Research and Development held in Washington, D. C. by the American University with the co-operation of the National Research Council and the American Association for the Advancement of Science. The exact date of the meeting is not given. By careful planning of the original order of presentation and follow through on skillful editorship, the authors have highlighted today's "teamwork" problems. Excellent continuity is preserved and the focusing of the reader's attention on the central theme is accomplished with only gentle guidance and minimum of repetition in its 186 pages.

The book is obviously intended as a permanent record for those attending the Institute meeting as well as for reference by advanced students and executives interested in the growth of "team" action in our scientific organizations engaged in some form or another of "research." It is not however the final comprehensive authority on the subject nor is it so intended. It is more the presentation of what is happening right now.

The individual authors have each achieved eminent recognition in their specialties and their remarks are each phrased in a dynamic interesting manner. Quite often there is agreement on basic definitions of such matters as "research, development." Although at all times there is a lively commentary expressing positive pronouncements indicating that "teamwork" will not result of itself, but rather must be *worked* on.

In general, one cannot help but conclude from this volume that the grouping of specialists into "teams" has the tendency to mask the possible contribution of the individual. This, of itself, is not necessarily detrimental, but rather is the outgrowth of the "bigness" aspect of organized science today. One should take for granted however, that we are all seeking the most efficient use of manpower and associated resources and it certainly appears that the "team" approach enables greater *mass* effort to be placed on projects and ultimately produce *faster* answers.

RALPH I. COLE
Melpar, Inc.
Alexandria, Va.

Mass Spectroscopy in Physics Research—National Bureau of Standards Circular 522

Published (1953) by the U. S. Department of Commerce, Supt. Documents, U. S. Gov't Printing Office, Washington 25, D. C. 273 pages+vi pages. 177 figures. 5¾×9. $1.75.

Proceedings of the NBS Semicentennial Symposium on Mass Spectroscopy in Physics Research held at the NBS on September 6, 7, and 8, 1951.

Since the initial work by F. W. Aston in England and A. J. Dempster in this country at the end of World War I the field of mass spectroscopy has greatly enlarged and it has yielded important contributions to nuclear science. Both the expansion of the field and the magnitude of its importance are underlined by the 36 papers bound together in this volume. These papers were given in September of 1951 at a symposium held at the National Bureau of Standards. Leading mass spectroscopists from all over the world attended the meeting. Their discussions, reproduced in this well-illustrated book, range from basic principles (J. Mattauch, A. O. C. Nier, H. Ewald and K. T. Bainbridge) to precision measurements of atomic masses and descriptions of new mass analysis instruments. Largely of interest to nuclear physicists, the book will also be of value to engineers interested in ion optics.

R. E. Lapp
Nuclear Science Service
Washington, D. C.

Wave Propagation in Periodic Structures by Leon Brillouin

Published (1953) by Dover Publications, Inc., 1780 Broadway, New York, N. Y. 239 pages+7-page index+8-page appendix+xii pages. 131 figures. 5⅜×8. Paperbound: $1.75, clothbound: $3.50.

L. Brilluoin is a member of the Watson Laboratory staff, International Business Machines, New York, N. Y.

This is the second edition of a work originally published by the McGraw-Hill Book Company, Inc. in 1946. It is printed without change from the original plates except for a few corrections. An eight-page appendix has been added, however, that discusses recently published work relating to waves in periodic structures. These examples of the applicability of analytic methods presented in the book include the analysis of waveguide slow-wave structures, artificial dielectrics, magnetrons, and semi-conductors. In addition, several points in the text are clarified by the appendix. For example, a proof of an important theorem on crystal-lattice zone theory has been added, thus placing a previously intuitive rule on a rigorous basis.

Dr. Brillouin's book establishes the close similarity of behavior of the various types of waves in various kinds of media. Some of the subjects receiving attention are elastic waves on mechanical periodic structures, electromagnetic waves from radio through X-ray wavelengths in crystals, electric waves in filters, and free electrons in metals. It is shown that such concepts as phase velocity, group velocity, characteristics impedance, pass-bands, and stop-bands occur in all cases. The theory of wave propagation in generalized one-, two-, and three-dimensional lattices is developed, and mathematical tools such as matrices and the solutions of Mathieu's equation are introduced.

This book has been greatly appreciated by engineers and physicists, and will certainly continue to be in the future. Its greatest value has probably been in suggesting to the reader new concepts and analytical techniques applicable to research. The numerous illustrative examples greatly aid the reader's comprehension of the principles introduced.

It must be pointed out, however, that the book is not a source of directly usable design information, and hence would not be very useful to the average engineer. However, the more thoughtful research student and engineer will find it to be clearly written, stimulating, and frequently of immediate value to his work.

Seymour B. Cohn
Stanford Research Institute
Stanford, California

Radiotron Designer's Handbook—Fourth Edition. Edited by F. Langford-Smith

Published (1952) by Amalgamated Wireless Valve Company Pty. Ltd., 47 York St., Sydney, Australia; The Radio Corporation of America, Harrison, N. J.; and Iliffe & Sons Ltd., Dorset House, Stamford St., London, S.E.I., England, under the title of "Radio Designer's Handbook." American edition 1423 pages +51-page index +8-page supplement+xl pages. 956 figures. 73 tables. 5½"×8½". $7.00.

Mr. Langford-Smith is associated with the Amalgamated Wireless Valve Company of Sidney, Australia.

The fourth edition of this well-known reference book has been increased in size more than four times, and like its predecessors, it deals exclusively with the design of broadcast radio receivers and audio amplifiers. There is no specific information on television, radar, nor on industrial electronics; but the general principles and problems discussed in this book are equally applicable to these fields, including FM. The book is divided into seven parts (38 chapters) covering the following topics: (1) receiving tubes, (2) general theory and components, (3) audio frequencies, (4) radio frequencies, (5) power supply, (6) complete receiver, and (7) technical data.

Part (1) contains useful information on the characteristics and testing of receiving tubes, including perveance, negative-grid load lines, suppressor characteristics of pentodes, drift, tolerance, rf interelectrode insulation resistance, and so forth. Such information is not readily available elsewhere except in some manufacturer's literature.

The text is descriptive in general; but some of the passages, particularly in part (2), are so elementary that the only requirement of the reader is a knowledge of English. Such topics as the series and parallel combination of resistors, and a 48-page chapter on elementary mathematics are included. The authors could have safely assumed an elementary knowledge of radio and mathematics on the part of the reader, thereby making room for more useful information. For instance, a chapter on transistors in part (2) and another on the mechanical aspects of receiver design in part (6) would have been quite welcome. As it is, transistors are mentioned in about two lines. Otherwise, part (2) of this book contains much valuable information on the design of coils and transformers and a practical, detailed treatment of negative feedback.

The audio engineer will be happy to see more than 400 pages devoted to his field. This part alone is a book in itself on sound reproduction, covering everything from methods of testing pickups to the loudspeaker enclosure having the least diffraction troubles. Even the characteristics of currently available test records are given. There is a nonmathematical but exhaustive treatment of all kinds of distortion. Various measurement and test methods are explained, including the difference frequency method (CCIF) of measuring intermodulation distortion. However the author does not indicate that the difference tone should be chosen in the region of highest hearing sensitivity. There is little on magnetic recording.

Much descriptive information dealing with rf circuits appears in part (4); but there does not seem to be a uniform, concise and lucid exposition of such basic problems as what optimum coupling in the antenna circuit will yield the best signal-to-noise ratio. A few more equations, equivalent circuits, and curves would have been more helpful in pinning down such problems. Here, one misses Bond's and Zepler's books. AVC, AFC and frequency conversion are covered in great detail; but there is no information on balanced mixers inasmuch as these are not used in ordinary broadcast receivers.

In addition to AM broadcast and SW receiver design, FM receivers are briefly covered in part (6). Receiver test and measurement methods are generally based on the IRE and RTMA Standards. However, more information on noise and a circuit diagram and description of a noise factor meter would have been quite useful inasmuch as such test equipment is not readily available at present.

The book in general is clearly written, and the subject matter is expertly presented. However, some parts are in outline form with frequent cross references to other parts of the book. Location of the various headings would have been simplified if a decimal marking system had been used instead of a combination of letters and Arabic and Roman numbers. Some errors were noticed in the Australian edition; unfortunately these have not been corrected in the American version, which is a lithographic reproduction of the original volume. The American edition has an 8-page supplement giving additional references. Repetition is rather difficult to avoid in a book written by several authors and is noticeable particularly in parts (4) and (6).

Among the many good features of this book are the detailed and classified list of references at the end of each chapter and an unusually complete index. The references are to literature in the English language published throughout the world; but the terminology in the text is British.

It can be safely said that this is perhaps the most complete and up-to-date reference handbook on receiver and amplifier design. It is a veritable encyclopedia of existing knowledge on the subject. One finds here information which is not normally covered in textbooks nor readily available elsewhere. Therefore, the radio engineer in search of information will save time and effort if he refers to this book first. The authors, particularly Langford-Smith, deserve a great deal of praise and credit for presenting so much valuable design information in one volume.

Kerim Onder
Panoramic Radio Products, Inc.
Mount Vernon, N. Y.

Abstracts and References

Compiled by the Radio Research Organization of the Department of Scientific and Industrial Research, London, England, and Published by Arrangement with that Department and the *Wireless Engineer*, London, England

NOTE: The Institute of Radio Engineers does not have available copies of the publications mentioned in these pages, nor does it have reprints of the articles abstracted. Correspondence regarding these articles and requests for their procurement should be addressed to the individual publications, not to the IRE.

The index to the Abstracts and References published in the PROC. I.R.E., from February, 1952 through January, 1953, is published by the *Wireless Engineer* and may be purchased for $0.68 (including postage; from the Institute of Radio Engineers, 1 East 79th St., New York 21, N. Y. As supplies are limited, the publishers ask us to stress the need for early application for copies. Included with the Index is a selected list of journals scanned for abstracting, with publishers' addresses.

Acoustics and Audio Frequencies...... 1554
Antennas and Transmission Lines..... 1555
Circuits and Circuit Elements......... 1556
General Physics...................... 1558
Geophysical and Extraterrestrial Phenomena......................... 1559
Location and Aids to Navigation...... 1560
Materials and Subsidiary Techniques.. 1560
Mathematics.......................... 1562
Measurements and Test Gear......... 1562
Other Applications of Radio and Electronics............................ 1563
Propagation of Waves................ 1564
Reception............................ 1565
Stations and Communication Systems.. 1565
Subsidiary Apparatus................ 1566
Television and Phototelegraphy....... 1566
Transmission......................... 1567
Tubes and Thermionics............... 1567
Miscellaneous........................ 1568

The number in heavy type at the upper left of each Abstract is its Universal Decimal Classification number and is not to be confused with the Decimal Classification used by the United States National Bureau of Standards. The number in heavy type at the top right is the serial number of the Abstract. DC numbers marked with a dagger (†) must be regarded as provisional.

ACOUSTICS AND AUDIO FREQUENCIES

534:061.4 **2531**

Audio Developments—(*Wireless World*, vol. 59, pp. 301–305; July, 1953.) New products shown at the exhibitions organized by the Association of Public-Address Engineers and by the British Sound-Recording Association in London, May 1953, are described.

534.2:534.011 **2532**

An Acoustic Gyrator—W. E. Kock. (*Jour. Acous. Soc. Amer.*, vol. 25, p. 575; May, 1953.) See 1874 of July.

534.21:551.596 **2533**

A Review of the Influence of Meterological Conditions on Sound Propagation—U. Ingård. (*Jour. Acous. Soc. Amer.*, vol. 25, pp. 405–411; May 1953.) Discussion of the effects of the physical constitution of the atmosphere, temperature gradients, wind gradients, gustiness of wind, and ground absorption, on the propagation of sound waves. 36 references.

534.21-14 **2534**

Experimental Determination of the Damping of Pulsating Air Bubbles in Water—M. L. Exner and W. Hampe. (*Acustica*, vol. 3, pp. 67–72; 1953. In English.)

534.21-14:538.566 **2535**

Longitudinal Magneto-hydrodynamic Waves—N. S. Anderson. (*See* 2635.)

534.21-14:534.61 **2536**

On the Forces due to Acoustic Wave Motion in a Viscous Medium and their Use in the Measurement of Acoustic Intensity—F. E. Borgnis. (*Jour. Acous. Soc. Amer.*, vol. 25, pp. 546–548; May 1953.) The sum of the forces due to acoustic radiation and to the hydrodynamic flow associated with acoustic waves in viscous fluids is shown, under certain conditions, to be independent of the absorption in the fluid and also, within a considerable range, of the distance from the acoustic source. The source intensity of an acoustic beam can thus be measured without the use of thin screening films to eliminate the flow.

534.213.4 **2537**

The Attenuation of the Higher Modes of Acoustic Waves in a Rectangular Tube—E. A. G. Shaw. (*Acustica*, vol. 3. pp. 87–95; 1953.) Kirchhoff's theoretical treatment is applied to propagation between a pair of infinite parallel planes. The attenuation of (1, 0) waves in the range 2.4–3.0 kc has been measured accurately using a new probe-microphone technique. Under suitable conditions, attenuation is due almost entirely to thermal-conductivity and viscosity effects in the gas near the tube walls.

534.213.4-14 **2538**

The Dispersion of a Pulse Propagated through a Cylindrical Tube—D. V. Anderson and C. Barnes. (*Jour. Acous. Soc. Amer.*, vol. 24, pp. 525–528; May 1953.) The dispersion of an ultrasonic pulse transmitted through a thin-walled tube filled with water and immersed in a tank of water was investigated. The dispersion is in sufficiently close agreement with theory for the envelope of the dispersed pulse to be used for determining approximately the frequency spectrum of the initial pulse.

534.232:534.321.9 **2539**

The Ionophone applied in Ultrasonics—R. Miquel. (*Toute la Radio*, vol. 20, pp. 114–117; March/April 1953.) Report of an interview with S. Klein on the development of the ionophone (896 of 1952), particularly as an ultrasonic generator. Power output is comparable with that of a siren; frequencies of 3 mc have been reached in air. Distortion and response curves in the AF range are shown.

534.24/.25+538.566.2 **2540**

Total Reflection of Waves from a Point Source—E. Gerjuoy. (*Commun. Pure Appl. Math.*, vol. 6, pp. 73–91; Feb. 1953.) An analysis is made of the reflection of a pulse of sound at a plane boundary between nonabsorbing media, the velocity of propagation being greater in the second than in the first medium. It is shown without approximation that a pulse is received in the first medium after a delay consistent with propagation along the boundary with the velocity appropriate to the second medium. The theory affords an explanation of the head wave observed in acoustic experiments. The method is applicable to the analysis of the reflection of em waves radiated from a vertical dipole.

534.24(26) **2541**

The Scattering of Sound from the Sea Surface—C. Eckart. (*Jour. Acous. Soc. Amer.*, vol. 25, pp. 566–570; May 1953.) A theoretical analysis of the problem.

534.321.9-14:534.614 **2542**

An Acoustic Interferometer for High Fluid Pressure—H. D. Parbrook. (*Acustica*, vol. 3, pp. 49–54; 1953. In English.) Apparatus used for investigating ultrasonic propagation in fluids at critical pressure (Parbrook and Richardson, 3310 of 1952) is described. The quartz crystal transducer operates at pressures up to 270 ATM and in the temperature range 0–80°C. The effectiveness of different types of crystal holder is discussed.

534.321.9-14:534.612 **2543**

The Dependence of Sound Intensity at the Source on the Coefficient of Absorption in Liquids—S. Parthasarathy, S. S. Chari and D. Srinivasan. (*Z. Phys.*, vol. 134, pp. 408–412; March 25, 1953.) From measurements of radiation pressure, the intensity at the surface of a quartz-crystal radiator immersed in various organic liquids was determined for frequencies of 5 and 15 mc. The intensity was not found to be inversely proportional to the acoustic impedance, as expected on theoretical grounds. At 5 mc the intensity was proportional to the coefficient of absorption in 15 out of 19 liquids tested. At 15 mc no relation between absorption coefficient and intensity could be established.

534.612.4 **2544**

The Reciprocity Calibration of Capacitor Microphones—W. Holle and G. Latzel. (*Funk u. Ton*, vol. 7, pp. 109–123; March 1953.) Discussion of the application of the reciprocity principle to free-field calibration, corresponding to the conditions in which the microphone will later be used. By introducing a frequency-dependent voltage divider between the transmitting microphone and its amplifier, measurement of the capacitance of the reversible transducer and the frequency is not required. The frequency-response curve of the microphone is directly given by addition or subtraction of two curves obtained with a frequency-sweep recorder.

534.64 **2545**

Measurement of Acoustic Impedance by a Resonance Method—M. Ferrero and G. G. Sacerdote. (*Alta Frequenza*, vol. 22, pp. 3–16; Feb. 1953.) The theory of the method described by Harris (3310 of 1948) is discussed and some experimental results obtained by this method are reported.

534.76 **2546**

Stereoaudition—H. Kietz. (*Acustica*, vol. 3, pp. 73–86; 1953. In German.) Discussion, based on experimental results, of binaural hearing processes by which the direction and distance of a sound source may be estimated. 80 references.

534.845:551.575 **2547**

The Absorption of Sound in Suspensions

and Emulsions: Part 1—Water Fog Fog in Air—P. S. Epstein and R. R. Carhart. (*Jour. Acoust. Soc. Amer.*, vol. 25, pp. 553–565; May 1953.) The analysis presented is concerned with the effect of fluid spheres in a fluid medium. Viscosity and thermal conduction are both taken into account in the solution of the diffraction problem. The reduction of the general results to explicit formulas for attenuation is restricted to the case of liquid drops suspended in gases. Numerical calculations for fog in air are in satisfactory agreement with measurements made by Knudsen et al (614 of 1949).

534.845.1/.2 2548

The Coefficient of Sound Absorption as a Function of the Angle of Incidence of the Sound—F. K. Schroder. (*Acustica*, vol. 3, pp. 54–66; 1953. In German.) The absorption of porous material and of different forms of resonant absorber were investigated, using a pulse technique in a chamber specially designed to simulate two-dimensional space. With porous materials, results are in good agreement with theory; for resonant systems agreement is only qualitative. The absorption factor for partitioned cells is unexpectedly high in the frequency region above resonance and increases greatly with increasing angle of incidence, especially when the damping factor of the cavities is low. Energy losses depend largely on the manner of mounting in the case of facings and vibrating coils. Wedge arrangements show increased reflection towards grazing incidence.

534.851:621.317.35:621.3.018.78 2549

Distortion in Phonograph Reproduction—H. E. Roys (*See 2736.*)

621.395.625.2 2550

Binaural Disc Recording—E. Cook. (*Jour. Audio. Eng. Soc.*, vol. 1, pp. 1–3; Jan. 1953.) A description is given of the two-band method of binaural recording, which is completely compatible with ordinary disk recording; the two styli are spaced 1 11/16 inches apart on a 12-inch disk. Radial play-back error is discussed, and testing and alignment methods are indicated.

621.395.625.3 2551

Magnetic Sound-Recording Equipment—D. A. Snel. (*Philips Tech. Rev.*, vol. 14, pp. 181–190; Jan. 1953.) The general principles of sound recording on magnetic tape are outlined, the required magnetic and mechanical properties of the tape are discussed, and a general description is given of a recorder suitable for use in broadcasting studios and also of a portable recorder, with details of the unit containing the erasing, recording and reproducing heads.

621.395.625.3 2552

Methods of Measuring Surface Induction of Magnetic Tape—J. D. Bick. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 4–9; Jan. 1953.—*Jour Soc. Mot. Pict. Telev. Engrs.*, vol. 60, pp. 516–525; April 1953.) Two methods of measuring the recorded signal are described, in both of which the output from the recorded tape is measured with a calibrated reproducer. One method makes use of a narrow-gap head and the other of a head with a gap wide compared with the sound wavelength (Axon, 2121 of 1950). Frequency characteristics obtained by the two methods are compared.

621.395.625.3 2553

A New Professional Magnetic Recording Tape—E. Schmidt. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 10–16; Jan. 1953.) Production methods are described and performance figures given for tapes with bases of (a) standard 0.0015-inch cellulose acetate and (b) 0.001-inch mylar A.

621.395.625.3 2554

The Reproduction of Signals recorded on Magnetic Tape—E. D. Daniel and P. E. Axon. (*Proc. IEE*, Part III, vol. 100, pp. 157–167; May 1953.) The conventional analysis of the action of the ring type of reproducing head is re-examined, and experiments are described which demonstrate divergences between theoretical and practical results. The action of a single loop as a reproducer is analyzed. Experiments check the theory. Common faults of reproducing heads are discussed and the practical aspects of standardization are considered.

621.395.625.3 2555

The Influence of Some Head and Tape Constants on the Signal recorded on a Magnetic Tape—E. D. Daniel. (*Proc. IEE*, Part III, vol. 100, pp. 168–175; May 1953.) With recording heads of conventional design the distribution of magnetization through the thickness of the magnetic material may be markedly nonuniform, the amount of the nonuniformity depending on the high-frequency bias setting. Analysis of this effect affords an explanation of certain aspects of recording performance, including the anomalous loss of HF response when using large values of HF bias. The effect of self-demagnetization on the recording characteristic of tape is also discussed.

ANTENNAS AND TRANSMISSION LINES

621.315.21:621.392.21 2556

Determination of the Primary Parameters of Uniform [cable] Circuits—P. M. Prache. (*Câbles & Trans.* (*Paris*), vol. 7, pp. 89–96; April 1953.) Rigorous formulas are given for the required parameters, and also approximate formulas which are applicable when the loss angle of the circuit is small or when the circuit is short.

621.315.212:621.317.336 2557

Reflections in a Coaxial Cable due to Impedance Irregularities—G. Fuchs. (*Câbles & Trans.* (*Paris*), vol. 7, pp. 122–141; April 1953.) Translation. See 3495 of 1952.

621.315.212:621.317.343 2558

Determination of the Local and Mean Characteristic Impedance of Coaxial Cables by means of the Unit-Step Signal—G. Comte and A. Ponthus. (*See 2732.*)

621.315.212:621.392.2 2559

Transmission Parameters of a [cable] Amplification Section—R. Roch and J. A. Ville. (*Câbles & Trans.* (*Paris*), vol. 7, pp. 159–168; April 1953.) The quadripole formed by a length of cable can be characterized by five parameters, the three usual parameters of attenuation and input and output image impedances, and two new parameters: the image impedances of short sections at the two ends. Making use of these five parameters, methods of analysis previously described (Ville, 3374 of 1952) are applied to a quadripole chain representing a length of cable between two amplifiers. From the various parameters of the constituent sections, those of the whole length are deduced. The formula for the attenuation takes account of all the physical factors concerned, such as the reflections at the junctions of the various sections, and also double reflections.

621.392 2560

Heaviside's Condition for Distortionless Transmission—E. Astuni. (*Alta Frequenza*, vol. 22, pp. 37–39; Feb. 1953) The relations required between the parameters of a transmission line to provide distortionless transmission are derived by a simple method starting from consideration of an ideal line with zero inductance and capacitance.

621.392 2561

Heaviside, Vaschy, Pupin and Some Others—P. Lombardi. (*Alta Frequenza*, vol. 22, pp. 39–43; Feb. 1953.) Comment on 2560 above.

621.392+621.315.212].018.44 2562

Transmission Properties of Laminated Clogston-Type Conductors—E. F. Vaage. (*Bell Sys. Tech. Jour.*, vol. 32, pp. 695–713; May 1953.) The laminated transmission lines described by Clogston (2908 of 1951) are discussed and compared with ordinary coaxial cable. Approximate formulas are derived for the equivalent inductance, capacitance and resistance, and expressions are obtained for the attenuation, phase constant and propagation velocity, using conventional transmission-line theory. The results are compared with those obtained using the rigorous formulas developed by Morgan (25 of January and 618 of March).

621.392.26 2563

Calculation of the Excitation of Waveguides—L. S. Benenson. (*Zh. Tekh. Fiz.*, vol. 22, pp. 559–578; April 1952.) The excitation of a waveguide loaded at the ends is discussed and the amplitudes of voltages at slots are calculated. The case of a slot cut along the middle line of the wider wall of a rectangular waveguide is considered separately, and it is shown that it can be excited by a reactive vibrator, i.e., a vibrator short-circuited by the waveguide wall. The coupling of two rectangular waveguides by means of a longitudinal and a transverse slot cut in the shape of a cross is examined. The discussion is illustrated by experimental data.

621.392.26 2564

Excitation of a Circular Waveguide—G. T. Markov. (*Zh. Tekh. Fiz.*, vol. 22, pp. 747–758; April 1952.) A solution is obtained of a vectorial inhomogeneous wave equation by conversion to an analytical form referred to a cylindrical system of coordinates; the electric and magnetic fields due to external electric currents distributed in a uniform space are determined. The solution is used for considering the external and internal excitation of a perfectly conducting, infinitely long cylindrical waveguide. A number of particular problems, such as the diffraction of waves near the waveguide, operation of metal antennas on and near its surface, and the effect of slots in the surface, are discussed.

621.392.26 2565

The Susceptance of a Circular Obstacle to an Incident Dominant Circular-Electric Wave—L. S. Sheingold. (*Jour. Appl. Phys.*, vol. 24, pp. 414–422; April 1953.) A variational method is applied to determine the susceptance of a thin obstacle in a uniform round waveguide with an incident TE_{01} wave. The formulas obtained give results in good agreement with experimental values. Curves of normalized susceptance as a function of aperture, guide wavlength and free-space wavelength are included.

621.392.26 2566

The Slotted Diaphragm in Waveguides with Rectangular Cross Section—R. Müller. (*Z. Angew. Phys.*, vol. 5, pp. 142–148; April 1953.) Continuation of work noted in 1583 of June. The reflecting power of a symmetrically placed slit for an H_{10} wave is calculated as a function of wave number and slit width. For the case of a wide slit, the previously derived Fredholm integral equation is used; for the case of a narrow slit, a further integral equation is developed. By suitably transforming these equations they can be solved by a recurrence method details of which are given.

621.392.26:621.316.727.018.424 2567

A Wide-Band Waveguide Phase-Shifter—G. J. Halford, (*Proc. IEE*, Part III, vol. 100, pp. 117–124; May 1953.) Phase-shifters consisting of long slabs of dielectric, some with stepped ends, are discussed. For 3×1.5 inch waveguide, a cross section of 1×0.5 inch was adopted for the distrene used, which is supported on rods parellal eo the wider side of the waveguide, motion along the rods giving phase-shifts up to a maximum of 180°. Design theory is given for slabs with linear-taper quadratic-taper and stepped ends. Performance figures are given for four S-band models of the latter type with bandwidths of 10–25%.

621.396.67 2568

Distribution of Current and Voltage in Cylindrical, Ellipsoidal and Conical Aerials—O. Zinke. (*Onde Élect.*, vol. 33, pp. 107–117; Feb. 1953.) See 2437 of 1952.

621.396.67.011.21 2569

Mutual Impedance of Two Thin Straight Aerials, Parallel or with Directions Intersecting, carrying Harmonic Currents—F. Babin. (*Ann. Télécommun.*, vol. 8, pp. 145–148; April 1953.) Harmonic currents are defined as of the form $Ce^{jKz}+C'e^{jKz}$, where $K=2\pi/\lambda$, C and C' are complex coefficients, z is measured along the antenna, and λ is the wavelength in air and on the antenna. A general method is given for calculating the field and also the mutual impednace of wire antennas (a) parallel, (b) concurrent.

621.396.677 2570

The Field Radiated by a Ring quasi-Array of an Infinite Number of Tangential or Radial Dipoles—H. L. Knudsen. (Proc. I.R.E., vol. 41, pp. 781–789; July 1953.) The term "quasi-array" is used rather than "array" because with a tangential or radial arrangement of the elements they are not identically oriented. An analysis is made of the field due to such a system of an infinite number of dipoles carrying currents of the same amplitude but with phase varying uniformly round the ring. The gain of the system increases with the total change of phase round the ring, tending in the limit to the condition of "supergain." An approximate expression is derived for the minimum practical value of the ring radius for a given phase change.

621.396.677 2571

The Optimum Linear Array for a Single Main Beam—D. R. Rhodes. (Proc. I.R.E., vol. 41, pp. 793–794; July, 1953.) A method is indicated for determining current distribution and element spacing for an antenna array so as to obtain a single-beam endfire radiation pattern with minimum beam width for a given side-lobe level.

621.396.677 2572

A Note on the Circular Dielectric-Disk Antenna—E. M. T. Jones and R. A. Folsom, Jr. (Proc. I.R.E. vol. 41, p. 798; July 1953.) Brief discussion of an antenna similar to that noted in 2442 of 1952 (Jones).

621.396.677.1:523.72:621.396.822 2573

A High-Resolution Aerial for Radio Astronomy—W. N. Christiansen. (*Nature* (*London*) vol. 171, pp. 831–833; May 9, 1953.) An antenna constructed near Sydney, for scanning the sun, is described; it operates on a wavelength of 21 cm. The system consists of 32 paraboloids, each 6 feet in diameter, mounted on individual axes and arranged at equal distances along a 700 foot roughly east-west line. A family of beams with angular separation of 1.7° is produced; the earth's rotation causes these beams to sweep across the solar disk in succession. The antennas are connected by a branch 2-wire-line system to a receiver with a continuously recording milliammeter connected to its output. Peaks on the records indicate area of enhanced brightness on the solar disk; these are found to lie above sunspot groups or close to places previously occupied by sunspots. Use of the records to study the angular distribution of emission and time variations of emission from these areas is discussed.

CIRCUITS AND CIRCUIT ELEMENTS

534.13 2574

Diffraction Patterns for Solid Delay Lines—R. A. Mapleton. (*Jour. Acous. Soc. Amer.*, vol. 25, pp. 516–524; May 1953.) Solutions of the vector equation of equilibrium for an isotropic solid are presented for the special case of loss-free sine waves. Examples are considered in which the distribution of a single stress component is selected to simulate the stress produced by a HF quartz crystal.

621.3.011.6 2575

Extension of the Concept of the Time Constant—F. Nechleba. (*Electrotech. Z.*, *Edn. A*, vol. 74, pp. 98–101; Feb. 11, 1953.) Examples of the application of a general expression for time constant

$$T=[1/(x_\infty-x_0)]\int_0^\infty(x_\infty-x)\,dt$$

are illustrated in cases where the function is not exponential.

621.3.012.11 2576

Geometrical Transformation of Impedance Diagrams—H. Briner and W. Graffunder. (*Telefunken Ztg.*, vol. 26, pp. 102–110; March 1953.) The limited impedance range of the normal circle-diagram representation of impedances is noted. A second type of circle diagram can be constructed in which all possible impedance values satisfying the required conditions lie within the unit circle; its construction by means of Riemann's number sphere is described.

621.314.2.029.4 2577

Consideration of Some Factors concerning the Use of Audio Transformers—W. E. Lehnert. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 105–110; Jan. 1953.) The effect on the frequency response of using source or load impedances different from the rated values is discussed. Methods of reducing distortion due to nonlinear core characteristics and of eliminating noise due to various causes are indicated. Methods of matching several impedances to a single one simultaneously are shown.

621.314.235.012.12 2578

The Input Impedance and Transimpedance of I.F. Transformers—H. H. van Abbe. (*Electronic Appl. Bull.*, vol. 13, pp. 178–200; Nov./Dec. 1952.) Formulas are derived for the conventional IF transformer consisting of two coupled circuits tuned to the same frequency. The relation between transimpedance and input-impedance variations and the form of the frequency response curve are investigated. The method of constructing polar diagrams is explained, and diagrams are shown for the two impedances for various values of the parameters; their usefulness in the study of feedback phenomena, particularly feedback from tube anode to grid, is indicated.

621.314.3†+621.318.435.3 2579

Dynamic Characteristics of Transductors, or Magnetic Amplifiers— W. Schmidt. (*Arch. Elekt. Übertragung*, vol. 7, pp. 249–255; May 1953.) Review of the physical characteristics of transductors with low-resistance control circuits and of the self-excitation type.

621.314.3† 2580

The Figure of Merit of Magnetic Amplifiers—J. T. Carleton and W. F. Horton. (*Elec. Eng.*, vol. 72, p. 229; March 1953.) Digest only.

621.314.3† 2581

Magnetic Amplifier with Reset Control—G. M. Attura. (*Electronics*, vol. 26, pp. 161–163; June 1953.)

621.314.7:621.392.5 2582

Transistor Negative-Impedance Converters—J. G. Linvill. (Proc. I.R.E., vol. 41, pp. 725–729; July 1953.) Improved converters of the general type described by Merrill (1323 of 1951) are obtained by using transistor circuits in place of the original tube circuits. The characteristics obtained are highly stable. Various practical circuits are illustrated and discussed and applications in telephone repeaters are described.

621.314.7:[621.396.645+621.318.57 2583

Symmetrical Properties of Transistors and their Applications—G. C. Sziklai. (Proc. I.R.E, vol. 41, pp. 717–724; July 1953.) Symmetry of one kind is found in the complementary characteristics of the *n-p-n* and *p-n-p* types of junction transistor; by using these two types in combination, reduction of the number of components and other circuit simplifications can be achieved, particularly in single-ended push-pull amplifiers. Symmetry of a second kind can be found in single transistors and is evidenced by interchangeability as regards operation of emitter and collector; use is made of this property in switching circuits, e.g., for clamping and modulation, and for a high-efficiency television deflection circuit.

621.318.43.042.4 2584

On the Magnetization of Toroids with One and Two Air-Gaps—F. F. Panesenkov. (*Zh. Tekh. Fiz.*, vol. 22, pp. 989–999; June 1952.) A method is proposed for calculating the leakage coefficient in the case of a toroid with one large air-gap, and an experimental formula is derived for determining the average leakage coefficient for the cases of toroids with one air-gap and with two diametrically opposite air-gaps.

621.392 2585

The Second Fundamental Theorem of Electrical Networks—C. Saltzer. (*Quart. Appl. Math.*, vol. 11, pp. 119–123; April 1953.) An independent proof is given of a theorem which states, for the Norton (nodal) representation, the relations previously proved by Ingram and Cramlet (435 of 1945) for the Thévenin (mesh representation. The nodal equations of Kron, a given by Le Corbeiller (1892 of 1950), are deduced by a method similar to that of Synge (347 of 1952). The relation between the nodal and mesh theorems is discussed.

621.392 2586

Network Transformations—L. Norde. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 137–139; Jan. 1953.) A method of finding an equivalent for a given network is outlined, a table of equivalent networks is presented, and examples of the use of the method are given.

621.392.4/.5 2587

The Solution of Passive Electrical Networks by means of Mathematical Trees—W. S. Percival. (*Proc. IEE*, Part III, vol. 100, pp. 143–150; May 1953.) A new method of solution for network problems is based on the properties of certain basic types of network termed "trees" and "2-trees." Linkage functions, defined in terms of sets of trees and 2-trees, obey laws analogous to those of Kirchhoff, so that relations involving voltages and currents can be expressed in terms of linkages. Results of the method are given in terms of admittances. See also 347 of 1952 (Synge).

621.392.43:621.396.67 2588

Design Procedures for Pi-Network Antenna Couplers—L. Storch. (Proc. I.R.E., vol. 41, pp. 790–793; July 1953.) Discussion on paper noted in 571 of 1950.

621.392.5 2589

Reciprocal Ladder Networks—J. B. Rudd. (*A.W.A. Tech. Rev.*, vol. 9, pp. 159–170; Jan. 1953.) The transfer impedance of a system comprising generator and load with ladder network interposed is unchanged if instead of the original network a "reciprocal" network is connected in reverse. The reciprocal network is derived from the original one by replacing series impedances by shunt impedances and vice versa, the product of the original and new impedances being in each case equal to the product of the generator and load impedances.

621.392.5 2590

Reactive T or Π Sections resolvable into Two Matched Half-Sections— R. Leroy. (*Câbles & Trans.* (*Paris*), vol. 7, pp. 156–158; April 1953.) Means are indicated for determining whether the resolution into half-sections with matched terminal impedances is possible.

621.392.5 2591

Study of an Electronic Antiresonant Circuit—P. Riéty. (*Ann. Télécommun.*, vol. 8, pp. 113–122; April, 1953.) Theory is given of a circuit which can either be used as a low-pass filter or as an antiresonant circuit. The operation of the circuit in the steady state in response to an applied sinusoidal voltage, and in the transient regime in response to a unit-step voltage, is analyzed. As an antiresonant circuit it is more selective than a double-T RC circuit. Its characteristics can be varied within wide limits and the values of the components can easily be calculated from the characteristics specified. Its high selectivity, independent of the cut-off frequency, makes it particularly suitable for use at very low frequencies.

621.392.5:621.396.611.35 2592

Resistive Bidirectional Coupler—L. Rosenthal. (Proc. I.R.E., vol., 41 pp. 799–800; July 1953.) A resistive T network is discussed which, when inserted between a source and a load, acts as a bidirectional coupler, providing voltages proportional respectively to the incident and reflected waves. The arrangement is applicable to measurement purposes, and is used e.g. in the wattmeter described by Ryder and McVat (2394 of August).

621.392.5:621.396.645 2593

Resistance-Capacitance Networks in Amplifier Design—E. D. Sisson. (*Jour. Audio. Eng. Soc.*, vol. 1, pp. 116–124; Jan. 1953.) Two types of RC network are distinguished, the first of which includes all networks with a simple series or shunt capacitor. This type only is considered. Frequency and phase characteristics are derived and reduced to simple graphical form. Impedance matching and loading effects are discussed. Typical equalizer and tone-control circuits are examined.

621.392.5:621.396.667 2594

Attenuation Equalizers—F. R. Bies (*Jour. Audio Eng. Soc.*, vol. 1, pp. 125–136; Jan. 1953.) The performance of various commonly used equalizer networks is discussed, and a chart method of computing their insertion loss is presented.

621.392.52 2595

Minimum Inductor or Capacitor Filters—W. Saraga. (*Wireless Eng.*, vol. 30, pp. 163–175; July 1953.) Known methods are surveyed and some new methods developed for designing equivalent filter networks having fewer inductors or capacitors than a given network. The particular transformation appropriate in a given case depends on whether the given filter is an image-parameter type which can be split into separate *m*-derived sections, or is of a more general character. The methods presented are based on the values of the network elements, without reference to impedance/frequency functions of the network as a whole. Two practical examples of application of the methods to band-pass filters are treated in detail.

621 392.52 2596

The Effects of Terminations and Dissipation on the Insertion Loss of Some Simple Ladder Filters—M. Strasberg. (Proc. I.R.E., vol. 41, pp. 777–780; June 1953.) By using special terminations, the selectivity of these filters can be improved and elements with relatively low values of Q can be used. Insertion-loss curves indicating the combined effects of terminations and of dissipation in the filter elements are presented in a form applicable to low-pass, high-pass and band-pass filters of several types.

621.392.52 2597

Theory of Antimetrical Lattice Filters—J. Oswald. (*Bull. Soc. Franç. Élect.*, vol. 3, pp. 116–124; March 1953.) The theory of a class of lattice filters with inverse image impedances is a counterpart of that for symmetrical filters. These filters comprise two reactances and their inverses; the frequencies at which the modulus of the reactances is equal to the characteristic impedance correspond to the poles and zeros of the reactances in the symmetrical case. Calculations relative to the construction of such filters are explained and typical examples are described. A high-ratio impedance transformation is attainable with narrow-band circuits. See also 959 of 1940 (Piloty).

621.392.52 2598

Optimum Nonlinear Filters—L. A. Zadeh. (*Jour. Appl. Phys.*, vol. 24, pp. 396–404; April 1953.) Theory of optimum nonlinear filters is based on the consideration of a sequence of classes of nonlinear filters, N_1, N_2, $N_3 \ldots$, such that each class in the sequence includes all the preceding classes, and also includes the class of linear filters. The characteristic function of the optimum filter within the class N_m is found to satisfy a linear integral equation of order $2m$. A detailed treatment of optimum filters of class N_1 is given, and methods of approximate realization of such filters in the form of nonlinear delay-line filters and power-series filters are indicated. The results are extended to the case of nonstationary time series.

621.392.54:621.392.26 2599

Construction and Calibration of an Inductive Attenuator—L. Resegotti. (*Alta Frequenza*, vol. 22, pp. 17–31; Feb. 1953.) A HF attenuator is described which makes use of the properties of a waveguide at frequencies far below cutoff. For a frequency of 18 mc the attenuation varies linearly to within 1%, between 20 and 120 db, with the distance between the source and the output coil. The attenuation can be calculated from the physical dimensions only.

621.396.6 2600

Novel Valve Circuits—J. P. Oehmichen (*Toute la Radio*, vol. 20, pp. 43–46 and 88–90; Feb./April 1953.) A review of tube circuits operated under unusual conditions in respect of bias, anode and screen voltages, and of input and coupling arrangements, as in pulse squaring and gating circuits and electrometer applications.

621.396.61 2601

A Note on Moving Poles in Nonlinear Oscillating Systems—W. B. Wrigley. (Proc. I.R.E., vol. 41, pp. 774–777; July 1953.) "Since poles of the complex immittance of a linear system represent the decrements and frequencies of rotating phasors in the linear time domain, it is suggested that a nonlinear system might be represented by moving poles whose instantaneous decrements and frequencies are associated with phasors rotating in the nonlinear or time-distorted phase space. This idea is applied to the analysis of a class of nonlinear oscillation generators of the second order which is described by the differential equation, $\ddot{X} - N_1(\dot{X}, X) = 0$."

621.396.611.1 2602

A Second Contribution to the Solution of the "Rukop Problem"—K. Steimel. (*Telefunken Ztg.*, vol. 26, pp. 73–76; March 1953.) Re-examination of the problem of the dynatron-driven series circuit and the arc-driven parallel circuit (1931 Abstracts, p. 92). Nyquist's stability criterion is applied to the equivalent circuit, and the necessary and sufficient conditions for excitation of oscillations are determined.

621.396.611.2:621.319.4 2603

Compensation of the Temperature Effect in *LC* Circuits by means of Negative-Coefficient Capacitors—P. A. Colavita. (*Rev. Telegr. Electronica* (Buenos Aires), vol. 41, pp. 199–203, 215; April 1953.) Compensation at a given frequency is obtained by connecting in parallel with a variable capacitor a series arrangement of a fixed negative-coefficient capacitor and a variable capacitor. The experimental method of adjustment is described. Frequency variation with temperature for uncompensated settings is studied.

621.396.615 2604

More on the RC Oscillator—W. J. Wray, Jr. (Proc. I.R.E., vol. 41, p. 801; July 1953.) Comment on 3512 of 1952 (Davidson).

621.396.615 2605

The Frequency Spectrum of a Pulled Oscillator—A. G. Simms. (Proc. I.R.E., vol. 41, p. 798; July 1953.) The conclusions reached by Buchanan (3043 of 1952) are presented in a simpler and more precise form.

621.396.615 2606

Blocking Oscillators—K. G. Beauchamp. (*Elec. Eng.*, vol. 25, pp. 239–243; June 1953.) The use of blocking oscillators as generators of voltage or current pulses, or of repetitive saw-tooth voltage or current wave forms, is examined in some detail, with a description of the mode of operation of the various circuits considered and discussion of the factors affecting their practical design.

621.396.615.12:621.316.726 2607

The Impulse-Governed Oscillator, a System for Frequency Stabilization—E. H. Hugenholtz. (*Philips Tech. Rev.*, vol. 14, pp. 130–140; Nov. 1952.) Detailed description. See 767 of 1951.

621.396.645 2608

Improved "Lock-In" Amplifier—H. L. Cox, Jr. (*Rev. Sci. Instr.*, vol. 24, pp. 307–308; April 1953.) A stable sinusoidal voltage drives a square-wave generator, whose output is applied to the anodes of a pair of diodes in phase opposition. The signal is applied to the diode cathodes in equal phase. The dc output voltage developed between the two cathodes is directly proportional to the signal and is largely independent of the input noise level, the value of the stable voltage, and the tube parameters.

621.396.645 2609

Constant-Current Operation of Power Amplifiers—H. T. Sterling and A. Sobel. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 16–21; Jan. 1953.) A Class-A$_2$ amplifier is discussed which is designed to be nearly independent of variations in tube characteristics. Cathode-follower drivers are used, together with balanced feedback and a separate feedback phase-inverter. See also 1635 of June.

621.396.645:621.3.018.78 2610

Distortion in Class-A Push-Pull Amplifiers S. Landesman. (*Alta Frequenza*, vol. 22, pp. 32–36; Feb. 1953.) The distortion is expressed in terms of the derivatives of the anode/grid characteristic at the operating point. The effect of the cathode resistance is to increase the distortion as compared with the effect due to the load resistance alone.

621.396.645:621.385.5 2611

Degenerative Pentode Equivalent Circuit—H. Stockman. (Proc. I.R.E., vol. 41, p. 801; July 1953.) Analysis and discussion, based on two forms of equivalent circuit, of a pentode arrangement with feedback via cathode-lead impedance.

621.396.645.018.424 2612

Distributed Amplifier Theory—D. V. Payne. (Proc. I.R.E., vol. 41, pp. 759–762; July 1953.) Matrix algebra is used to analyze operating conditions in the anode line. The manner in which the amplifier gain depends on grid- and anode-line terminations and propagation constants, number of tubes and grid driving voltage is indicated. Experimental results obtained with a six-tube amplifier provide general confirmation for the theory.

621.396.645.029.3 2613

Analysis of a Single-Ended Push-Pull

Audio Amplifier—Chai Yeh. (Proc. I.R.E., vol. 41, pp. 743–747; July 1953.) Analysis is given for the circuit described by Peterson and Sinclair (1250 of 1952). Linear tube characteristics and small signals are assumed. Some experimental results are reported.

621.396.645.029.3 2614

Bypass and Decoupling Circuits in Audio Design—L. S. Goodfriend. (*Jour. Audio Eng-Soc.*, vol. 1, pp. 111–116; Jan. 1953.) The amplifier equation is put into a form which expresses the gain for ideal conditions of perfect bypassing and no reactive elements, with separate terms taking account of the actual reactive effects. These terms are evaluated for the limiting conditions at the low and high ends of the frequency band, and the real and imaginary parts are separated. Design of triode and pentode circuits is considered.

621.396.645.029.3 2615

Audio-Frequency Input Circuits—W. B. Snow. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 87–94; Jan. 1953.) Careful design of input circuits is important, especially when the input level is low. Fundamental factors considered include signal/noise ratio of the source, optimum input impedance for resistive and reactive generators, noise in the amplifier tube, input-transformer and connecting-cable characteristics.

621.396.645.083.6 2616

A Differential Input Stage for Low-Frequency Amplifiers—V. H. Attree. (*Elec. Eng.*, vol. 25, pp. 260–261; June 1953.) An ac-coupled differential input stage is described in which the ratio of in-phase to anti-phase gain, i.e., the transmission factor, is theoretically infinite. In an actual circuit the measured value of the transmission factor was 10^4 at an in-phase signal level of 1.0V rms. The frequency range of 0.1 cps–20 kc is adequate for most applications.

621.396.645.35 2617

Cathode-Drift Compensation in D.C. Amplifiers—J. W. Rittenhouse. (*Elec. Eng.*, vol. 72, p. 299; April 1953.) Digest only. The Miller circuit has been found effective in compensating against cathode drift, but it has been assumed necessary to use a load resistance large enough to make the anode current of the output tube small compared with that of the other. Simple analysis is presented to show that this limitation is unnecessary; an improvement of the circuit based on this analysis is suggested.

621.396.615 2618

Vacuum Tube Oscillators [Book Review]—W. A. Edson. Publishers: Chapman & Hall, London. (*Wireless Eng.*, vol. 30, p. 183; July 1953.) Intended for senior and graduate students as well as for practicing electrical engineers; the subject is treated mainly from the point of view of design.

GENERAL PHYSICS

53.05:519.24 2619

Successive Differentiation of Experimental Curves, and Method of Smoothing—P. Vernotte. (*Compt. Rend. Acad. Sci.* (Paris), vol. 236, pp. 1737–1739; May 4, 1953.)

530.145:51 2620

Mathematical Aspects of the Quantum Theory of Fields: Part 5—Fields modified by Linear Homogeneous Forces—K. O. Friedrichs. (*Commun. Pure Appl. Math.*, vol. 6, pp. 1–72; Feb. 1953.) Part 4: 1290 of May.

530.145:517.51 2621

Dirac's Function and its Utilization in Mathematical Physics—S. Colombo. (*Ann. Télécommun.*, vol. 8, pp. 131–144; April 1953.)

534.1+538.56 2622

Some Exact Solutions in Nonlinear Oscillations—K. Munakata. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 383–391; July/Aug. 1952.) A rigorous analysis is made of forced oscillations of mechanical or electrical systems for certain cases which are specified by the condition that the forced oscillation has a wave form similar to that of the external force. The stability conditions are derived from Hill's equation, which can be solved exactly for the present cases.

535.33:538.569.4029.65 2623

One- to Two-Millimeter Wave Spectroscopy—W. C. King and W. Gordy. (*Phys. Rev.*, vol. 90, pp. 319–320; April 15, 1953.) Spectral lines have been measured at many positions between 1.37-mm and 2.3-mm wavelength, using similar technique to that previously described (Johnson *et al*, 1896 of 1952). Construction details of the new multiplier and detector used will be given elsewhere.

535.37 2624

The Mechanism of Phosphorescence in Crystal Phosphors—D. Curie. (*Phys. Rev.*, vol. 90, pp. 154–155; April 1, 1953.) A summary of the results of the investigations described elsewhere in greater detail (1643 of June).

535.42+534.26 2625

Infinite Matrices Associated with Diffraction by an Aperture—W. Magnus. (*Quart. Appl. Math.*, vol. 11, pp. 77–86; April 1953.) The results obtained by Levine and Schwinger (83 and 1897 of 1950) are discussed, and it is shown that the algebraic properties of the matrix used are such as to permit determination not only of the transmission coefficient but also of the distribution of field across the aperture.

537.122 2626

A Note on the Application of Schwinger's Variational Principle to Dirac's Equation of the Electron—H. E. Moses. (*Quart. Appl. Math.*, vol. 11, pp. 111–118; April 1953.)

537.311.33:[546.28+546.289 2627

Transistors: Theory and Application: Part 4—Transistor Action in Germanium and Silicon—A. Coblenz and H. L. Owens. (*Electronics*, vol. 26, pp. 166–171; June 1953.) A simple account of the physical structure and properties of Ge and Si crystals. Part 3: 2289 of August.

537.315 2628

Investigation of the Potential Barrier between Two Electrodes of the Same Metal with Different Applied Potentials—N. Nifontoff. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1538–1540; April 20, 1953.) A theoretical investigation of the barrier transparency and tunnel effect. Analysis leads to formulas which for limiting cases give the known results corresponding to a rectangular or triangular type of barrier.

537.315 2629

Some Properties of Potential Barriers—A. Blanc-Lapierre and N. Nifontoff. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1634–1636; April 27, 1953.) Matrices used in defining the wave function at the junction between different media are shown to be applicable for calculations relating to potential barriers of various forms.

537.525 2630

The Electrical Breakdown of Gases in Nonuniform Fields at Low Pressure—F. L. Jones and G. C. Williams. (*Proc. Phys. Soc.* (*London*), vol. 66, pp. 345–361; May 1, 1953.) Breakdown voltages between coaxial cylinders were investigated for air, H and He. The results obtained support the view that the same primary and secondary ionization processes are involved as for uniform fields.

537.534.71:537.534.8 2631

The Reflection Coefficient of Positive Lithium Ions striking a Metal Surface, and the Energy Spectrum of the Secondary Electrons—G. Couchet. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1862–1864; May 11, 1953.) Results obtained for targets of duralumin and nickel are shown graphically. See also 384 of February, for which the UDC number should be 537.534.8:621.385.833.

537.583:621.385.032.21 2632

A Survey of Present Knowledge of Thermionic Emitters—D. A. Wright. (*See* 2832.)

538.114 2633

The Zero-Point Susceptibility of a Linear Antiferromagnetic Atomic Chain—E. Ledinegg and P. Urban. (*Acta Phys. austriaca*, vol. 6, pp. 257–287; Jan. 1953.)

538.56:537.525 2634

Operation of the Penning Gauge—M. Bayet and G. Dumas. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1648–1650; April 27 1953.) Experiments were made to check results reported by Laffineur and Pecker (1139 of 1951) on the emission of HF waves from a gas discharge. A receiver tunable over the band 3–0.50 m and fixed-tuned receivers for 75, 10 and 3 cm were used. No radiation was detected on the last two wavelengths; on the other wavelengths continuous spectra were observed with a fairly sharp peak at a frequency less than half the gyromagnetic frequency. The effect of a component of electric field normal to th magnetic field is discussed.

538.566:534.21-14 2635

Longitudinal Magneto-hydrodynamic Waves—N. S. Anderson. (*Jour. Acous. Soc. Amer.*, vol. 25, pp. 529–532; May 1953.) Alfvén's theory indicates that the velocity of sound waves in a conducting fluid will be changed by application of a strong magnetic field. Theory of this effect is presented for a fluid with finite conductivity and is applied to predict effects that should be obtained in propagation of sound (a) in Hg in a very strong field, (b) in sea water under the influence of the geomagnetic field.

538.566:537.562 2636

Generalized Magneto-hydrodynamic Formulae—C. O. Hines. (*Proc. Camb. Phil. Soc.*, vol. 49, Part 2, pp. 299–307; April 1953.) The formulas of magneto-hydrodynamic theory are extended by the simpler methods of magneto-ionic theory, in which mean velocities and forces are used, and nonlinearities are avoided by a perturbation treatment. The results are applied to the case of plane-wave propagation in the direction of a primary magnetic field.

538.566:537.562 2637

Interaction of Microwaves propagated through a Gaseous Discharge Plasma—L. Goldstein, J. M. Anderson and G. L. Clark. (*Phys. Rev.*, vol. 90, pp. 151–152; April 1, 1953.) Experimental observations are reported on the interaction of 8.6-kmc and 9.4-kmc signals in discharge plasma produced in He, Ne, Ar, Kr, Xe and H gases over the pressure range 0.2–20 mm Hg, pulse excitation being used. The 8.6-kmc disturbing wave was pulse modulated, and the wanted cw, transmitted through the decaying plasma, was detected by means of a cavity resonator, the amplified envelope being displayed on a cro. Typical oscillograms, showing the modification of the envelope of the wanted wave due to the pulsed disturbing wave, are reproduced. When a magnetic field is applied, the interaction is observed at low signal levels for which no effect is found in the absence of the magnetic field. See also 914 of 1952 (Goldstein *et al*) and back reference.

538.691 2638

The Characteristics of an Electron Beam entering a Coaxial Magnetic Field—L. Brück. (*Telefunken Ztg.*, vol. 26, pp. 85–88; March 1953.) The effect of nonuniformity of the focusing field on the convergence of an electron beam is studied by considering a particular field configuration and calculating the path of an electron at the edge of the beam. The radius of the beam is plotted as a function of distance traveled in the transition zone, for different values of a parameter which is dependent on current density, accelerating voltage and length of the transition zone.

621.3.011.4 2639

Calculation of the Electrostatic Capacitance of a Conductor by the Method of Excess and Deficit: Application to the Case of the Cube—L. Daboni. (*Rend. Accad. naz. Lincei*, vol. 14, pp. 461–466; April 1953.) Using a method based on a theorem due to Fichera, the capacitance of a cube of side a is found to be between $0.654a$ and $0.676a$.

GEOPHYSICAL AND EXTRATERRESTRIAL PHENOMENA

523.72:621.396.822:621.396.677.1 2640

A High-Resolution Aerial for Radio Astronomy—W. N. Christiansen. (*See* 2573.)

523.746:550.385 2641

On Sunspots and Magnetic Storms—F. Moriyama. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 151–157; 1951.) Study of the correlation between active sunspots and geomagnetic storms shows that the effect of central-meridian passage of active sunspots on the occurrence of storms is more evident when the activity is defined by both the spot type and the magnetic character than by the spot type alone. This is particularly noticeable in the case of geomagnetic storms with gradual commencements.

523.746:550.386 2642

Control of Geomagnetic Activity by Sunspots—J. F. Denisse. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1856–1858; May 11, 1953.) Statistical analysis of the sunspots observed in 1948, 1949 and 1950 shows that as regards their effect on geomagnetic activity they can be divided into two distinct classes: (a) radio-emissive spots, the source of relatively dense corpuscular jets and accompanied by marked peaks of mean geomagnetic activity; (b) sunspots with no corpuscular or radio emission, causing a marked reduction of geomagnetic activity. In the case of many spots of this latter type, the geomagnetic activity returns quickly to normal 3 to 4 days after the spots pass the central meridian.

550.384/.386 2643

Proposals for the Statistical Treatment of Geomagnetic Micropulsations—O. Schneider. (*Arch. Met. A, Wien*, vol. 4, pp. 403–412; 1951.) A system of classification is suggested in which the magnitude, duration and regularity of the pulsation trains are assessed semiquantitatively.

550.385 2644

Some Characteristics of Magnetic Storms: Part 1—Magnetic Storm on August 3, 1949—N. Fukushima. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 85–97; 1951.) Analysis of data from many observatories all over the world.

550.385 2645

The Morphology of Geomagnetic Storms: an Extension of the Analysis of D_s, the Disturbance Local-Time Inequality—S. Chapman. (*Ann. Geofis.*, vol. 5, pp. 481–499; Oct. 1952. In English.)

550.385.001.11 2646

Further Notes on a New Theory of Magnetic Storm—Y. Kato. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 75–83; 1951.)

551.510.53:537.311.37:550.384.4 2647

A Suggestion for the Electric Conductivity of the Upper Atmosphere from an Analysis of Diurnal Variations of Terrestrial Magnetism: Part 2—M. Hasegawa and H. Maeda. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 167–178; 1951, and vol. 6, pp. 155–158; 1952.) Diurnal variations of the electric field and electrical conductivity of the upper atmosphere are deduced from the observed variations of the geomagnetic field.

551.510.53:551.594.51 2648

On the Auroral-Zone Current—T. Nagata. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 87–101; 1950.) Analysis of eleven examples of auroral-zone disturbance of the geomagnetic field in the Second International Polar Year indicates that the height of the zone currents may be 100 km or less, the current intensity for moderate magnetic disturbances being of the order of 400–800 A/km, a very large increase in the electron density of the D and E layers being thus indicated.

551.510.534 2649

The Mean Vertical Ozone Distribution resulting from the Photochemical Equilibrium, Turbulence and Currents of Air—H. K. Paetzold. (*Jour. Atmos. Terr. Phys.*, vol. 3, pp. 125–131; April 1953.)

551.510.535+523.74 2650

Ursigrams—(*URSI Inform. Bull.*, No. 77, pp. 31–39; Jan./Feb. 1953.) Abbreviated codes are given for European ursigrams, and modifications in the French ursigram transmissions are tabulated.

551.510.535 2651

The Continuous Layer Formation in the Atmosphere under the Influence of Solar Radiation—H. K. Kallmann. (*Phys. Rev.*, vol. 90, pp. 153–154; April 1, 1953.) The formation of ionized layers in the atmosphere under the influence of (a) a quiet sun, (b) a disturbed sun, is found possible in both cases if account is taken of the variation with height of (a) the dissociation of the molecular constituents, (b) the ionization of the different constituents at various altitudes. The expression "continuous layer formation" signifies continuous increase and decrease of the electron density with height throughout the ionosphere.

551.510.535 2652

Formation of the D Layer—K. Watanabe, F. Marmo and E. C. Y. Inn. (*Phys. Rev.*, vol. 90, pp. 155–156; April 1, 1953.) Measurements of absorption cross sections of various gases are described. The results favor the assumption that absorption of solar radiation by NO is largely responsible for the formation of the D layer.

551.510.535 2653

Determination of the Coefficient of Recombination in the Ionosphere—V. V. Somayajulu. (*Sci. & Cult.*, vol. 18, pp. 494–496; April 1953.) A simple method is suggested in which the recombination coefficient α is determined from night-time observations, in terms of the gyrofrequency, the mean observation frequency, and the time interval between the disappearance of the ordinary- and extraordinary-ray echoes. The value of α for the F region found by this method, using records of Radio Ceylon transmissions on 11.98 mc, is 4.16×10^{-10} cm^3/seconds. Using vertical-incidence measurements at Calcutta, a value of 13.16×10^{-11} cm^3/seconds is obtained, compared with 13.14×10^{-11} cm^3/seconds calculated by the usual method.

551.510.535 2654

A Statistical Study on the Minimum Frequency in $h'f$ Curve for the E Region of the Ionosphere—H. Kamiyama. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 13–24; 1951.) The diurnal and seasonal variation of the minimum frequency in the HF curve for the E region is investigated, and also its relation to the sunspot number. The diurnal variation suggests the existence below the E layer of an absorbing layer which is ionized by solar radiation. The electron density in the D layer is estimated to be 1.5×10^4/cm^3.

551.510.535 2655

Wave Hypothesis of Moving Irregularities in the Ionosphere—C. O. Hines. (*Nature* (*London*), vol. 171, p. 980; May 30, 1953.) A preliminary discussion of magneto hydrodynamic effects which may afford an alternative explanation of the motion of ionospheric irregularities, usually referred to as "winds," in terms of the propagation of a wave-like disturbance. It is found that traveling atmospheric disturbances, governed by pressure oscillations and gravitational forces, will be accompanied by em oscillations which can, under special resonance conditions, become large. The corresponding amplification of the associated electron motions would render such disturbances particularly susceptible to detection by radio methods. Gravity tends to confine the movement of these disturbances to the horizontal plane, but a secondary vertical component is possible. A full treatment is to be published later.

551.510.535 2656

An Analysis of Electron-Density Variations in the F_2 Layer after Sunset—T. Yonezawa. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 1–12; 1951.) Analysis of data obtained at Kokubunji, taking temperature variations into account and assuming a linear law for the rate of disappearance of electrons, indicates that the nocturnal variation of electron density in the F_2 layer is explained more satisfactorily by the attachment theory than by the recombination theory. The corresponding temperature variations deduced are not satisfactory for the winter months, for which other factors must be taken into account.

551.510.535:523.746 2657

Critical-Frequency Variations—T. W. Bennington. (*Wireless Eng.*, vol. 30, pp. 175–179; July 1953.) Twelve-month running averages of f_0F_2 are plotted against twelve-month running averages of the sunspot number for two stations in the northern hemisphere, two in the southern hemisphere, and one near the equator. For the northern-hemisphere stations the slope of the curve is less at the higher values of sunspot number, for the southern-hemisphere stations the slope is constant, and for the equatorial station the slope varies in an intermediate manner. These differences may be related to the differences in the annual variation of f_0F_2 in the various regions considered.

551.510.535:523.78 2658

Effects on the F Regions of the Ionosphere of the Solar Eclipse of May 9, 1948—Y. Nakata. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 21–30; 1950.) Observations indicated the development during the eclipse of a new layer between the F_1 and F_2 layers. Discontinuities of the F_2-layer critical frequency and virtual-height curves and of the F_1-layer critical-frequency curve were noted for a period of about 30 min before and after the first contact. Estimates are made of the electron-density variations involved.

551.510.535:523.78 2659

The $h't$ Measurement of Ionosphere at the Time of the Annular Eclipse of May 9, 1948, at Wakkanai, Hokkaido, in Japan—H. Uyeda, H. Kudo, T. Shimizu and R. Sato. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 75–77; 1950.) Measurements were made at frequencies of 2.1, 4.5 and 7.05 mc. The results obtained show that (a) the absorption in and below the E layer decreased as the eclipse approached its maximum and increased again after the maximum phase; (b) the maximum F_1-layer electron density began to decrease immediately after first contact and continued to decrease to a minimum about 15 min after the maximum phase of the eclipse, then recovering.

551.510.535:535.34 2660

27-Day Variations in the Absorption of the D Region of the Ionosphere over Singapore

and Slough—G. Lange-Hesse. (*Jour. Atmos. Terr. Phys.*, vol. 3, pp. 153–162; April 1953. In German.) Appreciable variations of D-layer RF absorption, with a 27-day period, are found throughout the year at Singapore, but only during the summer months at Slough. Other variations of absorption, of larger amplitude than in summer, are found at Slough in the winter months, but are not related to the solar-rotation period of variations of particle radiation. The bearing of these results on radio communication and on ionospheric forecasting is discussed briefly. See also 3538 of 1952.

551.510.535:535.34 2661

Measurement of Ionospheric Absorption—P. Dominici. (*Ann. Geofis.*, vol. 5, pp. 561–568; Oct. 1952.) The significance of ionospheric absorption is discussed, and commonly used methods of measurement are examined.

551.510.535:537.567/.568 2662

The Recombination Coefficient and the Temperature Variation in the Upper Atmosphere at Night—T. Yonezawa. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 79–85; 1950.) The value of the F_2-layer recombination coefficient at Kokubunji, near Tokyo, shows a marked seasonal change, the maximum being in January and the minimum in June–July. Calculation of the corresponding relative temperatures indicates that in winter some mechanism other than temperature variation must be taken into account.

551.510.535.550.386:523.75 2663

The Solar-Flare Type Variation in Geomagnetic Field and the Integrated Electrical Conductivity of the Ionosphere: Part 1—T. Nagata. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 155–172; 1950.) Assuming that the solar-flare type of variation of the geomagnetic field is caused by anomalous increase of the electrical conductivity of the ionosphere, treatment based on the dynamo theory gives a value for the integrated conductivity of the ionosphere of the order of 5×10^{-8} emu, which is in good agreement with the value deduced from ionospheric observations.

551.510.535:550.386:523.75 2664

The Solar-Flare Type Variation in Geomagnetic Field and the Integrated Electrical Conductivity of the Ionosphere: Part 2—Effect of F layer—T. Nagata and T. Suzuki. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 201–205; 1950.) Analysis of mutual-inductance effects between different ionosphere layers shows that, as regards the effect of layer currents on the geomagnetic field, a single layer can be assumed, the conductivity of which is equal to that of the various layers integrated vertically throughout the whole conductive region. The previous estimate of about 5×10^{-8} emu for the integrated conductivity of the whole ionosphere is thus confirmed. Part 1: 2663 above.

551.510.535:550.386:523.75 2665

The Solar Flare Type Variation in Geomagnetic Field and the Integrated Electric Conductivity of the Ionosphere: Part 3—Effect of the Earth—T. Nagata and M. Tazima. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 113–121; 1951.) Further discussion, taking account of the electrical conductivity of the earth. Part 2: 2664 above.

551.510.535:550.386:523.75 2666

The Solar-Flare Type Variation in Geomagnetic Field and the Integrated Electric Conductivity of the Ionosphere: Part 4—The Conductivity of the Ionosphere over Japan—T. Nagata. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 123–128; 1951.) Statistical analysis of data obtained at Kakioka during 1936–1942 gave the average value of the integrated electrical conductivity of the ionosphere over Japan as 7×10^{-8} emu. Part 3: 2665 above.

551.510.535:621.3.013.783 2667

The Shielding Effect of the Ionosphere—M. Sugiura. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 31–36; 1950.) Analysis of the effect of the ionosphere in screening the earth from external em fields, taking account of the conductivity of the earth.

551.510.535:621.396.72:621.3.087.47 2668

Ionospheric Stations—*URSI Inform. Bull.*, pp. 19–29; Jan./Feb. 1953.) A list is given of all stations from which results of observations are regularly received at Slough; in a second list, which replaces those previously published, ionospheric stations are grouped according to the country controlling them.

551.594.6:621.396.11 2669

Atmospherics with Very Low-Frequency Components—Hepburn and Pierce. (*See* 2771.)

551.510.535(410) 2670

Radio Research Special Report No. 23. Characteristics of the Ionosphere observed in Great Britain, 1930–46. [Book Notice]—Publishers: H.M. Stationery Office, London; 1952. (*Gov. Publ., London*, p. 23; April 1953.) Report of measurements at Slough, 1930–1946, and at Burghead, 1941–1946.

LOCATION AND AIDS TO NAVIGATION

621.396.9 2671

The Effective Number of Pulses per Beamwidth for a Scanning Radar—L. V. Blake. (PROC. I.R.E., vol. 41, pp. 770–774; July 1953.) As regards signal/noise ratio, the optimum value for the angle over which the pulses are integrated, assuming a beam of Gaussian form, is 0.84β, where β is the half-power beam width. The equivalent rectangular beam has a width of 0.47β; hence the equivalent number of full-amplitude pulses is 0.47 times that usually assumed, corresponding to a value of system sensitivity lower by 1.6 db than that calculated on the assumption of integration over the angle β.

621.396.9 2672

M.T.I. in Pulse Radar Systems and the Doppler Myth—J. F. Bachman. (*Tele-Tech*, vol. 12, pp. 86–88, 172; April 1953.) The operation of a PPI system providing a display only of moving targets, and its dependence on echo delay, not on frequency shift, is explained.

621.396.9:551.311.17/.18 2673

Radar and Ice—L. S. Le Page and A. L. P. Milwright. (*Jour. Inst. Nav.*, vol. 6, pp. 113–127; April 1953. Discussion, pp. 128–130.) Data collected during a voyage on an ice-breaker between Quebec and Port Churchill in the summer of 1952 show that in a calm sea, ice formations of all types are detectable at distances of 2 miles or more. Under conditions of rough sea and bad visibility it is unsafe to rely upon the radar display when sea clutter extends to distances>1 mile. Suggestions for the provision of various anticlutter devices are made.

621.396.9:681.142 2674

Punched-Card-Controlled Aircraft Navigation Computer—E. H. Fritze. (PROC. I.R.E., vol. 41, pp. 734–742; June 1953.) Theory and description of a course-line computer for use with the available U. S. vhf omnirange system or with the proposed omnirange-dme system. A position fix can be obtained with the equipment by triangulation, using line-of-bearing data from two omniranges. A further computation then gives course and distance indications with respect to a ground point selected by the pilot. Alternatively, position-fix information derived from one omnirange-dme ground station may be used for course-line computation. The punched-card system and pictorial course-display instrumentation associated with the computer are described.

MATERIALS AND SUBSIDIARY TECHNIQUES

535.5:621.3.032.461 2675

Sorption of Gases at Very Low Pressures by Thorium Powder—S. Wagener. (*Proc. Phys. Soc.*, vol. 66, pp. 400–413; May 1, 1953.) Measurements were made of the rate of sorption of oxygen and hydrogen at pressures between 10^{-7} and 10^{-3} mm Hg as a function of the temperature of the thorium and of the period of its exposure to the gas. The significance of the results is discussed in relation to the gettering of tubes.

535.215:537.311.33 2676

Electrolytic Conduction in Cs_3Sb—H. Miyazawa and S. Fukuhara. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 645–647; Nov./Dec. 1952.) Measurements were made of the conductivity of thin layers of Cs_3Sb over a range of temperatures; the current was found to decrease slowly with time for a constant applied voltage. A detailed study indicated that electrolytic action occurred when the field strength exceeded a threshold value, the Cs ion being mobile.

535.215.4:546.817.221 2677

The Photoelectric and Optical Properties of a Special Type of Lead-Sulphide Layer—L. Genzel and H. Müser. (*Z. Phys.*, vol. 134, pp. 419–424; March 25, 1953.) The preparation of photo-resistors for use in the range of visible light and up to 1.8 μ is described. The photoelectric current i resulting from an illumination intensity I is given by $i\propto \gamma$, with $0.5<\gamma<1$, γ being independent of λ. The response to illumination of varying modulation frequency falls from 80% of maximum at 10 cps to 4.5% at 2 kc.

535.343:535.61–15:546.289 2678

The Infrared Absorption Characteristics of Thermiated Germanium—D. H. Rank and D. C. Cronemeyer. (*Phys. Rev.*, vol. 90, pp. 202–203; April 15, 1953.) Ge crystals when heated to 900°C and quenched in air show marked absorption in the infrared region. Subsequent annealing at 500°C reduces the absorption to the value prior to heat treatment.

535.37:546.472.21 2679

Electronic Transitions in the Luminescence of Zinc-Sulfide Phosphors—R. H. Bube. (*Phys. Rev.*, vol. 90, pp. 70–80; April 1, 1953.) The transitions involved in the processes of (a) absorption, (b) excitation, (c) emission, (d) trapping, (e) photoconductivity, at room temperature, have been measured for ZnS phosphors without impurity, and with Ag, Cu or Mn as impurity. A tentative energy-level diagram, based on the results of the measurements, is presented for the excitation and emission processes in ZnS phosphors.

535.376 2680

Decay of Long-Period Afterglow of Alkali Halides under Cathode-Ray Excitation—H. N. Bose and J. Sharma. (*Proc. Phys. Soc.*, vol. 66, pp. 371–376; May 1, 1953.) The results obtained at room temperature and at that of liquid oxygen show that, for the period 10–100 seconds after cessation of excitation, the decay follows the law $I\propto t^{-n}$, the values of n lying between 0.7 and 1.1. The decay rates are different for different parts of the spectrum.

537.228:537.226 2681

The Relation between the High-Voltage Polarization of Dielectrics and the Intensity of the Electric Field—V. A. Presnov. (*Zh. Tekh. Fiz.*, vol. 22, pp. 955–960; June 1952.) It is shown that measurements of the electrical conductivity of dielectrics in strong electric fields for various short time intervals can be used for investigating the high-voltage polarization of dielectrics.

537.311.3:539.23 2682

Capacitance Effects in Thin Conductive Films—J. N. Humphrey, F. L. Lummis and W. W. Scanlon. (*Phys. Rev.*, vol. 90, pp. 111–114; April 1, 1953.) For some films of PbS or Te, the observed frequency dependence of resistance can be explained by distributed capacitance alone, but in some films both distributed and intercrystallite capacitance must be assumed.

537.311.3:546.824–31 2683

Influence of Impurities on Electrical Conductivity of Rutile—G. H. Johnson. (*Jour. Amer. Ceram. Soc.*, vol. 36, pp. 97–101; March 1953.) The addition of certain oxides to TiO_2 increases its conductivity. Reduction has the same effect but produces an imperfect lattice. The insulating properties of a contaminated crystal can be partly restored by incorporating into its lattice cations of a lower valency, such as Al or Y.

537.311.3:666.76 2684

Electrical Resistance of some Refractory Oxides and their Mixtures in the Temperature Range 600° to 1500°C—J. R. Hensler and E. C. Henry. (*Jour. Amer. Ceram. Soc.*, vol. 36, pp. 76–83; March 1953.) Results of measurements indicate the predominance of surface conduction in SiO_2, Al_2O_3 and their mixtures, and show the effects of adding SiO_2, Cr_2O_3 and NiO respectively to TiO_2, Al_2O_3 and MgO. Al_2O_3–Cr_2O_3 mixtures with more than 35% Cr_2O_3 appear suitable as heating elements.

537.311.31:539.234 2685

Deviations from Ohm's Law in Very Thin Metal Layers—M. Perrot and J. P. David. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1641–1643; April 27, 1953.) Experimental results obtained with films of Ag, Al and Si at ordinary temperatures do not confirm the empirical law found e.g. by van Itterbeek et al. (2828 of 1952) relating the resistance of thin films to the strength of the applied field at low temperatures. The results show that the deviations from Ohm's law increase as the surface resistivity of the film increases and as the thickness of the film decreases.

537.311.33 2686

The Influence of the Surface on the Type of Electrical Conduction of a Semiconductor—S. G. Kalashnikov and Ya. E. Pokrovski. (*Zh. Tekh. Fiz.*, vol. 22, pp. 883–884; May 1952.) A comparison was made between ordinary solid samples and pressed-powder samples of a semiconductor. It appears that with finer powders the original electron conduction alters into hole conduction.

537.311.33 2687

Theory of Contact Phenomena in Semiconductors—A. I. Gubanov. (*Zh. Tekh. Fiz.*, vol. 22, pp. 729–735; May 1952.) The limits of applicability of the various aspects of the theory previously published by the author are determined. A comparison is made of the theoretical and experimental results for the case of a contact between Cu_2O (*p*-type) and TiO_2 (*n*-type). The most effective model of a metal rectifier is indicated.

537.311.33 2688

Semiconducting Intermetallic Compounds—R. G. Breckenridge. (*Phys. Rev.*, vol. 90, pp. 488–489; May 1, 1953.) Brief preliminary note of investigations on InSb, GaSb and AlSb; these compounds are semiconductors with high charge-carrier mobilities.

537.311.33 2689

D.C. Field Distribution in a "Swept Intrinsic" Semiconductor Configuration—R. C. Prim. (*Bell Sys. Tech. Jour.*, vol. 32, pp. 665–694; May 1953.) A system is considered consisting of an intrinsic semiconductor sandwiched between *n*-type and *p*-type extrinsic semiconductors. If a large reverse bias is applied to this system, making the *n*-type material positive with respect to the *p*-type material, the field set up in the intrinsic semiconductor sweeps away most of the mobile carriers. Analysis is presented for such a system. Curves are plotted showing the potential and field distribution in the intrinsic-semiconductor layer for different values of thickness and bias voltage.

537.311.33:546.23 2690

The Electrical Properties of Multicrystal Selenium—M. I. Iglitsyn. (*Zh. Tekh. Fiz.*, vol. 22, pp. 885–887; May 1952.) The dark conductivity and the Hall effect were investigated. The results obtained do not conform to the band theory.

537.311.33:[546.28+546.289 2691

Temporary Traps in Silicon and Germanium—J. R. Haynes and J. A. Hornbeck. (*Phys. Rev.*, vol. 90, pp. 152–153; April 1, 1953.) Experimental evidence of the existence of traps is described, with particular reference to effects observed with a uniform crystal of 28-Ω.cm *p*-type Si. After illumination is cut off, the decay of photoconductivity of the crystal takes place in three well-defined steps: (a) a rapid decrease for about 20 μs; (b) a slower decrease asymptotically exponential, for about 10 ms; (c) a very slow decrease for about 260 seconds. An explanation of these effects, involving the assumption of shallow traps and deep traps, is given.

537.311.33:546.289 2692

Recombination Rate in Germanium by Observation of Pulsed Reverse Characteristic—E. M. Pell. (*Phys. Rev.*, vol. 90, pp. 278–279; April 15, 1953.) When a square voltage pulse is applied to a Ge diode, a forward current pulse is followed by one in the reverse direction which gradually decays to the reverse saturation current. The shape of the decay curve is used to determine the recombination rate of the minority carriers injected during the forward pulse. Results agree well with those obtained by the light-beam method.

537.311.33:546.289 2693

Observations of Dislocations in Lineage Boundaries in Germanium—F. L. Vogel, W. G. Pfann, H. E. Corey and E. E. Thomas. (*Phys. Rev.*, vol. 90, pp. 489–490; May 1, 1953.)

537.311.33:546.289:534.321.9 2694

Ultrasonic Attenuation Measurements in Germanium—R. Truell and J. Bronzo. (*Phys. Rev.*, vol. 90, p. 152; April 1, 1953.) Large differences in attenuations were found for samples of Ge differing as regards impurity content, heat treatment, etc. The frequencies used ranged from 15 to 100 mc. Attenuation measurements may possibly be used to indicate the relative amounts of defects in various samples.

537.311.33:546.289:621.396.822 2695

Theory of Magnetic Effects on the Noise in a Germanium Filament—H. Suhl. (*Bell Sys. Tech. Jour.*, vol. 32, pp. 647–664; May 1953.) The redistribution of carriers over the cross section of a rectangular Ge filament due to application of a magnetic field perpendicular to one pair of its sides is analyzed, and calculations are made of the resulting variation of noise power to be expected in some special cases, on the basis of the theory advanced by Montgomery (122 of January) that the noise originates at least partly from variations in concentration of the minority carriers.

537.311.33:546.682.86:537.312.8 2696

The Magnetoresistance Effect in InSb—G. L. Pearson and M. Tanenbaum. (*Phys. Rev.*, vol., 90, p. 153; April 1, 1953.) The method used in the preparation of the compound, and the results of magnetoresistance measurements, are described. With the field H perpendicular to the current I, $\Delta\rho/\rho = 8.10^{-9} H^2$ at room temperature over the range 0–13000 gauss. The effect decreases with decreasing angle between H and I and approaches zero when H and I are parallel. This is in agreement with simple theory which assumes spherical energy surfaces.

537.311.33:621.314.632:546.289 2697

The Influence of Mobility Variation in High Fields on the Diffusion Theory of Rectifier Barriers—R. E. Burgess. (*Proc. Phys. Soc.*, vol. 66, pp. 430–431; May 1, 1953.) Shockley has reported (1011 of 1952) that in Ge the electron drift velocity for fields >3 kv/cm has a constant value. The effect this constant drift velocity has in the diffusion equation for a rectifying contact between a metal and *n*-type Ge is examined, some simplifying assumptions being made. The expression derived for the current density from metal to semiconductor is found to have the form associated with a Mott layer; it involves no specific assumption about the distribution of ions in the barrier, i.e., about the spatial variation of the electrostatic potential for electrons. For reverse voltages the expression for the current density takes the usual ideal form.

537.311.33:621.314.632:546.289 2698

The Barrier Layer of a Germanium Plate Rectifier with Forward Current—W. Bösenberg and E. Fues. (*Z. Naturf.* vol. 6a, pp. 741–744; Nov. 1951.) Calculations are made of the field and concentration distribution of electrons and holes in the Schottky barrier layer of a metal/Ge contact; the results facilitate understanding of the saturation effect in the neighborhood of a transistor emitter electrode. For high values of forward current the concentration of electrons and holes in the semiconductor is greatly increased.

537.311.33:621.314.634 2699

The Blocking Mechanism of Selenium Rectifiers—S. Poganski. (*Z. Phys.*, vol. 134, pp. 469–482; March 25, 1953.) Experiments with specially prepared Se rectifiers are described. The variation of the properties of Se/metal barrier layers with the difference between the work functions of Se and the metals Bi, Zn, Pb, Cd, In, is in agreement with Schottky's boundary-layer theory. For rectifiers with an intermediate CdSe layer, the barrier-layer properties were practically independent of the electrode metal used, indicating that in this case the barrier layer was at the CdSe/Se boundary, i.e., between an excess and a defect semiconductor.

537.582 2700

Thermionic Constants of Metals and Semiconductors: Part 3—Monovalent Metals—S. C. Jain and K. S. Krishnam. (*Proc. Roy. Soc. A*, vol. 217, pp. 451–461; May 21, 1953.) An account is given of measurements on Cu Ag and Au, using the effusion method. The value found for the coefficient A in Richardson's equation is only slightly less than the theoretical value of 120 A/cm^2 per deg^2. Part 2: 1392 of May.

538.221 2701

Magnetic Compounds with Perovskite Structure: Part 3—Ferromagnetic Compounds of Cobalt—G. H. Jonker and J. H. van Santen. (*Physica*, vol. 19, pp. 120–130; Jan./Feb. 1953. In English.) Polycrystalline mixed crystals of $(La,Sr)CoO_3$ have been prepared. Perovskite structure is found for all compositions. Ferromagnetism is observed for intermediate Sr concentrations. Part 2: 656 of 1951.

538.221 2702

Applications and Properties of Ferroxcube (*Elec. Appl. Bull.*, vol. 13, p. 201; Nov./Dec. 1952.) Correction to paper noted in 750 of March.

538.221 2703

On the A.C. Magnetization Characteristics of a Perminvar Wire—T. Hirone, H. Watanabe, T. Iwata and K. Ikeda. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 593–598; Nov./Dec. 1952.) Observations made on a wire under tension are discussed on the basis of the pipe-domain theory. The existence of an effect other than eddy currents is indicated. The results are in general agreement with those of Williams *et al.* (855 of 1951).

538.221:548 2704

The Anisotropy of the Coercive Force in Monocrystals of Silicon-Iron Alloys—V. V.

Druzhinin and R. I. Yanus. (*Zh. Tekh. Fiz.*, vol. 22, pp. 848–857; April 1952.) Experimental results indicate that the coercive force in crystallites of these alloys has a maximum along the digonal axis of the crystal and not the trigonal axis, as has been previously assumed on the basis of limited observations by Williams (1210 of 1938).

538.662:549.517.2 **2705**
Thermomagnetic Properties of Rhombohedric Ferric Oxide—H. Bizette, R. Chevallier and B. Tsaï. (*Compt. Rend. Acad. Sci. (Paris)*, vol. 236, pp. 2043–2045; May 27, 1953.) Results of measurements in the range 73–293°K on two samples cut from a crystal of hematite are shown graphically and discussed. The λ transformation extends over the range 173–253°K. See also 3125 of 1952 (Néel & Pauthenet).

546.817.221:[535.34+535.215 **2706**
Optical and Photoelectric Properties of Microcrystalline Layers of Lead Sulphide in the Visible and Infrared Regions—P. Vernier. (*Jour. Phys. Radium*, vol. 14, pp. 175–178; March 1953.) Measurements of PbS layers are reported and the photoelectric sensitivity and absorption coefficient k of different layers are compared. Overall sensitivity varies considerably from layer to layer; k decreases rapidly with increasing λ and is not dependent on layer thickness. In layers prepared by distillation or chemical action, sensitivity is generally high; the sharpest fall in k and also in sensitivity occurs in the ranges 0.9–1.4 μ and 2.5–3 μ.

548.55:546.289 **2707**
Apparatus for Drawing Single Crystals—J. Malsch and F. W. Dehmelt. (*Telefunken Ztg.*, vol. 26, pp. 121–122; March 1953.) Description of high-vacuum equipment for manufacturing Ge crystals of extreme purity.

549.325.2:[537.311.3+538.632 **2708**
Electrical Properties of Molybdenite—R. Mansfield and S. A. Salam. (*Proc. Phys. Soc.*, vol. 66, pp. 377–385; May 1, 1953.) Conductivity, Hall coefficient and thermoelectric power of natural crystals of MoS_2 were measured over the temperature range from −183° to 500°C. The change of conductivity on applying a magnetic field was measured at room temperature. The majority of the specimens were *p*-type semiconductors. The results are discussed in relation to the theory of charge carriers in semiconductors.

621.318.2:669.255.231 **2709**
Permanent-Magnet Properties of Cobalt-Platinum Alloys—D. L. Martin and A. H. Geisler. (*Jour. Appl. Phys.*, vol. 24, p. 498; April 1953.) Comment on 1035 of April (Adams *et al.*), pointing out that the properties of Co-Pt alloys, which depend on composition and heat treatment, compare very favorably with those of bismanol.

621.396.62+621.397.62].002.2 **2710**
Mechanized Dip-Soldering of Television Receivers—K. M. Lord. (*Electronics*, vol. 26, pp. 130–137; June 1953.) Detailed account of the production technique developed for the automatic assembly and soldering of the chassis of either television or radio receivers.

661.1.037.5 **2711**
Hermetic Glass/Kovar Seals—W. Düsing. (*Telefunken Ztg.*, vol. 26, pp. 111–120; March 1953.) The application of kovar for glass/metal seals in high-power transmitter tubes, particularly uhf tubes, is described. Different types of seal are illustrated and limiting ratios of expansion coefficients are noted. The occurrence of strain in the glass due to electrolysis, the influence of the lead content of the glass and advantages of coating the kovar with a highly conductive metal are discussed.

661.1.037.5 **2712**
Fundamentals of Glass-to-Metal Bonding: Part 1—Wettability of some Group-I and Group-VIII Metals by Sodium-Silicate Glass—V. F. Zackay, D. W. Mitchell, S. P. Mitoff and J. A. Pask. (*Jour. Amer. Ceram. Soc.*, vol. 36, pp. 84–89; March 1953.) The degree of wetting of Cu, Ag, Au, Pd, Pt and Ni by molten glasses containing different amounts of soda was observed in vacuo and in various atmospheres. Differences of contact angle may be related to the polarizing power of the metal. In O_2 and H_2, chemical reactions are possible which tend to increase spreading.

MATHEMATICS

517.941.9 **2713**
Use of Tschebyscheff-Polynomial Operators in the Numerical Solution of Boundary-Value Problems—G. Shortley. (*Jour. Appl. Phys.*, vol. 24, pp. 392–396; April 1953.) Discussion of techniques suitable for obtaining, on automatic computers, numerical solutions of boundary-value problems arising from linear partial differential equations such as those of Laplace and Poisson.

518.5:512.99 **2714**
A New Vector Slide Rule—E. Friedlander. (*G. E. C. Jour.*, vol. 20, pp. 91–94; April 1953.) A description is given of the design principles; construction and operation of a slide rule which should greatly simplify the manipulation of complex quantities. Its most direct application in electrical engineering is the conversion of resistance and reactance into impedance and phase angle, which can be read directly. It also eliminates many of the transformations necessary in the analysis of real and complex electrical networks by means of a convenient combination of direct and reciprocal scales.

519.271.3:620.113.2 **2715**
The Efficiency of Sequential Sampling for Attributes: Part 1—Theory—H. C. Hamaker (*Phillips Res. Rep.*, vol. 8, pp. 35–46; Feb. 1953.) For practical purposes, Wald's 3-parameter probability-ratio sequential plans may be reduced to a 2-parameter set of plans with decision lines symmetrical with respect to the origin.

681.142 **2716**
Micro-programming and the Design of the Control Circuits in an Electronic Digital Computer—M. V. Wilkes and J. B. Stringer. (*Proc. Camb. Phil. Soc.*, vol. 49, Part 2, pp. 230–238; April 1953.)

681.142 **2717**
The Relative Merits of A.C. and D.C. as a Signal Source in Analogue Computors—K. H. Simpkin. (*Elec. Eng.*, vol. 25, pp. 230–233; June 1953.)

681.142 **2718**
Analog Computer solves Geophysical Problems—S. Kaufman. (*Electronics*, vol. 26, pp. 174–177; June 1953.) Description of equipment for rapid calculations from the large number of field observations for an extensive region.

681.142 **2719**
Fourier Analyzer—F. J. McDonal. (*Rev. Sci. Instr.*, vol. 24, pp. 272–276; April 1953.) An analogue computer is described which provides Fourier analyses of transients encountered in seismic research.

681.142 **2720**
A Five-Channel Analog Correlator—M. J. Levin and J. F. Reintjes. (*Tele-Tech*, vol. 12, pp. 70–72, 125; March 1953.) The operation and circuit details are described of equipment which determines simultaneously five points on the correlation curve of a time series and displays the approximate curve on a cro. The value for the time increment can be set between 1 and 400 μs by adjusting the rate at which the sampling-pulse generator is triggered.

681.142:517.941.4 **2721**
A Useful Theorem in Linear-Differential-Equation Theory, its Proof and its Application to Analogue Computors—D. O. Burns. (*Trans. Soc. Instr. Tech.*, vol. 4, pp. 173–176; Dec. 1952.) A theorem is given relating the generalized differential equation $f(D)x=\phi(D)y$ to the simpler form $f(D)x=y$ for certain initial conditions, where y represents a suddenly applied disturbance of the step type, or of a type that can be represented by a rational algebraic operation on the step function.

681.142:538.691 **2722**
Analogue Computer for Study of Trajectories in Electron Lenses—A. Hampikian. (*Compt. Rend. Acad. Sci. (Paris)*, vol. 236, pp. 1864–1866; May 11, 1953.) Description of a computer comprising an 8-stage network based on principles given by Grivet and Rocard (2810 of 1950), and of its use in determining the parameters of magnetic electron lenses.

681.142:621.396.9 **2723**
Punched-Card-Controlled Aircraft Navigation Computer—E. H. Fritze. (*See* 2674.)

MEASUREMENTS AND TEST GEAR

621.317.3:621.396.822 **2724**
A Simple Proof of the Formula for the Relative Accuracy of a Noise-Power Measurement with a Quadratic Detector—A. van der Ziel. (PROC. I.R.E., vol. 41, pp. 800–801; July 1953.) It is shown that, for certain stated conditions, the relative accuracy of a single noise-power measurement is $(2B\tau)^{-1/2}$, where B is the noise bandwidth and τ the time constant of the indicating instrument. If a critically damped galvanometer is used, the formula becomes $(4B\tau)^{-1/2}$.

621.317.3:621.396.822 **2725**
Measurement of the Constants of the Flicker Effect—H. Rothe, W. Dahlke and J. Schubert. (*Telefunken Ztg.*, vol. 26, pp. 77–84; March 1953.) A quick investigation of the low-frequency noise characteristic of a series of tubes can be made by the method described. This is based on the determination of the constants c and α in the equation $\bar{u}_2=(c/f^{\alpha})^2\Delta f$, where $\bar{u}^2$ represents noise voltage and f frequency. Measurements are reported on a number of Type-EF804 tubes connected as pentode and as triode.

621.317.321 **2726**
Electronic Device for the Precision Measurement of Direct Voltages by Comparison—R. Aumont and J. Romand. (*Rev. gén. élect.*, vol. 62, pp. 210–216; April 1953.) The device has high input impedance and can be used for comparing voltages from sources of high internal resistance, possibly with widely different values, or as a null detector in bridge circuits for the measurement of low voltages or of resistances. The two input voltages are applied to the measurement circuit alternately via a vibrator.

621.317.333.4.015.7:621.315.2 **2727**
Location of Cable Faults and Irregularities using Pulse-Echo Methods—W. Kroebel. (*Z. angew. Phys.*, vol. 5, pp. 48–52; Feb. 1953.) The design of suitable equipment is discussed particularly for measurements on power cables in Germany, where the distance between accessible points on earth cables is generally <10 km and the propagation velocity is $1.46–1.54=10^8$ m/s, corresponding to a maximum pulse delay of about 10^{-4} seconds and an accuracy to within about 1.3×10^{-8} seconds.

621.317.333.4.015.7:621.315.2 **2728**
Experimental Investigations with Direct-Voltage Pulses on Wide-Band Cables—C. W. Busch. (*Z. angew. Phys.*, vol. 5, pp. 52–60; Feb. 1953.) Using the equipment mentioned by Kroebel (2727 above) an investigation was made of the smallest observable irregularity in characteristic impedance. The experimental re-

sults, which are in good agreement with theory, show that for available wide-band cables an indication can be obtained of real reflection factors of about 1×10^{-4} at distances up to 1 km and of about 3×10^{-3} at distances up to 10 km. At these low values it is necessary to have an auxiliary display corresponding to a fault-free line, for comparison purposes. The accuracy of location for small faults is a function of the magnitude of the fault. A correction factor is derived to take account of uncertainty introduced by pulse deformation over long distances. Use of rectangular pulses is recommended.

621.317.335.029.63/.64:547.476.3 2729

On the Dielectric Constant of Rochelle Salt at 3000 Mc/s—H. Akao, T. Takakura and T. Sasaki. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 361–363; July/Aug. 1952.) A resonant-cavity method of measurement is described.

621.317.336:621.315.212 2730

Reflections in a Coaxial Cable due to Impedance Irregularities—G. Fuchs. (*Câbles & Transm.*, vol. 7, pp. 122–141; April 1953.) Translation. See 3495 of 1952.

621.317.34:621.396.645 2731

An Instrument for Measuring Complex Voltage Ratios from 1 to 100 Mc/s—G. Thirup and F. A. Vitha. (*Commun. News*, vol. 13, pp. 1–12; Feb. 1953.) See 1735 of June (Thirup).

621.317.343:621.315.212 2732

Determination of the Local and Mean Characteristic Impedance of Coaxial Cables by means of the Unit-Step Signal—G. Comte and A. Ponthus. (*Câbles & Transm.*, vol. 7, pp. 97–121; April 1953.) Mathematical theory is presented for the voltages produced by impedance irregularities in a coaxial cable to which is applied a unit-step signal or a rectangular type of periodic signal. Apparatus suitable for measurement of the local or mean characteristic impedance of production lengths of coaxial-pair cables is described and experimental results are given. The method used enables a direct relation to be established between transient and steady-state measurements on coaxial pairs.

621.317.343:621.392 2733

Transmission-Line Impedance Measurements—H. Sutcliffe. (*Wireless Eng.*, vol. 30, pp. 180–181; July 1953.) For $\lambda >$ im it is convenient to find the impedance from measurements of current or potential at three fixed points rather than from standing-wave measurements which involve moving the detector over a distance $\geq \lambda/2$. A method of calculating the impedance is indicated for the case of measurement points separated by $\lambda/8$, and a generally applicable graphical method is described which gives the solution in terms of the coordinates of a point on a Smith chart.

621.317.35:621.3.018.78 2734

Measurement of Nonlinear Distortion—A. Bloch. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 62–67; Jan. 1953.) A comparison is made of the harmonic, heterodyne (CCIF) and intermodulation (SMPTE) methods of measuring distortion. All three methods yield equivalent information when properly applied, but the intermodulation method is the most practical for giving a quantitative indication.

621.317.35:621.3.018.78 2735

Comparative Study of Methods for Measuring Nonlinear Distortion in Broadcasting Audio Facilities—D. E. Maxwell. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 68–78; Jan. 1953.) A comparison is made of the harmonic, heterodyne (CCIF) and intermodulation (SMPTE) methods as applied to studio AE equipment. For systems with sharply limited response at the upper end of the frequency band, e.g. sound-recording systems, the CCIF method is superior to the other two. For wide-band low-noise systems the harmonic method is satisfactory. A generator for simulating common distortion conditions is described.

621.317.35:621.3.018.78:534.851 2736

Distortion in Phonograph Reproduction—H. E. Roys. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 78–85; Jan. 1953.) A comparison is made of the harmonic, heterodyne (CCIF) and intermodulation (SMPTE) methods. The intermodulation method is useful for studying tracing distortion, while the heterodyne method has the advantage of enabling measurements to be made right up to the cut-off frequency of the system.

621.317.353.3:621.3.018.78 2737

Intermodulation Measurements—H. H. Scott. (*Jour. Audio Eng. Soc.*, vol. 1, pp. 56–61; Jan. 1953.) Intermodulation measurements are recommended as a basis for correlating measured values of nonlinearity with subjective assessments of reproducing systems. Known methods of measurement are described and their field of application is discussed.

621.317.61+621.317.772 2738

A Gain and Phase-Angle Measuring Set—F. B. Anderson. (*Elec. Eng., N. Y.*, vol. 72, p. 245; March 1953.) Digest only. Equipment is described which has an accuracy sufficient for circuit design purposes. The frequency range is 10 cps to 10 mc, the gain range −18 to +68 db, and the phase-angle range 0 to ±180°.

621.317.729 2739

The Accurate Mapping of Electric Fields in an Electrolytic Tank—K. F. Sander and J. G. Yates. (*Proc. IEE*, Part II, vol. 100, pp. 167–175; April 1953. Discussion, pp. 176–183.) A new technique for electrolyte-tank measurements is described. Square-wave excitation is used with two pairs of liquid probes and a specially designed differential amplifier, the detailed circuit of which is shown. Field strengths can be measured to within 0.1%. The relative merits of various electrode-electrolyte combinations are assessed.

621.317.753:[621.316.86:537.312.6 2740

A Direct-Reading Thermistor Bridge—W. B. W. Alison and J. C. E. Taylor: R. M. Pearson and F. A. Benson. (*Elec. Eng.*, vol. 25, p. 262; June 1953.) Comment on 1749 of June and authors' reply.

621.317.733:[621.317.332.029.3
+621.317.37 2741

Audio Impedance and Phase-Angle Meter—J. E. Hansen. (*Electronics*, vol. 26, pp. 172–173; June 1953.) This direct-reading instrument measures impedances up to 100 kΩ at frequencies between 30 cps and 15 kc. A simple bridge arrangement, incorporating two equal arms and a calibrated resistor, together with a balanced-rectifier system is used in a null-indication method. A switch is then operated so that the phase change across the impedance may be determined by comparing the bridge unbalance voltage with that across the calibrated resistor.

621.317.755 2742

Trapezoidal Distortion in Oscillograph Tubes—E. Gundert. (*Telefunken Ztg.*, vol. 26, pp. 89–94; March 1953.) An electrostatic deflection system is described by which trapezoidal distortion is avoided with both balanced and unbalanced input. The deflection plates nearer the screen have a curved edge on the side at which the beam enters; the radius of curvature is about 80% of the distance of this edge from the center of the deflection system nearer the cathode. Pincushion distortion is eliminated by edge bending where the beam enters the plates system.

621.317.755 2743

Modern High-Voltage Oscillographs with Cold Cathode—G. Induni. (*Arch. tech. Messen*, no. 207, pp. 83–86; April 1953.) Descriptions are given of one-, two- and four-beam types.

621.396.91 2744

Time Signals: Observatoire National de Paris, Bureau International de l'Heure—(*URSI Inform. Bull.*, no. 77, p. 30; Jan./Feb. 1953.) A table is given of transmission times, call signs, wavelengths and frequencies of rhythmic time signals radiated from the Pontoise station.

621.397.317.755 2745

A Television-Waveform Display Apparatus—G. N. Patchett. (*Elec. Eng.*, vol. 25, pp. 184–188 and 248–250; May/June 1953.) Equipment is described, with full circuit details, for selecting any number of lines, from two upwards, from the television signal, so that the detail of the frame synchronizing period or of any other portion of the wave form may be examined easily. Typical results obtained with the equipment are illustrated.

621.397.62.001.4 2746

A Transmitter for Production Testing of Television Receivers—J. M. Silberstein. (*Elec. Eng.*, vol. 25, pp. 224–229; June 1953.) Description of equipment for producing and distributing to various testing points a composite test-pattern signal. A block diagram illustrates the way in which all the different pulse frequencies required are derived from a frequency of 60.75 kc. Circuit diagrams of particular units are also given.

OTHER APPLICATIONS OF RADIO AND ELECTRONICS

531.775 2747

Development of an Electronic Tachometer—I. Dujardin, M. Hoyaux, M. Mary and E. Symon. (*Rev. gén. élect.*, vol. 62, pp. 191–197; April 1953.) Equipment designed primarily for testing small electric motors is described; pulses are generated photoelectrically and are counted by means of circuits similar to those commonly used in electronic computers.

538.569.2.047 2748

Certain Physiologic and Pathologic Effects of Microwaves—J. F. Herrick and F. H. Krusen. (*Elec. Eng.*, vol. 72, pp. 239–244; March 1953.) Investigations in connection with the use of microwaves for therapy are discussed. A cavity magnetron operating at 2.4–2.5 kmc with a maximum output of 125 W was used, and three different energy-directing systems were tried. The principal effects observed are due to the heating. Some harmful effects were noted, particularly in connection with treatment of the eye.

550.83:621.3 2749

Instrumentation for Geophysical Exploration—D. H. Clewell, R. A. Broding, G. B. Loper, S. N. Heaps, R. F. Simon, R. L. Mills and M. B. Dobrin. (*Rev. Sci. Instr.*, vol. 24, pp. 243–266; April 1953.) Descriptions are given of various pieces of special equipment used in oil prospecting, including transducers for converting earth vibrations into electrical signals, amplifiers, radiation detectors and magnetometers.

621.317.755:771.36 2750

Electronic Instrument for Production Testing of Camera Shutters—R. W. Lavender. (*Elec. Eng.*, vol. 72, pp. 336–340; April 1953.) The main piece of equipment described is a photocell-and-cro arrangement for indicating the relative timing of flash lamp and shutter.

621.383.001.8:535.61-15:778.37 2751

High-Speed Photography by Means of the Image Converter—J. A. Jenkins and R. A. Chippendale. (*Philips Tech. Rev.*, vol. 14, pp. 213–225; Feb. 1953.) See 1693 of 1952.

621.384.612 2752

Characteristics of the Synchrotron Beam—M. Camac. (*Rev. Sci. Instr.*, vol. 24, pp. 290–297; April 1953.)

621.384.612 2753
Effects of Magnetic Defects in a Strongly Converging Cosmotron [proton synchrotron]—J. Seiden. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1657–1659; April 27, 1953.)

621.384.613 2754
Betatron Monitor and Integrator—R. D. England and W. E. Ogle. (*Rev. Sci. Instr.*, vol. 24, pp. 267–268; April 1953.)

621.384.622.1 2755
Principle of the Theory of the Motion of Ions in Linear Accelerators—M. Y. Bernard. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 1655–1657; April 27, 1953.)

621.385.833 2756
The Design of Small [electron] Microscopes—E. Kinder. (*Optik, Stuttgart*, vol. 10, pp. 171–191; 1953.) General discussion, with details of an instrument designed for an accelerating voltage of 50 kv.

621.385.833 2757
Emission-Microscope Surface Images obtained with Electrons due to Oblique Bombardment by Ions—G. Möllenstedt and H. Düker. (*Optik, Stuttgart*, vol. 10, pp. 192–205; 1953.)

621.385.833 2758
New External Objective Aperture Centering and Interchanging Device for the R.C.A. EMU Electron Microscope—F. W. Bishop. (*Rev. Sci. Instr.*, vol. 24, pp. 269–271; April 1953.)

621.385.833 2759
Direct Measurement of Images in the Electron Microscope—H. Froula. (*Rev. Sci. Instr.*, vol. 24, pp. 304–306; April 1953.)

621.385.833:621.392.5:001.362 2760
Analogy between Electron Lenses and Electrical Quadripoles—F. Bertein. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 2047–2049; May 27, 1953.) Discussion shows that every electron lens has an equivalent quadripole network to which the same equations apply.

621.396.62:536.55 2761
The Sensitivity of Radio Thermometers—V. S. Troitski. (*Zh. Tekh. Fis.*, vol. 22, pp. 455–460; March 1952.) Sensitive radio receivers which can separate weak signals with a wide continuous spectrum from the background noise inherent in the receiver are considered; the possibility of using them for temperature measurements is discussed, and formulas are derived for calculating the sensitivity of these radio thermometers.

621.398+621.317.083.7]:621.396.61 2762
Broadcast Transmitter Remote-Control System—G. W. Lee. (*Electronics*, vol. 26, pp. 138–141; June 1953.) Description of control and telemetry equipment for Canadian 1-kw transmitters. Two pairs of telephone wires are required between studio and transmitter. Indications of the state of all important transmitter circuits, and of the RF output level and carrier-frequency drift can be obtained. An alarm circuit giving warning of overmodulation is included. Interruption of communication between studio and transmitter automatically switches off the transmitter.

621.398+621.317.083.7]:621.396.61 2763
Broadcast Remote Control—(*Electronics*, vol. 26, pp. 200–204; June 1953.) Two types of equipment are briefly described, both requiring two pairs of telephone wires and providing facilities for control and for telemetry via a dial-impulse selector switch. In one system the meter indications are corrected for variations of line resistance. In the other, audible tones are used for control switching.

PROPAGATION OF WAVES

534.24/.25+538.566.2 2764
Total Reflection of Waves from a Point Source—E. Gerjuoy. (*See* 2540.)

538.566 2765
Reflection of Waves from Varying Media—C. O. Hines. (*Quart. Appl. Math.*, vol. 11, pp. 9–31; April 1953.) The wave propagation equation $d^2f/dx^2+g(x)f=0$ is studied for functions $g(x)$ which are everywhere real, finite and continuous, have a constant positive value for large values of $|x|$ and smaller values in the neighborhood of $x=0$. Solutions are obtained in terms of a new variable $r=r(x)$ which is itself a solution of a Riccati equation. Exact formulas are derived for the reflection coefficient of a medium in terms of r. The curve of $r(x)$ is traced by inspection of the determining differential equation. Many media which might be expected to be highly reflecting are shown to be completely transparent to certain frequencies. The method gives an approximate evaluation of the exact solution rather than, as with the BWK method, an exact evaluation of an approximate solution. Em waves are treated principally, but the method is applicable also to mass waves.

538.566.2 2766
Propagation of Plane Electromagnetic Waves in the Ionosphere—R. Jancel and T. Kahan. (*Compt. Rend. Acad. Sci.* (*Paris*), vol. 236, pp. 2045–2047; May 27, 1953.) The propagation is considered of plane em waves in an ionized medium characterized by a certain dielectric tensor. The property of double refraction of such a medium is deduced and the corresponding refractive indexes are determined for directions respectively coincident with and perpendicular to that of the magnetic field. Formulas for the attenuation and group velocity of the waves are also obtained.

621.396.11 2767
The Value of Forecasts—D. A. Bell and C. M. Minnis. (*Wireless Eng.*, vol. 30, p. 184; July 1953.) Comment on 2110 of July and author's reply.

621.396.11:551.510.52:001.891 2768
Tropospheric Propagation Research—(*Tech. Bull. Nat. Bur. Stand.*, vol. 36, pp. 120–124; Aug. 1952.) An outline of the NBS program of theoretical and experimental investigations of the effects of climatic conditions, terrain, antenna characteristics, transmission frequency, etc., on the propagation of vhf and uhf signals over distances extending far beyond the horizon. A map is given which shows the location of NBS field stations, commercial radio installations, and FCC monitor stations.

621.396.11:551.510.535:523.75 2769
Observations on the Propagation of Very Long Radio Waves Reflected Obliquely from the Ionosphere during a Solar Flare—W. C. Bain. (*Jour. Atmos. Terr. Phys.*, vol. 3, pp. 141–152; April 1953.) Anomalies in the field of GBR (16 kc) observed at ranges of 400–550 km during the occurrence of solar flares are discussed. The main effect is due to a sky wave, varying in phase but not in amplitude, that reaches the observation point by single reflection from the ionosphere. An explanation of the magnitude of the effect is based on the assumption of two layers below the ionosphere E layer. The layer usually the lower of the two is normally responsible for oblique-incidence propagation of very long waves; the other layer is affected by the solar radiation during a flare. From the observed field-strength changes a value of 70 km is deduced for the apparent height of the layer responsible for oblique-incidence reflection of 16-kc waves. See also 2804 (Bracewell and Bain) and 2871 (Bain *et al.*) of 1952.

621.396.11:551.510.535:523.78 2770
Study of Propagation Characteristics of Obliquely Incident Impulse Wave in Time of the Solar Eclipse—K. Miya, T. Murata and H. Wada. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 1–20; 1950.) A report of observations on and around May 9, 1948. Pulses of duration 0.1 ms, frequency 9.24 mc, peak power 2kw and repetition frequency 50/seconds were transmitted from an antenna at Hiraiso directed towards Yamakawa, and were received at three stations in approximately the same direction at distances of 99, 542 and 1659 km respectively. The observed variations of wave form, attenuation and angle of incidence of the waves reflected from the F layer during the eclipse are shown graphically and discussed, with particular reference to the effect of distance between transmitter and observation point.

621.396.11:551.594.6 2771
Atmospherics with Very Low-Frequency Components—F. Hepburn and E. T. Pierce. (*Nature* (*London*), vol. 171, pp. 837–838; May 9, 1953.) Brief report of an extensive series of observations made at the Cavendish Laboratory. For distances up to 5,000 km, simple linear formulas are derived for the average values of the parameters t and $\tau/4$ of the low-frequency ("slow-tail") component as defined by Watson-Watt *et al.* (419 of 1938). The constants in these formulas have different day-time and night-time values. The features of the atmospheric wave form are discussed in terms of the waveguide theory of propagation between the earth and a homogeneous ionosphere (*see* Budden, 2773 below). Using theory developed by Hales (2888 of 1948), interrelated solutions are obtained for the ionosphere height h and conductivity σ; combining these with available estimates of the variation of σ with h, the "slow-tail" observations indicate 65 km and 5×10^3 esu as the day-time values of h and σ respectively, and 90 km and 11×10^3 esu as the night-time values.

621.396.11:621.396.812 2772
Correlations of 100-Mc/s Radio Propagation with Certain Meteorological Variables—K. H. Jehn and R. C. Staley. (*Jour. Atmos. Terr. Phys.*, vol. 3, pp. 163–171; April 1953.) Observations are reported of signal-strength measurements for paths of 78 and 175 miles in Texas. High signal strengths are in general associated with maritime tropical air, and lower strengths with air of polar (continental) origin. A correlation is found between signal strength and the vertical gradient of the refractive index. Atmospheric turbulence also has an effect on the propagation of 100-mc signals, a scattering mechanism being possibly involved.

621.396.11.029.45 2773
The Propagation of Very Low-Frequency Radio Waves to Great Distances—K. G. Budden. (*Phil. Mag.*, vol. 44, pp. 504–513; May 1953.) Experimental results obtained by Weekes (1491 of 1950) with 16-kc signals transmitted over distances of 340–3640 km are discussed, using the theoretical approach in which the region between the earth and the ionosphere is considered as a waveguide (1108 of April). The measurements can be explained in terms of the four least-attenuated waveguide modes. Neglecting the geomagnetic field, and assuming the ionosphere to be a homogeneous sharply bounded medium, the height of the boundary is found to be 69.1±0.5 km.

621.396.81 2774
On the Study of Attenuation Characteristics for H.F. and M.F. and its Application to Calculation of Field Intensity—K. Miya, S. Ouchi and S. Kanaya. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 25–41; 1951.) From analysis of experimental results, formulas for the attenuation of waves reflected from the E and F layers of the ionosphere are developed, and are applied to the problem of calculating the field strength of radio waves once reflected from the ionosphere or undergoing multireflection between ionosphere and earth.

621.396.81 2775
Field Intensity of Scattered Wave in Radio Wave Propagation—K. Miya, T. Kobayashi

and N. Wakai. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 55–73; 1951.) Waves traveling via multi-hop paths were always found to be accompanied by scattered waves arising from irregular reflection at the earth's surface. Observations of these scattered waves enabled calculations to be made of the scattering coefficients for ground and for a sea surface with small islands. The delay and wave form of the scattered waves, as deduced from the scattering coefficient, agreed well with observational results.

621.396.81 2776

Experimental Study on Scattered Echoes—T. Kono. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 127–135 and 189–199; 1950.) Investigations are described from which it is concluded that scattered echoes are due to irregular reflection at the surface of the earth during the course of multi-reflection paths. A formula for the field strength of scattered echoes gives results in agreement with measured values.

621.396.81 2777

A Tentative Method of Calculation of H.F. Radio Sky-Wave Field Intensity by use of Transmission Curve—K. Maeda, Y. Aono and T. Kobayashi. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 61–70; 1950.) A graphical method of determining field strength is proposed which utilizes a curve for field strength as a function of vertical-incidence limiting frequency and also the normal height/frequency curve.

621.396.81 2778

Field Intensity for Long-Distance Transmission deduced from the Long Time Measurement—H. Uyeda and T. Obayashi. (*Rep. Ionosphere Res.* (*Japan*), vol. 4, pp. 71–73; 1950.) A method of calculating field strength for long transmission paths, taking account of E-layer and F-layer attenuations and F-layer critical frequency for vertical incidence, is applied to the paths from Tokyo to San Francisco and London. Better agreement with observation is found for the San Francisco path than for that to London.

621.396.81 2779

Calculation of Field Intensity about the Antipode of the Transmitting Station—K. Furutsu. (*Rep. Ionosphere Res.* (*Japan*), vol. 5, pp. 159–165; 1951.) Formulas are derived for the field strength in the neighborhood of the antipode, taking account of ionospheric conditions.

RECEPTION

621.396.621 2780

Noise Limiter for Mobile V.H.F.—N. Bishop. (*Electronics*, vol. 26, pp. 164–165; June 1953.) A conventional full-wave shunt-type diode limiter with self-rectified bias, connected across the primary circuit of the final IF transformer of the receiver, improves the intelligibility of AM speech signals under conditions of strong impulse interference.

621.396.621:621.396.822 2781

Study of a Signal, consisting of Periodic Rectangular Pulses, superposed on Thermal Noise. The Combination being Clipped, Investigation of the Optimum Amount of Clipping—L. Robin. (*Ann. Télécommun.*, vol. 8, pp. 127–130; April 1953.) A large number of samples of the voltage of the combination of signal and noise are added, each sampling being coincident with one of the signal pulses. Analysis is presented, for the case when a limiter is applied, in order to determine the conditions under which the ratio of the mean value of the output voltage to the standard deviation noise-voltage should be as great as possible. An optimum degree of clipping is determined and a curve is constructed which shows the ratio of the variation of output voltage to the square of its mean value, as dependent on the ratio of the clipping height to the standard deviation noise-voltage.

621.396.621:621.396.822 2782

Statistical Criteria for the Detection of Pulsed Carriers in Noise: Part 1—D. Middleton. (*Jour. Appl. Phys.*, vol. 24, pp. 371–378; April 1953.) A theory for the detection of pulsed carrier waves, of constant amplitude, in narrow-band random noise is based on several optimum tests of a statistical hypothesis against a single alternative, i.e., signal and noise *vs* noise. Siegert's concept of the betting curve whereby, for a finite integration time, the minimum detectable signal is uniquely defined, is introduced. Three types of observer are considered, the Neyman-Pearson, the ideal and the sequential type, whose characteristics are determined by the test method adopted. In all cases it is found that the best second detector is a log *Io* rectifier, which in practice is closely approached by the usual half-wave linear envelope detector.

621.396.621:621.396.822 2783

Statistical Criteria for the Detection of Pulsed Carriers in Noise: Part 2—D. Middleton. (*Jour. Appl. Phys.*, vol. 24, pp. 379–391; April 1953.) Specific betting curves are determined for weak signals for the three types of observer considered in part 1 (2782 above) and some approximate curves for the case of strong signals are included. The input signal/noise (power) ratio corresponding to the minimum detectable signal at the output, with an arbitrary probability of a correct decision, is found to vary as $n^{-\frac{1}{2}}$ for weak signals and as n^{-1} for strong signals, n being the number of pulses integrated. Comparison of the three types of observer, on the basis of the minimum detectable signal and the approximate distribution of sample size, favors the Neyman-Pearson type.

621.396.621:621.396.822 2784

RC Memory Commutator for Signal-to-Noise Improvement—C. I. Beard and E. N. Skomal. (*Rev. Sci. Instr.*, vol. 24, pp. 276–280; April 1953.) Description of a simple electromechanical device for detecting and displaying, with only a short time delay, periodic signals of frequency 1–10 cps received in the presence of noise of amplitude up to 100 times that of the signal. The signal is chopped by applying it through a resistor and rotating brush to successive capacitors arranged round the commutator, and the average value over the charging interval is stored and displayed on an oscilloscope. A rejection ratio of 85:1 for 60 cps interference has been achieved.

STATIONS AND COMMUNICATION SYSTEMS

621.39:06.04(100) 2785

International Organization of Radio Communications and the World Problem of Frequency Allocation—L. Bramel de Clejoulx. (*Onde élect.*, vol. 33, pp. 77–84; Feb. 1953.) The organization of the International Telecommunications Union is described and the functions of its component bodies, in particular the International Frequency Registration Board, are defined with reference to the decisions of the 1947 Atlantic City Conference. Subsequent conferences and the operation of this Board are reviewed.

621.39.001.11:621.396.619 2786

A Comparison of the Informational Capacities of Amplitude- and Phase-Modulation Communication Systems—N. M. Blachman. (PROC. I.R.E., vol. 41, pp. 748–759; July 1953.) Calculations indicate that the capacity of a channel as given by Shannon (1649 of 1949) is fully realized only if AM and PHM are used simultaneously, both at transmitter and receiver. For very high signal/noise ratios, AM and PHM alone each account for half the channel capacity. For signal/noise ratios $\ll 1$, PHM alone provides 79% and AM no more than about 17% of the full capacity; but if the receiver responds to both AM and PHM the full capacity is effective whatever the type of transmitter. An AM signal received on a PHM receiver at low signal/noise ratio can convey as much information as a PHM signal; but for large signal/noise ratios the information capacity of this system is of a smaller order of magnitude than that of the other systems.

621.395.828:629.135 2787

Noise Reduction in Intercom Systems—R. J. Stahl and G. A. Walters. (*Electronics*, vol. 26, pp. 214–222; June 1953.)

621.396.41:621.3.018.78 2788

Reducing Distortion in Microwave Systems—W. L. Firestone and J. S. Byrne. (*Electronics*, vol. 26, pp. 184–188; June 1953.) Analysis of second-, third- and fourth-order distortion terms shows that limiting the applied peak-to-peak voltage, maintaining the individual channels voltages equal in magnitude, and restricting the frequency spectrum to one octave, reduces distortion in frequency-division multiplex systems. Measurements made on a 24-channel system support the theoretical results.

621.396.61.029.64:621.396.8 2789

Physical and Technical Bases for the Planning of U.S.W. Transmitters—W. Nestel and E. Schwartz. (*Funk u. Ton*, vol. 7, pp. 165–178; April 1953.) The laws governing the propagation of uhf waves over land and sea paths are discussed and atmospheric effects on the field strengths obtainable at a distance from an usw transmitter are considered. The problem of obtaining adequate coverage over a large area by means of a system of common-wave transmitters is discussed, and curves are given showing the coverage to be expected in the case of transmitter powers of 1kW-1MW, with adequate signals for 99% and for 90% of the time. 26 references.

621.396.619 2790

A Generalization of Modulation Spectra—H. Chang and V. C. Rideout. (*Quart. Appl. Math.*, vol. 11, pp. 87–100; April 1953.) Theory applicable to both AM and FM is developed. The modulation products are shown to be harmonics of the highest common factor of the carrier and modulation frequencies. Fourier analysis is used where there is an integral relation between carrier and modulation frequencies; where this relation does not hold, Bohr's method for nearly periodic functions is applicable.

621.396.619:621.396.65 2791

Comparison of the Principal Methods of Modulation for Directional Radio Links, taking account of Recent Developments—H. Holzwarth. (*Arch. elekt. Übertragung*, vol. 7, pp. 213–222; May 1953.) Various modulation methods are discussed with particular reference to the signal/noise ratios obtainable and to crosstalk and distortion characteristics. The discussion indicates that the following methods are about equally good for links with many channels: PCM and PPM with AM of the HF carrier; SSB and PAM with FM of the HF carrier. For links with fewer channels (up to about 24), the second of each of these pairs, namely, PPM-AM and PAM-FM, is about 10 db the better as regards noise.

621.396.65:621.385.029.6 2792

The Travelling-Wave Tube as Output Amplifier in Centimetre-Wave Radio Links—D. C. Rogers. (*See* 2829.)

621.396.71:621.396.5(45) 2793

The New Radiotelephony Terminals of the Centro Radio Nazionale P.T.—G. Bronzi. (*Poste e Telecomun.*, vol. 21, pp. 107–115; March 1953.) Description of the circuits in use at the transmitting and receiving stations at Prato Smeraldo and Tor San Giovanni. The equipment includes VOGAD (voice-operated gain adjustment) and VODAS (voice-operated device anti-singing) arrangements, whose action is explained.

621.396.721 2794

Ferroxcube + Westectal = Simultaneous Translation—E. Aisberg. (*Toute la Radio*, vol. 20, pp. 58–60; Feb. 1953.) To make translations available to delegates at the Palais de Chaillot, two 5-w transmitters radiate on 300 kc (French) and 400 kc (English) from two parallel metal strips along the walls of the conference room. Pocket receivers comprise a 1850-μH ferroxcube coil and Ge crystal detector operating into headphones, and can be switched simply to the required channel.

621.39.001.11 2795

Information Theory and its Engineering Applications [Book Review]—D. A. Bell. Publishers: Pitman & Sons, London. (*Wireless Eng.*, vol. 30, pp. 182–183; July 1953.) Developments in the theory published since 1948 are presented; the mathematics used is "within the range associated with an honours degree in electrical engineering or physics."

SUBSIDIARY APPARATUS

621.3.013.783 2796

Development of an Absorber for Electromagnetic Waves—R. Müller. (*Arch. elekt. Übertragung*, vol. 7, pp. 223–229; May 1953.) Theory is given relative to the design of mesh networks suitable for screening electrical equipment from em radiation within a specified frequency band.

621.311.6:621.314.7 2797

Power Requirements for Transistor Circuits—J. Dalfonso. (*Electronics*, vol. 26, pp. 204–214; June 1953.) Primary requirement for transistor power supply is constancy of voltage or current with time. Long life and small size are next in importance. These requirements are all satisfied by RM HgO cells (Clune, 2048 of 1952.)

621.311.6.027.3:[621.397.62+621.317.755 2798

High-Voltage Generation for Television Equipment and Oscillographs—H. Lennartz. (*Funk u. Ton*, vol. 7, pp. 179–191; April 1953.) A review of various methods described in the literature on the subject.

621.311.62:621.314.6 2799

Effective Current and Efficiency of Small Mains Supply Units with Capacitively Terminated Rectifiers—H. Schweitzer. (*Funk u. Ton*, vol. 7, pp. 192–198; April 1953.) When a mains transformer is wholly or partially loaded by a capacitively terminated rectifier network, the effective value of the rectifier current pulses is determinative for the copper losses, and the wave form distortion for the magnetic losses. Effective-current and efficiency curves are presented for various simple types of rectifier circuit.

621.311.62:621.314.67:621.316.722.1 2800

A Stabilized Extra-High-Tension Rectifier for 5000 V, 50 mA—P. Perilhou and J. Cayzac. (*Philips Tech. Rev.*, vol. 14, pp. 190–199; Jan. 1953.) Description of equipment using a triode control valve which functions as a variable resistor in the dc circuit. The 300-v reference voltage is provided by a dry battery. The output-voltage fluctuations are only 1/3000th of those of the mains supply. The output voltage is variable between 900 and 5100-v in four overlapping 1200-v stages, each subdivided into 200-v steps which can be varied continuously. Protective measures are described.

621.314.64.011.21 2801

Impedances of the Electrolytical Rectifier—J. W. A. Scholte and W. C. van Geel. (*Philips Res. Rep.*, vol. 8, pp. 47–72; Feb. 1953.) The impedance characteristic of an Al-Al_2O_3-electrolyte rectifier is investigated experimentally. A method for calculating an equivalent circuit of the oxide layer from the frequency dependence of its impedance is described. It is concluded that rectification occurs by means of contact between p-type and n-type semiconducting layers.

621.316.722.1 2802

Voltage Stabilization with Series Valve Control—R. D. Trigg. (*Elec. Eng.*, vol. 25, pp. 254–256; June 1953.) Analysis of the operation of equipment taking a large load current.

621.316.722.1:621.387 2803

Corona Discharge Tubes for Voltage Stabilization—A. M. Andrew: E. E. Shelton and F. Wade. (*Elec. Eng.*, vol. 25, p. 263; June 1953.) Comment on 1136 of April and authors' reply.

TELEVISION AND PHOTOTELEGRAPHY

621.397.24/.26 2804

[Coronation] Television Arrangements—T. H. Bridgewater. (*Wireless World*, vol. 59, pp. 317–319; July 1953.) Vision and sound signals from the five mobile control rooms disposed along the processional route, including that at Westminster Abbey, were brought to a temporary central control room at Broadcasting House. Some details are given of particular camera equipment used, including room lenses, two of which were of the Watson type with interchangeable back elements giving a choice of two 5:1 magnification ranges with angles of view of 3°–15° and 6°–30°, another new design, due to Taylor, Taylor and Hobson, having a range of 5°–25°. Another special lens, the Dallmeyer 40-inch double-folded telephoto lens, was used with an image orthicon for close views of the Royal Family during their appearances on the balcony at Buckingham Palace. This lens has a viewing angle of under 2°.

The use of the new BBC derivative equalizers (Gourier, 1936 of July) gave a noticeable enhancement of picture definition. The pictures relayed to France, Holland and Western Germany were the same as those broadcast in Britain, but commentaries in the different languages were provided, French commentators being stationed alongside the British at several of the main camera positions and using independent microphones connected to a separate control point. Five cm-wave links were operated between London and Cassel (France), a special feature being the use of space-diversity reception with two parabolic antenna systems, one about 15 feet above the other, to obtain fading-free reception.

621.397.5:535.623 2805

Note on the Channel Required for Colour-Television Transmission—É. Labin. (*Onde élect.*, vol. 33, pp. 85–92; Feb. 1953.) Basic formulas of information theory relating channel capacity, bandwidth, power and noise level are applied to determine the bandwidth required for transmission of monochrome signals. This bandwidth is compared with that required for a color system. The alternatives to a much increased bandwidth are discussed, with particular reference to the RCA dot-interlacing system.

621.397.5:535.767 2806

Stereoscopic Television—(*Wireless World*, vol. 59, pp. 296–298; July 1953.) Discussion of the practicability of a system using a slotted mask a little distance in front of the cr tube screen, so that a viewer's left eye sees only one set of interlaced images on the screen while the other set is visible only to the right eye.

621.397.611:535.623 2807

Measurement and Control of the Color Characteristics of a Flying-Spot Color-Signal Generator—R. C. Moore, J. F. Fisher and J. B. Chatten. (Proc. I.R.E., vol. 41, pp. 730–733; July 1953.) The particular color characteristics required to suit the NTSC system are indicated; since these have negative lobes, the required result is obtained in practice by finding an equivalent combination of characteristics without negative lobes. For this purpose, the color characteristics of the flying-spot signal generator are determined by passing its light output through a system of splitters to a set of photocells whose output is measured electrically; appropriate correcting color filters are then inserted in the respective paths.

621.397.611.2 2808

The French Origin of the Image-Orthicon Target—R. Barthélemy. (*Électronique (Paris)*, no. 75, pp. 37–41; Feb. 1953.) Experiments on thin-film targets carried out in 1930 are noted and the process of charge transfer in thin slightly conducting targets is analyzed by considering an equivalent CR network and the current-density distribution in the target. The optimum ratio of target thickness to beam diameter is discussed. See also 1755 of 1952 and back reference.

621.397.62 2809

A 427/45-Mc/s Converter for the Society's Television Transmissions—D. N. Corfield. (*Jour. Telev. Soc.*, vol. 7, pp. 19–27; Jan./March, 1953.) The converter comprises two units: (a) mixer, amplifier and oscillator circuits; (b) power supply unit. Reception is possible between 420 and 450 mc; the tuning range for a 45-mc output is 425–436 mc. Full circuit details are given, including the specification and arrangement of components. Alignment procedure is described and details of the dimensions and construction of 3 types of antenna suitable for the reception of 427-mc signals are shown.

621.397.62 2810

Modernizing the *Wireless World* Television Receiver—(*Wireless World*, vol. 59, pp. 215–217, 279–284 and 306–310; May–July 1953.) Modifications of the original design (1186 of 1948 and back references) are described, including new frame and timebase units needed for obtaining a picture of adequate brightness on a 12-inch or 15-inch cr tube. A new deflector-coil assembly (Cocking, 574 of February) is also required, these new units necessitating minor alterations in other parts of the equipment. Reprints of the articles describing the original superheterodyne receiver are still available from Iliffe & Sons, Ltd.

621.397.62:535.88 2811

The Design of a Large-Screen Receiver—P. D. Saw. (*Jour. Telev. Soc.*, vol. 7, pp. 3–11; Jan./March 1953.) The receiver is designed to use a 2.5-inch cr tube and is built on three separate chassis with interconnecting plugs and sockets so that alternative units can be easily substituted. The RF unit is a straight SSB receiver. Circuit details and descriptions of the timebase and power-supply units are given. Different front-projection arrangements for 20, 30, 40 and 50-inch screens are described and developments in the design of projection screens are discussed.

621.397.62+621.317.755]:621.311.6.027.3 2812

High-Voltage Generation for Television Equipment and Oscillographs—H. Lennartz. (*Funk u. Ton*, vol. 7, pp. 179–191; April 1953.) A review of various methods described in the literature on the subject.

621.397.62:621.314.7 2813

A Study of Transistor Circuits for Television—G. C. Sziklai, R. D. Lohman and G. B. Herzog. (Proc. I.R.E., vol. 41, pp. 708–717; July 1953.) The use of transistors in television receivers was studied, using an experimental battery-operated set including 37 transistors and a 5-inch kinescope housed in a cabinet 13×12×7 inches, with self-contained loop antenna. The various stages are described in detail; both point-contact and junction-type transistors are used. The design of several of the circuits makes use of the symmetrical properties of transistors discussed in 2583 above.

621.397.621 2814

A Single-Valve Line Timebase—J. Greenhalgh. (*Jour. Telev. Soc.*, vol. 7, pp. 12–18;

Jan./March 1953.) The operation of a self-running timebase circuit is explained and methods of ensuring effective control of scan amplitude, good linearity and satisfactory fly-back voltage are described. "Shadowing" due to spurious deflection of the beam may be eliminated by use of a dc component in the scan coils.

621.397.9 2815

A Survey of Some Applications of Television in Industry, Scientific Research and Education—J. E. Telfer. (*AWA Tech. Rev.*, vol. 9, pp. 173–207; Jan. 1953.) Reprint. Original noted in 1512 of May.

TRANSMISSION

621.396.61:621.316.726 2816

Synchronization of a Variable-Frequency Oscillator at Discrete, Stabilized Frequencies with the E80T Tube—J. Bruijsten, H. Groendijk and M. R. Mantz. (*Elec. Appl. Bull.*, vol. 13, pp. 169–174; Nov./Dec. 1952.) (*See* 2817 below.)

621.396.61:621.385.83 2817

Simplification of Multi-channel V.H.F. and U.H.F., I.G.O.-Circuits by the Use of the Phase-Discriminator Valve, Type E80T—J. Bruijsten, H. Groendijk and M. R. Mantz. (*Commun. News*, vol. 13, pp. 13–20; Feb. 1953.) A simplified IGO circuit (Hugenholtz, 767 of 1951) is described based on use of the specially developed Type-E80T beam-deflection tube. This combines the functions of pulse generator and phase discriminator, making possible the direct synchronization of oscillators operating in the vhf and uhf bands and enabling frequency-multiplication factors as high as 100 to be used. Both the electrical design of the tube and its constructional requirements for use in mobile installations are discussed.

621.396.61:621.396.932 2818

Modern Transmitting Equipment for Mercantile-Marine Vessels—L. 't Hart and C. Strässer. (*Commun. News*, vol. 13, pp. 50–60; April 1953.) Equipment for A_1 or A_2 radiotelegraphy is described comprising crystal-controlled 30-channel HF (4–22 mc) and 10-channel MF (405–535 kc) transmitters with common power-supply unit using a dc/ac converter, and an emergency MF transmitter with auto-oscillator, fed from a 24-v battery.

621.396.61.029.55:621.396.712 2819

A 100-kW Short-Wave Broadcast Transmitter—A. G. Robeer. (*Commun. News*, vol. 13, pp. 22–40; Feb. 1953.) This transmitter is designed on the same general principles as the 40-kw transmitter previously described (Robeer and Swets, 1461 of 1952), the most important modification being the use of two water-cooled tubes in the penultimate stage.

621.396.619.23:621.396.619.13 2820

Fundamentals of Frequency Modulation by means of Reactance Units—H. Fick. (*Funk u. Ton*, vol. 7, pp. 199–204; April 1953.) Formulas are derived for the parameters of various simple types of reactance unit and for the frequency swing obtained.

TUBES AND THERMIONICS

621.314.7+621.314.632 2821

Theory of the Germanium Rectifier and the Transistor—H. Krömer. (*Z. Phys.*, vol. 134, pp. 435–450; March 25, 1953.) Expressions are derived for the charge density in the boundary layers of a metal/semiconductor junction in a strong field. The carrier density is found to increase proportionally to field strength and current density; the boundary-layer potential deviates appreciably from the simple Schottky parabolic form. The corrected potential is used to calculate Ge-transistor and Ge-diode characteristic curves.

621.314.7:546.28 2822

Some Properties of Silicon Point-Contact Transistors—J. W. Granville and W. Bardsley. (*Proc. Phys. Soc.*, vol. 66, p. 429; May 1, 1953.) Preliminary report on Si transistors giving a voltage gain at 90°C about 50% of that at room temperature, with a fall to 20% at 150°C, the current gain remaining substantially constant over this temperature range. High-resistivity *p*-type Si is used, with phosphor-bronze or tungsten probes about 0.002 inches apart.

621.314.7:546.28 2823

On the Transistor Action of Silicon Crystals—Y. Kanai. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 435–436; July/Aug. 1952.) Characteristics measured for transistors made from *p*-type Si differed from those obtained by Bardeen and Brattain (2979 of 1949) for Ge transistors, in that collector voltage, was not a double-valued function of collector current for a given value of emitter current. Results are analyzed using Hunter's method (1311 of 1950) with appropriate modifications.

621.383.2:537.311.33 2824

On the Composition of Antimony-Caesium Photocathode—H. Miyazawa, K. Noga, S. Chikazumi and A. Kobayashi. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 647–649; Nov./Dec. 1952.) Report of an experimental investigation of the effect on the photoelectric emission, the conductivity and the Cs-vapor pressure of varying the concentration of Cs in the Sb layers. The high photoelectric sensitivity of the semiconducting compound Cs_3Sb is ascribed to its electron structure.

621.383.5:546.289 2825

The Properties of Germanium Phototransistors—J. N. Shive. (*Jour. Opt. Soc. Amer.*, vol. 43, pp. 239–244; April 1953.) The point-contact, *p-n*-junction and *n-p-n*-junction types of phototransistor are described and compared. The point-contact type has a high value of dark current and a yield of 3 or 4 electrons per quantum. The *p-n* type has a dark current of the order of microamperes and a quantum yield of about unity. The *n-p-n* type has a yield which may be as high as several hundred electrons per quantum. All three types have long-wave thresholds around 1.8 μ.

621.385.029.6 2826

Characteristics of the Travelling-Wave Valve in the Dispersive Region of its Delay Line—W. Klein and W. Friz. (*Arch. elekt. Übertragung*, vol. 7, pp. 236–248; May 1953.) Analysis is presented in which the traveling-wave tube, together with its input and output circuits, is treated as an active quadripole. The transfer coefficient is discussed as regards both magnitude and phase, and the effect of the helix dispersion on the amplification bandwidth is investigated. The way in which amplification and group delay are affected by mismatch at input and output is discussed and means of reducing the effect are described. The frequency dependence of the phase constant and of the group delay for the active case is different from that for the passive helix. The results of the analysis enable traveling-wave tubes to be designed with optimum amplification, bandwidth and group delay.

621.385.029.6 2827

Magnetic Electron Optics in Long-Beam Amplifier Valves—M. Müller. (*Telefunken Ztg.*, vol. 26, pp. 95–101; March 1953.) Principles of design of traveling-wave tubes are discussed. Methods of screening the electron gun and of calculating the required field intensity are outlined. The lens effect of the transition zone and the effects of space charge are considered. The plane in which the beam diameter is a minimum with no field applied should coincide with the plane in which the applied field reaches 70% of its full intensity.

621.385.029.6:621.392.22 2828

High-Power Delay Line for a Traveling-Wave Amplifier or Oscillator—J. F. Hull, G Novick and B. D. Kumpfer. (*Proc. NEC* (*Chicago*), vol. 8, pp. 313–320; 1952.) Analysis is presented for a delay line similar to that considered by Fletcher (3275 of 1952), with interleaved sets of fingers projecting from the wider walls of a rectangular waveguide, a ribbon beam being directed along the sides of the fingers or a round beam sent through holes in the fingers. An accurate expression is derived for the line impedance and for the guide wavelength. The breaking-up of the fields between the teeth into an infinite number of Hartree space harmonics is discussed. For each order of space harmonic there are two phase velocities in opposite directions. The desirable characteristics of delay lines for either space-harmonic amplifiers or backward-wave oscillators are discussed. Experimental results confirm the theory.

621.385.029.6:621.396.65 2829

The Travelling-Wave Tube as Output Amplifier in Centimetre-Wave Radio Links—D. C. Rogers. (*Proc. IEE*, Part III, vol. 100, pp. 151–156; May 1953.) The requirements for the output amplifier at the relay stations of a FM 4-kmc radio link are discussed and the relative merits of klystron, disk-seal triode, and traveling-wave tubes for this service are considered. Details are given of the construction, operating conditions and performance of the Type-CV2188 traveling-wave tube which is used at the relay stations of the Manchester-Edinburgh television link as output amplifier. With an input signal power of 25 mw from a Ge crystal mixer, the tube delivers about 1.5-w to the antenna. Improvements to effect still better performance are being investigated.

621.385.029.6:621.396.65 2830

British TV Relay uses Traveling-Wave Tubes—D. C. Rogers and P. F. C. Burke. (*Electronics*, vol. 26, pp. 156–160; June 1953.) (*See* 2829 above.)

621.385.029.64 2831

A Space-Harmonic Traveling-Wave Amplifier—P. M. Lalley. (*Proc. NEC* (*Chicago*), vol. 8, pp. 73–80; 1952.) Spatial harmonics obtained in the case of a wave traveling along a periodically loaded waveguide structure are discussed, mathematical theory being given in an appendix. The design is described of an amplifier tube for the range 4–6 kmc. This uses a waveguide loading structure consisting of teeth projecting inwards from opposite walls of the waveguide, the teeth being tapered down for a length of 1 inch at each end of the tube. With a normal beam current, oscillations could be obtained at nearly all beam voltages >200-v. Such tubes can be used as electrically tunable filters or oscillators, the frequency varying with beam voltage. See also 547 of 1952 (Millman).

621.385.032.21:537.583 2832

A Survey of Present Knowledge of Thermionic Emitters—D. A. Wright. (*Proc. IEE*, Part III, vol. 100, pp. 125–139; May 1953.) Discussion, pp. 140–142.) Factors affecting the work function of metals are discussed, the work functions of the elements are tabulated and the effects of adsorbed films are considered particularly for emitters with monatomic layers of Th, Cs or Ba. The omission from compounds, especially from semiconductors, is described. Difficulties in the way of using the emissive properties of certain metallic borides and carbides are noted LaB_6 and ThC_2 are likely to be valuable as practical emitters. The general properties of oxides are discussed, a table of work-function data being given for the oxides of metals in the first four groups. The properties of the (Ba, Sr)O cathode are discussed in detail and the performance of thoria as an emitter is described. 70 references.

621.385.032.216 2833

Investigations on Oxide Cathodes with a Resistive Interface Layer—A. P. Weber. (*Tele-*

funken Ztg., vol. 26, pp. 123–127; March 1953.) By means of a special microscope technique, tightly adhering vitreous crusts have been discovered on the cathode core in cathodes which have developed an interface resistance; their average thickness is 3μ. The general roughening of the cathode core is not connected with the resistive layer.

621.385.032.216 2834

Dissociation of Oxide-Coated by Primary Electron Bombardment—S. Yoshida, I. Takeda and H. Arata. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 430–431; July/Aug. 1952.) An experimental investigation leads to a value of 10.5 ev for the energy of dissociation of solid-state BaO.

621.385.032.216:537.311.3 2835

A Retarding-Potential Method for Measuring Electrical Conductivity of Oxide-Coated Cathodes—I. L. Sparks and H. R. Philipp. (*Jour. Appl. Phys.*, vol. 24, pp. 453–461; April 1953.) The method described cannot be used at very low temperatures or for coatings with a conductivity thermionic-emission ratio >2 cm/v. It can, however, be used for coatings in a normal state for thermionic emission, as probes or other devices which might impair emission are not used, and conductivity and thermionic emission measurements can be made simultaneously. Results obtained for BaO and (BaSr)O coatings are given.

621.385.032.216:537.533.8 2836

Secondafy Electron Emission from Oxide-Coated Cathode—S. Yoshida and I. Takeda. (*Jour. Phys. Soc.* (*Japan*), vol. 7, pp. 639–640; Nov./Dec. 1952.) An experimental investigation is made of the variation of the secondary-emission ratio due to (a) formation of excess Ba when the BaO suffers dissociation as a result of electron bombardment (*See* 2834 above), (b) variation of primary-electron-current density and (c) variation of temperature.

621.385.032.216:537.583:537.533.1 2837

The Velocity Distribution of Electrons of Thermionic Emitters under Pulsed Operation: Part 1—Apparatus and Measuring Technique—C. G. J. Jansen and R. Loosjes. (*Philips Res. Rep.*, vol. 8, pp. 21–34; Feb. 1953.) The construction of a tube for determining the electron velocity distribution, particularly of oxide coatings at high current densities, is described. Electron-velocity measurements are accurate to within ~1%. Complete i/v characteristics of an emitting surface of area $8 mm^2$, and points on the characteristics of the small portions (0.03 mm^2) whose velocity spectra are observed, can be determined by pulse methods. Typical (BaSr)O, BaO, and SrO velocity spectra are shown. Using tubes with L cathodes, peak voltages can be determined to within $\pm v$.

621.385.032.216:621.317.332 2838

The Dependence of Mutual Conductance on Frequency of Aged Oxide-Cathode Valves and its Influence on their Transient Response—J. R. Tillman, J. Butterworth and R. E. Warren. (*Proc. IEE*, Part III, vol. 100, pp. 175–176; May 1953.) Digest only. The interface-layer impedance, represented as a parallel RC combination, is determined from measurements of the apparent mutual conductance at three frequencies, the first so high that C renders the interface impedance negligible, the second so low that only R is important, the third at an intermediate frequency. The values of R and C can then be determined. A diagram of the test circuit is given. Measurements on some aged HF pentodes show that the interface impedance is frequency dependent. This is confirmed by the results of measurements of the transient responses of the tubes. A more complex network may be needed to represent interface impedance. (*See* also 2839 below.)

621.385.032.216:621.317.332 2839

A Simple Method for Measuring Interface Impedance—A. van der Ziel. (*Jour. Appl. Phys.*, vol. 24, p. 496; April 1953.) The method described is an adaptation of that used by Strutt and van der Ziel (3211 of 1938). The components of a variable impedance, connected between grid and anode of the tube under test, which is connected as an amplifier, are successively adjusted to obtain zero output (a) at 5 mc, (b) at 1 kc, (c) from a wide-band receiver connected across the load resistor. The values of the components then give the tube transconductance and the resistance and parallel capacitance of the cathode-interface layer.

621.385.032.216.1:546.841.4–31 2840

Contribution to the Study of Thoria Cathodes—G. Mesnard. (*Jour. Phys. Rad.*, vol. 14, pp. 179–191; March 1953.) Résumé of a thesis. (*See* 2506–2508 of August and back references.)

621.385.026.445 2841

High-Power Transmitting Valves with Thoriated-Tungsten Cathodes—E. G. Dorgelo. (*Philips Tech. Rev.*, vol. 14, pp. 226–234; Feb. 1953.) A description is given of two models of a new transmitting triode, Types TBW 12/100 and TBL 12/100, the former with water cooling and the latter with forced-air cooling. Thoriated-tungsten filaments are used, three specially prepared Zr getters ensuring the necessary very high vacuum. Power consumption in the filaments is 3.5 kw and maximum output power 105 kw for telegraphy, 65 kw for telephony, with an efficiency of 80% at frequencies up to 30 mc and 60% at 68 mc.

621.385.83:[537.291+538.691 2842

Electron-Beam Deflection Systems and their Aberrations. Dynamic Systems Symmetrical in Two Planes—G. Wendt. (*Onde élect.*, vol. 33, pp. 93–106; Feb. 1953.) Different systems are classified. The chief factors governing uniformity in dynamic systems, i.e., when the deflection field is variable, are angle of deflection, principal plane of deflection, and deflecting power; these are defined. Distortion, astigmatism, curvature of field and coma are third-order aberrations. Their dependence on beam width and deflection angle is discussed and methods of eliminating them are noted. Detailed mathematical treatment of field equations is given in an appendix.

621.385.831 2843

The E80T Beam Deflection Tube—(*Elec. Appl. Bull.*, vol. 13, pp. 175–177; Nov./Dec. 1952.) Details are given of the construction and characteristics of this ribbon-beam tube. (*See* also 2816 above.)

621.385.83:621.396.61 2844

Simplification of Multi-channel V.H.F. and U.H.F. I.G.O.-Circuits by the Use of the Phase-Discriminator Valve, Type E80T—J. Bruijsten, H. Groendijk and M. R. Mantz. (*See* 2817.)

621.385.832 2845

Development of an Improved Graphechon Storage Tube—W. T. Dyall, G. R. Fadner and M. D. Harsh. (*Proc. NEC* (*Chicago*), vol. 8, pp. 535–542; 1952.) See 1539 of May.

621.385.832:537.563 2846

Positive and Negative Ions in Cathode-Ray Tubes—C. H. Bachman, G. L. Hall and P. A. Silberg. (*Jour. Appl. Phys.*, vol. 24, pp. 427–433; April 1953.) Ion formation in cr tubes has a deleterious effect. Investigations show that the greatest offender is hydrogen, which forms both positive and negative ions. Other ions identified are C^+, C^-, O^+, O^-, $C_2H_2^-$, CO^+. Aluminized screens were found to afford little protection to the ion-bombarded phosphor.

621.396.615.141.2 2847

Application of the Thermodynamics of Irreversible Processes to the Theory of the Magnetron—P. A. Lindsay and G. D. Sims. (*Proc. Phys. Soc.*, vol. 66, pp. 423–425; May 1, 1953.) Discussion of the possibility of building a satisfactory theory of magnetron conduction and oscillations on the foundation of Onsager's thermodynamics of irreversible processes.

621.396.615.141.2 2848

Calculation of a Waveguide-Loaded Resonator for Interdigital Magnetrons—G. Hok. (Proc. I.R.E., vol. 41, pp. 763–769; July 1953.) The electromagnetic-field configuration in the various parts of the resonator is considered, as well as the boundary relations at the junction between them. The result is used to relate resonance frequency and Q to the geometry and to design the output transformer so that the desired slot conductance is obtained for the electronic operation of the magnetron.

621.396.615.141.2 2849

Inverted Magnetron—F. Lüdi. (Proc. I.R.E., vol. 41, p. 799; July 1953.) Comment on paper noted in 3621 of 1952 (Hull), with reference to numerous previous publications by the author dealing with the planar magnetron, this form being closely approached by the single-cavity magnetron known as the "turbator" (2518 of Aug. and back references).

621.396.615.141.2:621.365.55† 2850

Tubes for Dielectric Heating at 915 Mc/s—R. B. Nelson. (*Trans. Amer. IEE*, vol. 71, part I, pp. 72–80; 1952.) For a shorter account see 3292 of 1952.

621.396.615.141.2(091) 2851

Genesis of a Generator—The Early History of the Magnetron—R. L. Wathen. (*Jour. Frank. Inst.*, vol. 255, pp. 271–287; April 1953.) Early types are noted and a detailed account is given of the development in England by Boot and Randall of the multicavity magnetron, and of the improvements, such as Sayers' method of segment strapping for mode suppression, which resulted in the practical designs which contributed so largely to the efficiency of wartime radar equipment. Developments in the United States since 1940, when information on the British design was disclosed, are not considered, as they have been well covered by Collins (588 of 1949) and by Fisk et al. (293 of 1947). See also 891 (Megaw) and 892 (Willshaw et al.) of 1948.

621.396.615 141.2(43) 2852

The State of Magnetron Development in Germany—K. Fritz. (*Funk u. Ton*, vol. 7, pp. 133–138; March 1953.) Brief descriptions are given of typical magnetrons, including one with a cw output of 1 kw on a wavelength of 12.5 cm and an efficiency $>50\%$.

621.396.615.142.2 2853

Design Features of a New 14.5–17.5-kMc/s Reflex Klystron—G. C. Dalman. (*Proc. NEC* (*Chicago*), vol. 8, pp. 50–55; 1952.) Description of a mechanically tuned tube, Type SRU-55, which is designed for direct connection to a standard 0.622+0.311-inch waveguide without insertion of a transformer section. Minimum output throughout the range with 300-v beam voltage, is 20 mw, over 100 mw being given in parts of the range.

MISCELLANEOUS

621.396+621.396.9 2854

Radio and Radar Technique. [Book Review]—A. T. Starr. Publishers: Pitman and Sons, *London*. (*Wireless Eng.*, vol. 30, p. 182; July 1953.) A concise account of the essentials; the reader is assumed to have a knowledge of the subject approaching that of a university degree.

Having the RIGHT CONNECTIONS *is a big help!*

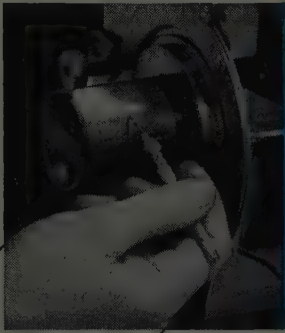
Helipot*... first in precision potentiometers ... makes sure that, in *every* Helipot, you do have the right connections. No pressure-type connections are used in *any* Helipot. Tap connections are spot-welded by a Helipot-developed process, and other electrical connections are soldered ... they all *stay put!*

The spot welding process is a particularly interesting one ... and more important, it offers a very real advantage to users of Helipot precision potentiometers. Skilled workers, using binocular microscopes, employ a new technique in spot welding the very fine electrical connections. This technique assures that tap connections are attached to a single turn *only* of the resistance wire, rather than to several adjacent turns as is usually the case with the conventional method. Thus the high resolution, so important to the proper functioning of a precision potentiometer, is not reduced, and none of the wire turns adjacent to the one tapped are shorted out.

The spot welding process offers the further advantage of providing the strongest possible type of connections ... vibration proof, shock proof, corrosion proof, unaffected by temperature and humidity changes. And to cap the climax, the new process is efficient and economical ... another example of the Helipot policy offering the lowest price consistent with the high quality you expect in Helipot products.

For information about Helipot's complete line of precision potentiometers, call your nearest Helipot representative or write direct!

*T.M. Reg. U.S. Pat. Off.



WRITE FOR YOUR COPY!

Your copy of the HELIPOT Condensed Catalog describing every model of HELIPOT Precision Potentiometers and Duodials is now ready. Please write for it on your company letterhead. Ask for Data File # 160-1006.

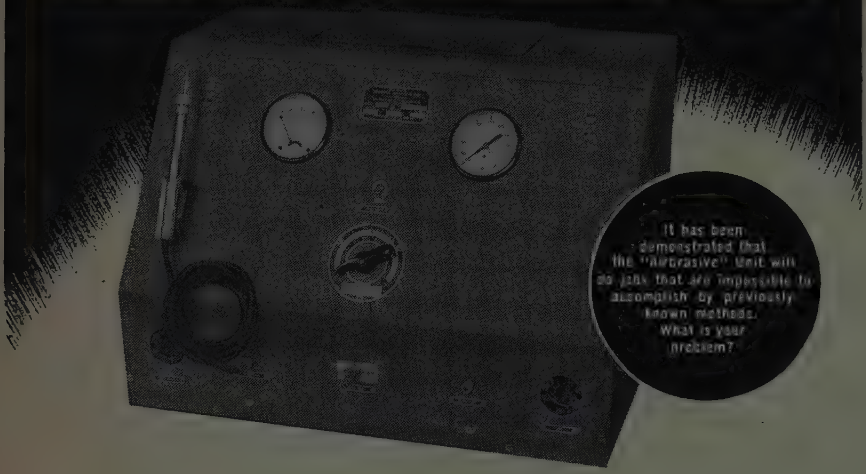
Helipot *corporation*

a division of BECKMAN INSTRUMENTS, INC.
SOUTH PASADENA, CALIFORNIA

PLANTS AT SOUTH PASADENA, CALIFORNIA & MOUNTAINSIDE, NEW JERSEY
ENGINEERING REPRESENTATIVES IN PRINCIPAL CITIES

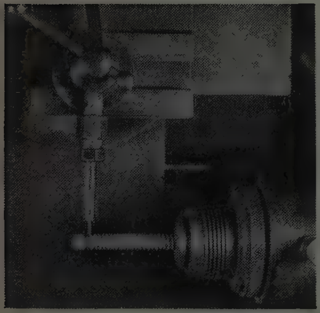
Helipot | *first in precision potentiometers*

THE S. S. WHITE
INDUSTRIAL "AIRBRASIVE" UNIT



It has been demonstrated that the "Airbrasive" Unit will do jobs that are impossible to accomplish by previously known methods. What is your problem?

Ideal for high precision cutting, surface film removal, etching and light deburring



Automatic set-up on a lathe for cutting spiral bands on a deposited carbon resistor.

Cutting a piece of hard, brittle metal manually by means of the "Airbrasive" process.

This remarkably versatile machine can be used for a wide variety of high precision operations from cutting hard, brittle materials to producing fine matte surface finishes.

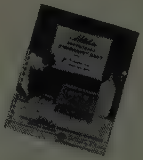
Using a high speed jet of gas-propelled abrasive particles, it can produce cuts as fine as .008" diameter. Its basic advantages are that it cuts cool and without shock or vibration — its accuracy is unaffected by surface irregularities of the work—and it can be accurately regulated for depth and type of cut.

Many manufacturers are now using the Unit to remove surface coatings on deposited carbon resistors and on printed circuits — for light deburring on inside surfaces of tubular parts — drilling fine holes through glass — cutting germanium.

We will be glad to make tests to determine the suitability of the "Airbrasive" Unit to your production requirements. Send us a sample of the part or material as well as details of the job you have in mind. There's no obligation.

WRITE FOR BULLETIN 5307

It has full facts and data on the Airbrasive Unit. It tells you how the "Airbrasive" Unit works and provides information on where, when and how it can be used.



THE S.S. White INDUSTRIAL DIVISION
DENTAL MFG. CO.
Dept. GA, 10 East 40th St.
NEW YORK 16, N. Y.

Western District Office • Times Building, Long Beach, California

Industrial Engineering Notes*

RETMA Activities

Members of RTMA voted to change the Association's name to the Radio-Electronics-Television Manufacturers Association and approved a reorganization plan which will expand the Board of Directors and provide larger representation for new segments of the industry, especially in the advanced electronics field. . . .

Paul V. Galvin of Motorola Inc. has been reappointed Chairman of the RETMA Committee to Survey Subscription Television by Chairman of the Board Robert C. Sprague. During the coming year the committee will continue to study the nontechnical phases of subscription television with particular reference to its possible effects on the telecasting of sports events, theatrical presentations and other events. . . .

Television

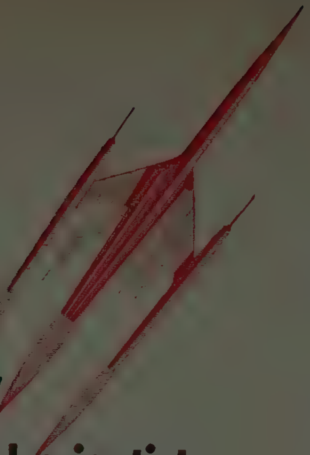
A five-year contract with the University of Notre Dame for presentation of all Notre Dame home football games on closed-circuit theater television starting this fall has been signed, according to an announcement by Milton N. Mound, President of the newly-formed Box Office Television, Inc. Other sporting events planned by the firm include a six-year contract with the Harlem Globetrotters basketball team and possibly a middleweight championship fight this summer and the Marciano-La Starza heavyweight championship fight in September. The company will use AT&T transmission facilities and reportedly has employed RCA to check equipment in subscribing theaters. Theaters equipped for closed-circuit television total 110 in 62 cities, it was announced. . . .

Television service at the beginning of July was a practical reality in 23 foreign countries, two more than at the start of 1953. By the end of this year, it is expected that TV service will be available in six additional foreign countries, according to information made available to RETMA by the Television Development Branch, International Broadcasting Service, Department of State. Of the 23 foreign countries which have TV, 16 have regular service, while in the other seven, it is on an irregular or experimental basis. By the end of 1953, it is estimated that TV service will be available in 29 foreign countries. Expected to be added are Belgium, Chile, Morocco, the Philippine Republic, Thailand, and Yugoslavia. The number of TV sets in use abroad increased from an estimated 2.4 million at the end of 1952 to three million on April 1 of this year. On the latter date the estimated number of viewers was set by the International Broadcasting Service at between 25 and 30 million and it was pointed out that group viewing is well established in a number of countries. . . .

(Continued on page 84A)

---

* The data on which these Notes are based were selected by permission from *Industry Reports* issues of July 17, 24, and 31, and August 7, published by the Radio-Electronics-Television Manufacturers Association, whose helpfulness is gratefully acknowledged.



Six facts every engineer and scientist should know about the new

CRC 102-A

Electronic Digital General-Purpose Computer

1. LOW INITIAL COST—The CRC 102-A is one of the lowest priced, large scale, digital electronic computers now available commercially. It may be purchased, rented, or leased with an option to buy. Performance guarantees are given as part of every lease contract.

2. FAST AVAILABILITY—Applying production-line techniques to the construction of the CRC 102-A has resulted in the shortest delivery time of any fully electronic, digital, general-purpose computer. Production schedules call for completion of one CRC 102-A every eight working days.

3. WIDE CHOICE OF INPUT-OUTPUT DEVICES—Data in either octal or decimal form may be entered into the CRC 102-A manually from a typewriter, automatically or semi-automatically from punched paper tape, and automatically from IBM cards or from computer-controlled magnetic-tape units.

The computer will print output data automatically on its typewriter in octal, decimal, or alphabetic form, perforate paper tape in octal or decimal form for reproducing hard copy or for re-entering data into the computer at some later time, punch octal or decimal data on IBM cards for use with punched card equipment, or record data on magnetic tape for later use.

4. HIGH RELIABILITY—The unique circuit design and relatively small number of vacuum tubes and other critical components in the CRC 102-A result in less down time due to machine failure. Complete plug-in circuitry and easily adjusted mechanical components speed up preventive maintenance checks. Each machine undergoes extensive shakedown tests and is operated under actual customer conditions in CRC's Computing Center before delivery to further assure high reliability.

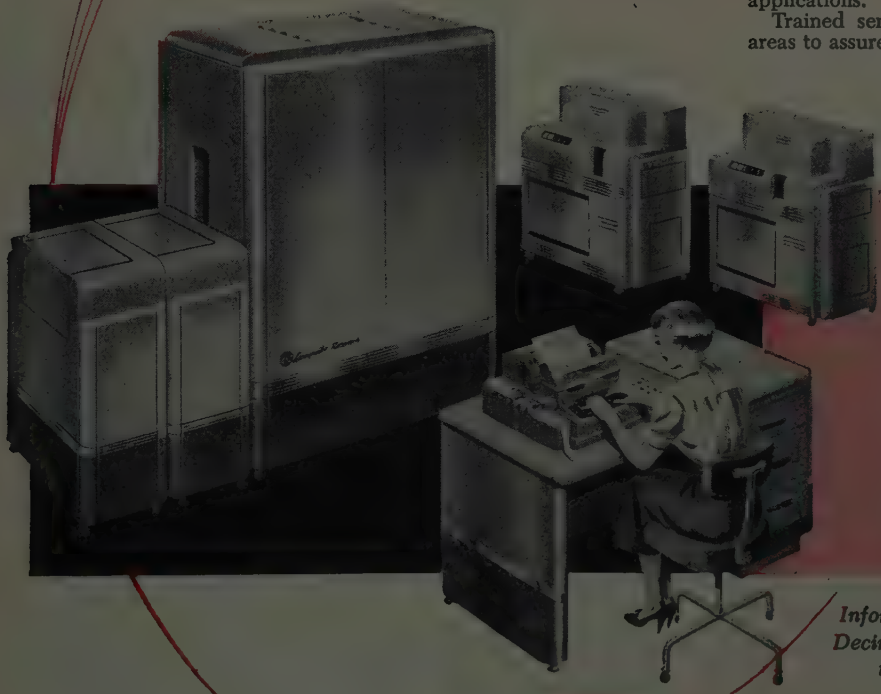
5. EASY PROGRAMMING—Addition of "programmer's" commands, a test switch for program debugging, faster speeds, greater flexibility, and the wide selection of input-output equipment has greatly simplified programming procedures and increased the computer's capabilities.

6. ADDITIONAL SERVICES ARE NOW AVAILABLE—Programming sub-routines, application studies, and training courses on computer operation, are now available from CRC's Applications Division.

Facilities of the new Computing Center enable potential computer users to evaluate the CRC 102-A for their specific applications.

Trained service personnel are now available in most areas to assure proper maintenance of all CRC computers.

For complete, detailed information on the new CRC 102-A write to the Director of Applications.



TYPICAL APPLICATIONS

Wave Propagation Studies
Network Analysis • Antennae Design
Transient Analysis
Electrical Power Distribution
Servo Problems
Solution of Partial Differential Equations
Net Relaxation Problems

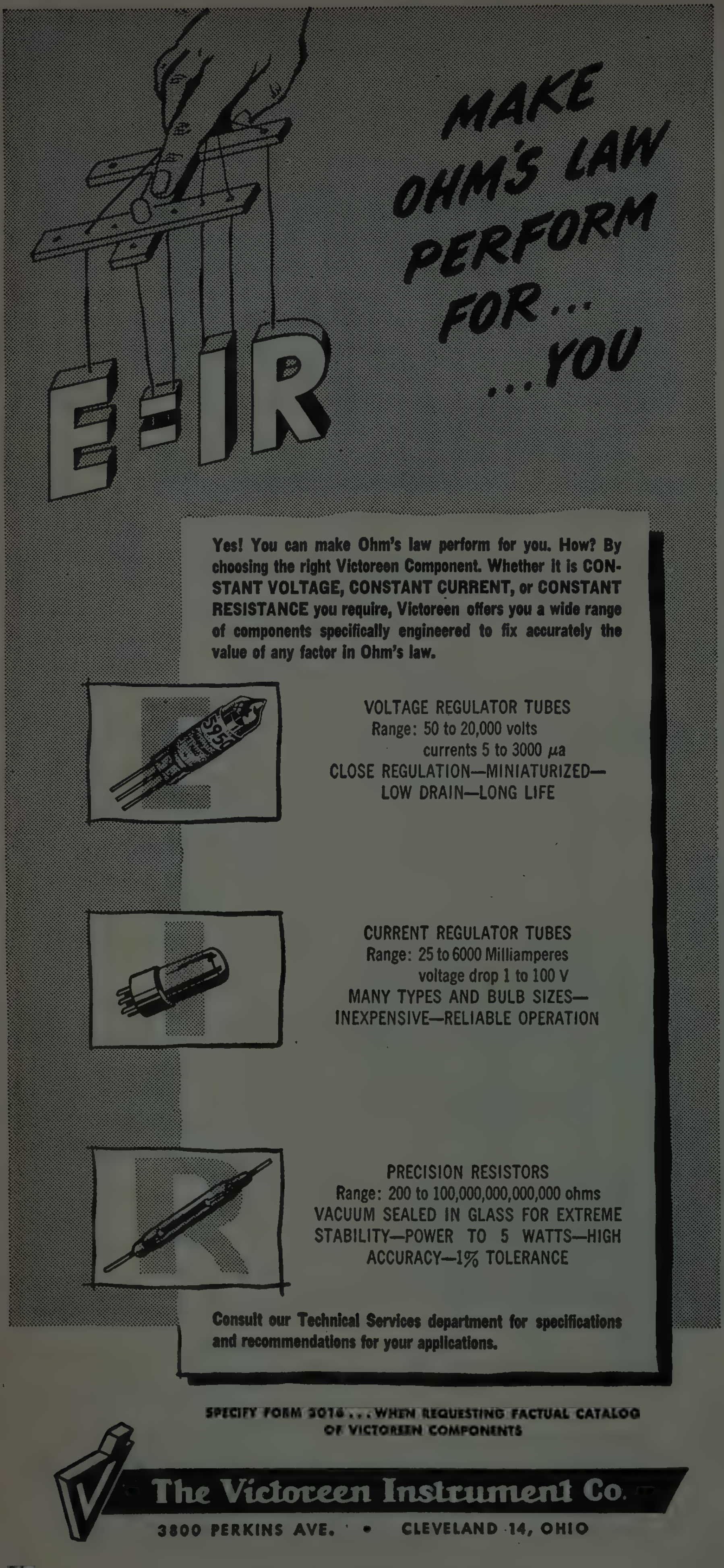
Information is also available on the CRC 105 Decimal Digital Differential Analyzer and the CRC 107 Data Processing Computer.

FIRST IN ELECTRONIC COMPUTATION

CRC

Computer Research
CORPORATION

3348 WEST EL SEGUNDO BLVD., HAWTHORNE, CALIFORNIA



MAKE OHM'S LAW PERFORM FOR... ...YOU
E=IR
5950

Yes! You can make Ohm's law perform for you. How? By choosing the right Victoreen Component. Whether it is CONSTANT VOLTAGE, CONSTANT CURRENT, or CONSTANT RESISTANCE you require, Victoreen offers you a wide range of components specifically engineered to fix accurately the value of any factor in Ohm's law.

VOLTAGE REGULATOR TUBES
Range: 50 to 20,000 volts
currents 5 to 3000 μa
CLOSE REGULATION—MINIATURIZED—
LOW DRAIN—LONG LIFE

CURRENT REGULATOR TUBES
Range: 25 to 6000 Milliamperes
voltage drop 1 to 100 V
MANY TYPES AND BULB SIZES—
INEXPENSIVE—RELIABLE OPERATION

PRECISION RESISTORS
Range: 200 to 100,000,000,000,000 ohms
VACUUM SEALED IN GLASS FOR EXTREME STABILITY—POWER TO 5 WATTS—HIGH ACCURACY—1% TOLERANCE

Consult our Technical Services department for specifications and recommendations for your applications.

SPECIFY FORM 3016 . . . WHEN REQUESTING FACTUAL CATALOG OF VICTOREEN COMPONENTS

The Victoreen Instrument Co.
3800 PERKINS AVE. • CLEVELAND 14, OHIO

Industrial Engineering Notes

(Continued from page 82A)

FCC Actions

The National Television System Committee has asked the FCC to adopt its proposed new and improved standards for color television. The petition was approved by members of the NTSC on July 21, and subsequently filed by Dr. W. R. G. Baker as Chairman of the NTSC. The action cleared the way for early Commission consideration of the whole color TV question including the petition filed on June 25 by RCA and NBC, and the expected repeal of the CBS color standards adopted almost three years ago. NTSC in its petition stated that other companies, in addition to RCA, also will petition the FCC for adoption of the proposed color standards. Complete copies of the petition and the proposed standards have been mailed by Chairman Baker to all companies in the industry which have displayed any interest in the NTSC activities. The Philco Corp. has filed a petition in support of the NTSC, requesting the FCC to authorize TV broadcasters at their option to transmit programs in color in accordance with the technical standards proposed by NTSC. The Columbia Broadcasting System in New York was quoted by the Associated Press as stating that it would not only support the move to substitute the NTSC compatible standards for the present incompatible standards but would by Sept. 15 have started providing some programs to its affiliated stations on an experimental basis, using the NTSC standards of transmission. Dr. Baker informed the FCC that "highly successful" tests have been made under the proposed standards which produce a compatible transmission that can be received in black and white on all TV receivers now in use. In its petition, the NTSC pointed out that transmission under its proposed standards will "produce a color picture which has a high quality of color fidelity, adequate definition and good picture texture." The NTSC petition said the standards proposed are an improvement over existing television standards in that they permit the broadcasting of color and simultaneously provide black and white sets with a high quality black and white picture. No changes would be necessary in present sets to permit them to continue to receive a black and white picture from transmissions in color. . . .

Three additional petitions have been filed by manufacturers with the FCC requesting the agency to adopt as its standards for color television the technical signal specifications proposed by the NTSC. Sylvania Electric Products Inc., the General Electric Co., and Motorola Inc. are the companies that have filed supporting petitions. As a result of its work, Sylvania said it estimated that "within six to nine months from the date of the Commission's approval of the proposed standards" it will be in a position "to produce substantial quantities of color television picture tubes." Continuing, Sylvania said it "has also built a number of color television receivers designed to receive the signal

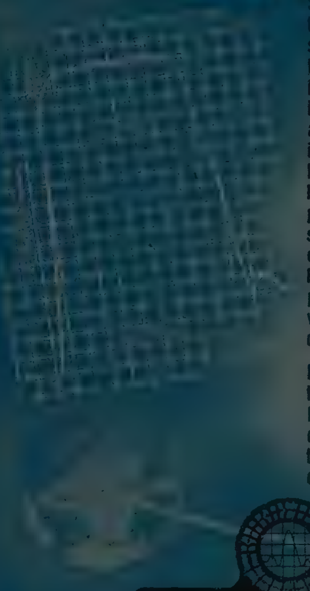
(Continued on page 86A)

A New Approach in Economical Side-Band Filters

TOMORROW'S FILTERS TODAY ..is

IN COMMUNICATION NETWORK COMPONENTS

Burnell SINGLE SIDE-BAND FILTERS



Single side band reception of space carrier telegraph and telephone transmissions, despite the improvement in reception attributable to its use, is still considered to be in its embryonic stage. Elimination of the duality of the modulation products, and the attainment of mono-band reception of the intelligence transmitted, has always been the apotheosis of communication engineers. Probably the greatest single factor that has precluded the rapid advancement of single side band systems, has been the excessive cost of the carrier and side band filters. Filters presently produced consist of a complex array of crystals and L. C. networks, which represents not only an expensive design but one not readily obtainable.

BURNELL & COMPANY'S new approach to this problem, not employing crystals, is based on the use of a system having a 25KC carrier and the exclusive embodiment of toroidal coils in a highly engineered circuit of temperature stabilized and temperature compensated components to produce the sharp-sided curve required in this system.

Burnell & Company
YONKERS 2, NEW YORK
CABLE ADDRESS "BURNELL"

.... A STEP FORWARD ....

IN COMMUNICATION NETWORK COMPONENTS

Burnell SINGLE SIDE-BAND FILTERS

The use of the 25KC carrier is a major advance in the design of side band filters. Primarily, it establishes a better ratio between the carrier frequency and the cut off frequency which, together with the aid of ingenious circuitry and miniaturized molybdenum permalloy toroidal cores, obviates the necessity for quartz crystals. The end result is a tremendous saving in size and weight, producing filters which are a fraction of the size of the former crystal filters. Typical dimensions are 1⅝″ x 6″ x 2⅝″ and weight 1½ lbs.

In offering these advantages BURNELL & COMPANY has taken not one but five steps forward by offering single side band filters which are:
1) LESS EXPENSIVE
2) MUCH SMALLER
3) MUCH LIGHTER
4) MORE RUGGED
5) MORE AVAILABLE

Burnell & Company
YONKERS 2, NEW YORK
CABLE ADDRESS "BURNELL"

and OPENS NEW DOORS ..... *in*

IN COMMUNICATION NETWORK COMPONENTS

Burnell SINGLE SIDE-BAND FILTERS

The potential demand for single side band equipment has up to now been restrained behind the "locked doors of frustration", so to speak, but we feel that we are helping to unlock those doors and release an even greater demand for side band equipment small enough and inexpensive enough to reawaken the interest of communication equipment manufacturers in this field for both civilian and military application. In the latter field single side band systems were virtually prohibitive because of the inadequateness of crystal filters for field use. The BURNELL system now eliminates all the objectionable features.

Burnell & Company
YONKERS 2, NEW YORK
CABLE ADDRESS "BURNELL"

HIGH SPEED COMMUNICATIONS

IN COMMUNICATION

Burnell SINGLE SIDE-BAND FILTERS

In addition to the carrier, lower side band and upper side band filters illustrated for 3.5KC pass bands, there is available a low pass filter for the demodulation circuit. There is also available for wider band operation side band filters having a 6KC pass band, with the same dimensions and weight.

By adding this group of filters to our regular series of multiplex filters we can, with pride, state that BURNELL & COMPANY has gone a long way toward assisting the communications industry to develop high speed communications resulting from more efficient operation and greater freedom from interference.

If you are an engineer in 'communications', you will be interested in our brochure describing the BURNELL single side band filters in greater detail.

Burnell & Company
YONKERS 2, NEW YORK
CABLE ADDRESS "BURNELL"

We've Stepped-up Production!

NOW Sangamo HUMIDITITE* Mica Capacitors are available in Quantity

When Sangamo HUMIDITITE Molded Mica Capacitors were first put on the market, the great interest shown in these remarkably moisture resistant capacitors far exceeded our expectations. We have increased our manufacturing facilities and our production capacity . . . initial demands have been met . . . and we can now handle quantity orders for Humiditite Micas with full assurance that delivery requirements will be met.

*what is HUMIDITITE?

Humiditite is the very effective new plastic molding compound, developed by Sangamo, that gives Sangamo Mica Capacitors moisture resistance properties far superior to any others on the market.

Sangamo Humiditite Micas, under the standard moisture resistance tests described in MIL-C-5A (proposed) Specification, tested in excess of 50,000 megohms—more than 500 times the specification requirements.

Humiditite is just another example of the advanced engineering that enables Sangamo to meet the existing and future needs of the electronic industry. For additional information about HUMIDITITE, write for Engineering Bulletin No. TS-111.

Those who know... SANGAMO choose Sangamo

The Little Indian

SANGAMO
ELECTRIC COMPANY
MARION, ILLINOIS

Industrial Engineering Notes

(Continued from page 84A)

specifications now proposed, both independently and in the field test program undertaken" by NTSC. "The Petitioner has tested its receivers. Petitioner estimates that it will start commercial production of color television receivers for sale to the public within nine months from the date of the Commission's adoption of the specifications proposed." Both the General Electric and Sylvania petition acknowledged that the initial price of color receivers will be high, but both expressed the opinion, based on past experiences, that through technological advances the price would be reduced. . . .

The FCC has issued a Notice of Proposed Rule Making looking toward the adoption of the NTSC's proposed color signal specifications as the standard for commercial color television broadcasting. The Commission invited comments from interested parties up to Sept. 8 after which another 15 days were allowed for receipt of replies. The notice gave no indication whether hearings would be held thereafter, and presumably the FCC would make no decision in this respect until after all comments had been filed. Noting that none of the petitioners proposed to put a color signal on the air in Washington at this time, although the NTSC did offer its cooperation in arranging demonstrations, the FCC stated that it would not be necessary that a Washington demonstration be held prior to the institution of rule-making proceedings. Other developments in color TV in Washington have been: The Commission waived its rules to permit the Columbia Broadcasting System to conduct experimental transmissions over its television network of "non-standard color television signals" conforming to the NTSC specifications. A letter was received from Hazeltine Corp. supporting the NTSC proposed signal specifications and the supporting petition from Motorola Inc. . . .

The FCC has announced substantial changes in its rules governing the priority in which it will consider applications for licenses to operate new television stations. A Commission spokesman said that many big cities no longer deserve the priority which they had received under the old rules. Now, uncontested applications for stations will continue to receive first priority under the new rules, which set up three major groups. Uncontested TV applications will be handled in the order of their filing. Contested applications will be divided into two classes, one including those communities with no TV station, and the other for communities already served by TV. The latter group will be further subdivided on the basis of the number of stations now serving an area in question. In either of the latter groups, the priority will be in the order of the size of the community, with largest areas coming first. Another major change, and one to which Commissioner Frieda B. Hennock filed a dissenting opinion, will eliminate priorities between applications for VHF and UHF transmitters. These applications will be handled alike, except on the basis of the above difference. . . .

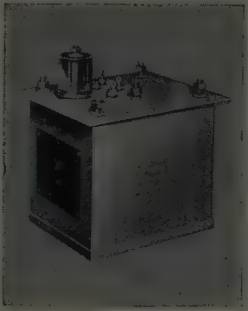
(Continued on page 90A)

DIGEST

TIMELY HIGHLIGHTS ON G-E COMPONENTS

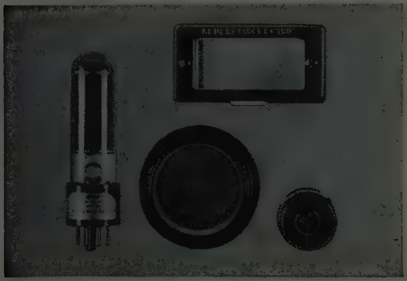
Compact high-voltage components built for extra long service life

These G-E high-voltage components offer a continuous-service life for long periods under extreme temperatures and mechanical shocks. All are oil-filled and hermetically sealed to resist moisture, dirt and dust. For applications 5000 volts and higher, where corona must be held to a minimum, a wide range of ratings can be tailored to meet your needs. In your inquiry, please include all functional requirements, any physical limitations, and expected quantities. Contact your G-E Apparatus Sales representative for more information.


Rectifiers

Reactors

Transformers

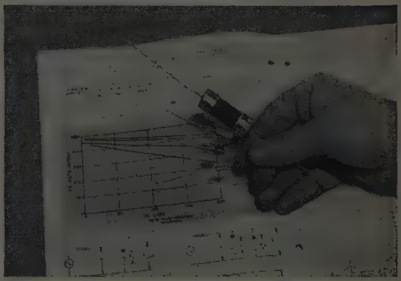


Detects, measures light accurately

G-E photovoltaic cells—for applications where electronic amplifiers are not practical—provide extra-high output with stability and long life in capturing light energy and converting it into electrical energy. This self-generating power plant can detect, measure, and control light—and can measure variations in colors. These G-E cells are available in a hermetically sealed series with standard mountings, and in a wide variety of mounted and unmounted sizes. See Bulletin GEC-690.

Speeds solution to field problems

The G-E analog field plotter offers a valuable aid to electronics equipment engineers in simplifying complex field studies. Problems in electrostatics, electromagnetics, and many other fields are rapidly solved with this sensitive, versatile plotting board and associated equipment. It needs only a low-voltage d-c supply, and is not affected by line-voltage variations. Explanation and instructions are covered in a 50-page manual accompanying plotter. For details, see Bulletin GEC-851.



Cover wide temperature range

From −55C through +100C—that's the wide range covered by these new G-E miniature selenium rectifiers. Stacks—available for either lead or bracket mounting—have the same outstanding features as larger G-E selenium cells: long life, good regulation, high reverse resistance, and low heat rise. For protection, they are enclosed in either Textolite* tubes, or hermetically sealed in metal-clad casings. For more data, contact your G-E Apparatus Sales representative.

EQUIPMENT FOR ELECTRONICS MANUFACTURERS

Components

- Meters, instruments
- Dynamotors
- Capacitors
- Transformers
- Pulse-forming networks
- Delay lines
- Reactors
- Thyrite*
- Motor-generator sets
- Inductrols
- Resistors
- Voltage stabilizers
- Fractional-hp motors
- Rectifiers
- Timers
- Indicating lights
- Control switches
- Generators
- Selsyns
- Relays
- Amplidynes
- Amplistats
- Terminal boards
- Push buttons
- Photovoltaic cells
- Glass bushings

Development and Production Equipment

- Soldering irons
- Resistance-welding control
- Current-limited high-potential tester
- Insulation testers
- Vacuum-tube voltmeter
- Photoelectric recorders
- Demagnetizers

*Reg. Trade-mark of General Electric Co.

General Electric Company,
Apparatus Sales Division, Section C667-26
Schenectady 5, New York

Please send me the following bulletins:
✓ for reference
✗ for immediate project

☐ **GEC-690** **Photovoltaic Cells**
☐ **GEC-851** **Analog Field Plotter**
☐ **GEC-987** **Permafil Capacitors**

1878 75 1953 YEARS OF ELECTRICAL PROGRESS

Name ________________________

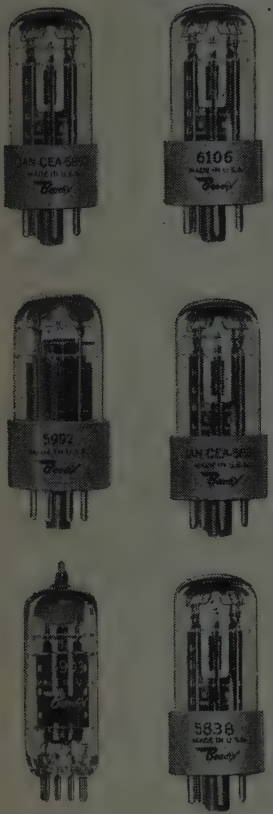
Company ________________________

City ________________ State ________

DEPEND ON

Bendix Red Bank

RELIABLE ELECTRON TUBES



With electronic controls taking over more and more operational functions in aircraft, it's becoming increasingly important that the electron tubes used be dependable under conditions of high altitude, continuous vibration, varying voltages and frequent shock. Because of their advanced design and construction . . . born of never-ceasing research and special production skills . . . Bendix Red Bank Reliable Electron Tubes have the dependability necessary to meet these severe operating conditions. You can depend on our long, specialized experience to give you the right answer . . . for all types of regular as well as special-purpose tube applications. Call on us for full details.

Manufacturers of Special-Purpose Electron Tubes, Inverters, Dynamotors and Fractional D. C. Motors

TYPE AND MODEL INDEX				TYPICAL OPERATING CONDITIONS		
Bendix No.	RTMA No.	JAN No.	General Type	Heater Voltage	Plate Voltage Per Plate	M.A. Load
TE-2		5839	OCTAL FULL WAVE RECTIFIER	26.5	350	70
TE-3	5838		OCTAL FULL WAVE RECTIFIER	12.6	350	70
TE-5		5852	OCTAL FULL WAVE RECTIFIER	6.3	350	70
TE-10	5993		MINIATURE FULL WAVE RECTIFIER	6.3	350	70
TE-22	6106		OCTAL FULL WAVE RECTIFIER	5.0	350	100

BEAM POWER AMPLIFIER TUBE	
SPECIFICATIONS	
BENDIX NO.	TE-8
RTMA NO.	5992
HEATER VOLTAGE	6.3 V
PLATE VOLTAGE	250 V
SCREEN VOLTAGE	250 V
GRID VOLTAGE	12.5 V
G. M.	4000
PLATE CURRENT	45 MA
POWER OUTPUT	3.5W

Bendix Red Bank DIVISION OF Bendix AVIATION CORPORATION

THE NAME MILLIONS TRUST

EATONTOWN, N. J.

Export Sales: Bendix International Division, 205 East 42nd St., New York 17, N. Y.

Industrial Engineering Notes

(Continued from page 86A)

MOBILIZATION

Through a joint announcement by Commerce Secretary Weeks and Defense Secretary Wilson, it has been made known that the major ordnance research and development projects, including guided missiles, proximity fuses, rockets, and electronic ordnance, which have been handled by the National Bureau of Standards will be transferred to the Defense Department. These projects to be transferred to Defense will be under the supervision of the Chief of Ordnance of the Department of the Army. They now represent around 50 per cent of the operating budget of the NBS. Four of the Bureau's 17 technical divisions are involved in the shift: Ordnance development, electro-mechanical ordnance, electronic ordnance and missiles development. After the transfer is completed, which has the approval of Dr. M. H. Kelly, President of Bell Laboratories and Chairman of a special committee appointed by Mr. Weeks to evaluate functions of the Bureau of Standards in relation to present national needs, serious consideration will be given to transferring supervision of this facility to the Navy Department, the announcement said. . . .

LEGISLATION

Rep. Carl Hinshaw (R., Calif.) has introduced H.R. 6431, designed to amend the Communications Act of 1934 so as to more closely restrict the definition of "Broadcasting" and classify subscription television and radio as a common carrier. The proposed change is not designed to include community antenna operations, Rep. Hinshaw said, but only subscription broadcasting. At present, the FCC is considering what classification should be applied to subscription broadcasting but as yet has announced no decision. . . .

AVIATION

John S. Anderson, President of Aeronautical Radio Inc., has been elected Vice Chairman of the Radio Technical Commission for Aeronautics. He succeeds John F. Horne, retired admiral and former Civil Aeronautics Administrator, who had been appointed Manager of the Pomona, Calif., Division of Consolidated Vultee Aircraft Corp. . . .

FEDERAL PERSONNEL

Capt. Rawson Bennett has been transferred from the Ships Division of the Bureau of Ships to Supervising Inspector of Machinery, Schenectady, New York. . . .

Colonel Francis F. Uhrhane has been appointed Commanding Officer of the Signal Corps Engineering Laboratories at Fort Monmouth, N. J. Col. Uhrhane formerly was assigned to the staff of the Chief Signal Officer in Washington, and succeeds Maj. Gen. Edwin R. Petzing who recently became Chief Signal Officer in the European Command. He is a native of Marietta, Ohio, and a graduate of the U. S. Military Academy, and holds a Mas-

(Continued on page 94A)

FERRANTI

TRANSFORMERS

HERMETICALLY SEALED

A NEW LINE OF STANDARD TYPES

- Designed to MIL-T-27 specifications
- MIL-T-27 standard steel cases
- Rugged sealed terminals
- Core and coil securely anchored to mounting studs
- High Vacuum impregnated

These types have been selected to provide standard, readily available components of the highest quality, including the specific types chosen by ASESA for universal military use.

Complete specifications on this wide range of units are contained in a new catalog. Your copy will be sent promptly on request.

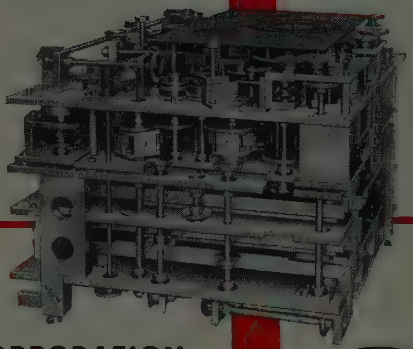
In addition to the group listed in this catalog, we manufacture reactors and transformers of all varieties, including the more economical types for use where conditions do not require the superior qualities of those listed in our catalog. We can offer competitive quotations on types to suit your exact needs.

FERRANTI
FERRANTI
FERRANTI

FERRANTI

FERRANTI ELECTRIC
INCORPORATED

30 Rockefeller Plaza
New York 20, N.Y.



computers . . .

for fire control,
bombing,
gun data,
navigation,
and shoran.

Since 1935
MAXSON
ENGINEERING
has developed
and produced
computers.

Our long experience
is at your
disposal.

THE W. L. MAXSON CORPORATION
460 WEST 34TH STREET, NEW YORK 1, NEW YORK
Plants at Long Island City, N. Y. and Old Forge, Pennsylvania

MAXSON

SECON

DEVELOPMENT and PRODUCTION
METALLURGISTS

Fine wire and ribbon in base, rare, and
precious metals, and alloys for
new and highly engineered applications.
In small units and sizes,
and to close tolerances.
Further details on request.

SECON

SECON METALS CORPORATION
7 Intervale Street, White Plains, New York
WHite Plains 9-4757

Industrial Engineering Notes

(Continued from page 90A)

ter's degree in electrical engineering from Ohio State University. . . .

Announcement has been made of the appointment of Paul D. Miles to be Engineering Assistant to FCC Chairman Rosel H. Hyde. He rejoined the Commission staff after a leave of absence of more than five years which enabled him to serve as a member of the International Frequency Registration Board (IFRB) of the International Telecommunication Union with headquarters at Geneva, Switzerland. Mr. Miles is a Senior Member of the IRE and an honorary member of the Order of the British Empire. . . .

SECTION MEETINGS

ALBUQUERQUE-LOS ALAMOS

"Description of Cornell University Solar Radio Observatory," by E. R. Schiffmacher, Cornell University and "Harvard University Solar Observatory," by J. W. Evans, Harvard University; August 1, 1953.

INYOKERN

"Design Problems of the Model 10-A-40 Doppler Radar," by Robert Young, Resdel Engineering Corporation; August 10, 1953.

ST. LOUIS

"Practical Applications of Transistors," by L. E. Flory, RCA Laboratories; May 14, 1953.

Election of Officers and Inspection of C.A.A. Facilities at St. Louis Municipal Airport; June 25, 1953.

SCHENECTADY

"Electronics Instrumentation," by Dr. Volkers, Millivac Corp.; May 11, 1953.

"Electronic Prestidigitation," by George Hobbs, General Electric Company; June 8, 1953.

SUBSECTIONS

WICHITA

Business meeting; June 11, 1953.

MEMBERSHIP

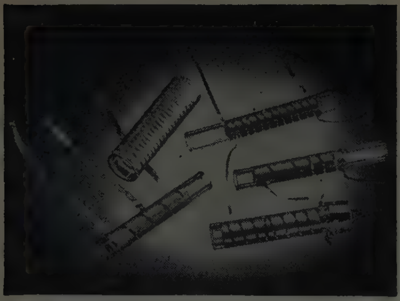
The following transfers and admissions were approved and will be effective as of October 1, 1953:

Transfer to Senior Member

Barnette, L. A. M., 4801 Linden St., Bellaire, Tex.
Blaisdell, K. L., 112 Shennecossett Pkwy., Groton, Conn.
Ebers, J. J., Elizabeth Pl., Whippany, N. J.
Eichert, E. S., 730 W. Springfield Rd., Springfield, Pa.
Halev, I., 1984 Sterling Rd., Philadelphia 38, Pa.
Hammond, E. B., Jr., 13 Oak Ct., Merrick, L. I., N. Y.
Haupt, G. H., 48 Van Voorhis Ave., Rochester 17, N. Y.

(Continued on page 96A)

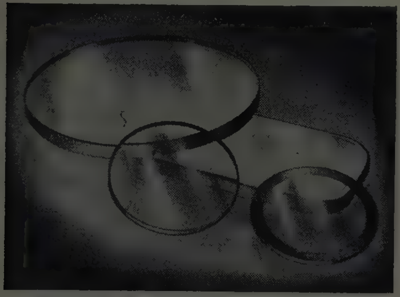
Are you overlooking the advantages of Corning metallized glass components?



Corning Metallized Glass Inductances are noted for their exceptionally high electrical stability and negligible drift characteristics, even under widely variable ambient temperatures. High Q is inherent. They can be furnished with uniform, variable, or double-pitch windings and for fixed tuned, permeability tuned, or permeability tuned inductance trimmer combinations. They can be duplicated within very close tolerances in any quantity.

Corning Film-Type Resistors afford a tough unit with unusual stability and capable of withstanding high ambient and high operating temperatures. Type N has a resistance tolerance of 1% and is capable of operating at ambient temperatures up to 140° C.; Type S has a normal resistance tolerance of 2% and is capable of operating at ambient temperatures up to 200° C.

Corning Metallized Glass Midget Trimmer Capacitors have practically zero temperature coefficients in the VHF range. Capacity shift is negligible even with widely variable ambient temperatures. They are available in standard types from .3 to 12 u.u.f., or can be designed to meet your specific requirements. With direct traverse trimming, there is negligible capacity shift under vibrations, and an absolutely smooth capacity curve.



Corning Metallized Glass Instrument Windows are made of tempered glass with a metallized band on the edge. They are easy to solder, provide a perfect hermetic seal. Temperature and humidity changes resulting from leaks in gaskets, cements and oils are virtually eliminated. These windows are available in a number of standard sizes, or can be furnished to your specifications.

Corning Metallized Glass Tubes for hermetic encasement of capacitors, resistors, Selenium rectifiers and other electronic components offer a number of advantages. The metallizing makes possible a true hermetic seal, the electrical characteristics of the glass are excellent, transparency permits visual inspection, units are impervious to moisture, corrosive atmospheres, molds, etc. Available in 15 sizes ranging from 1½″ to 7″ in length, O.D. 15″, I.D. .295″.

Corning Metallized Glass Bushings and Standoff Insulators are ideal for high voltage applications. The bushings provide hermetically sealed insulators for high-voltage capacitors and transformers, are available in 12 standard sizes ranging from 25/32″ to 7/32″ in length. Installation is fast and easy. The standoff insulators are made of tempered, low-loss glass, are completely nonhygroscopic. Both these components can be furnished in special sizes on order.

▶ *It will pay you to investigate the possibilities of Corning Metallized Glass Components. The coupon below will bring you the detailed information you need, or write and give us the details of the application you have in mind.*

Corning Glass Works

New Products Division

Corning means research in Glass

CORNING GLASS WORKS, Dept. RE-10, Corning, N. Y.

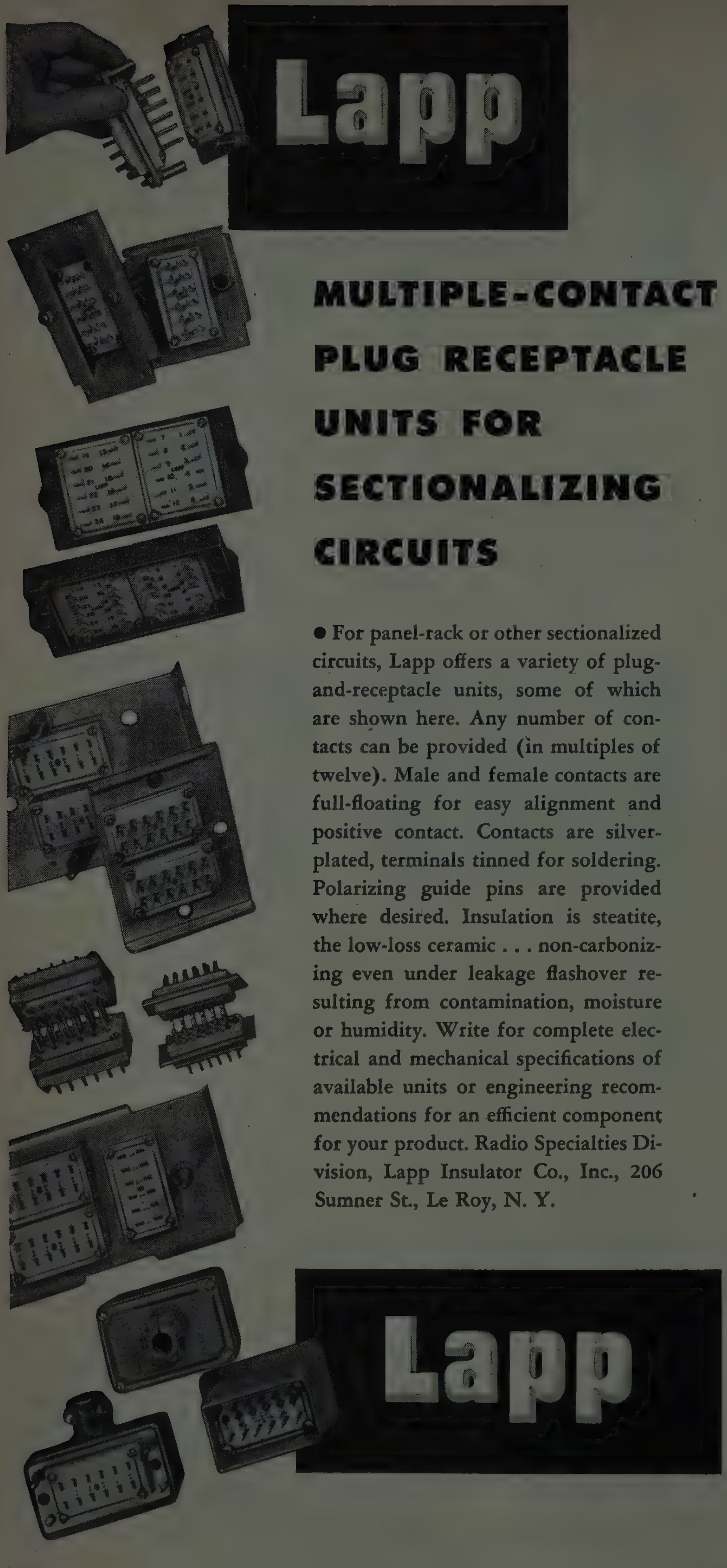
Please send me information on ☐ Inductances ☐ Resistors ☐ Capacitors ☐ Instrument Windows ☐ Tubes ☐ Bushings ☐ Standoff Insulators.

Name........................ Title........................

Company........................

Address........................

City........................ Zone.......... State..........



Lapp

MULTIPLE-CONTACT PLUG RECEPTACLE UNITS FOR SECTIONALIZING CIRCUITS

● For panel-rack or other sectionalized circuits, Lapp offers a variety of plug-and-receptacle units, some of which are shown here. Any number of contacts can be provided (in multiples of twelve). Male and female contacts are full-floating for easy alignment and positive contact. Contacts are silver-plated, terminals tinned for soldering. Polarizing guide pins are provided where desired. Insulation is steatite, the low-loss ceramic . . . non-carbonizing even under leakage flashover resulting from contamination, moisture or humidity. Write for complete electrical and mechanical specifications of available units or engineering recommendations for an efficient component for your product. Radio Specialties Division, Lapp Insulator Co., Inc., 206 Sumner St., Le Roy, N. Y.

Lapp

MEMBERSHIP

(Continued from page 94A)

Herrmann, F. J., 101-B Wallworth Park Apts., Haddonfield, N. J.
Hobbs, C. F., 16 Corinne Rd., Medford 55, Mass.
Ivans, W. S., Jr. 8669 Lemon Ave., La Mesa, Calif.
Kadish, J. E., 2 Evergreen Ave., Auburndale, Mass.
Knowles, D. J., 116 Quincy Ave., Oak Ridge, Tenn.
Langhi, A. M. A., San Juan 451-B, Martinez, FCBM, Argentina
Lucas, F. B., 5340 David Rd., S. Miami 43, Fla.
McClain, E. F., Jr., Naval Research Laboratory, Washington, D. C.
Osbahr, B. F., 492 Third St., Brooklyn 15, N. Y.
Seddon, J. C., Box 230-E, R.D. 1, Alexandria, Va.
Shirk, W. B., 6342 Hamilton Ave., Cincinnati 24, Ohio
Shoup, J. P., 7318 Bradshaw, S. E., Albuquerque, N. M.
Staras, H., 3426 Tulane Dr., West Hyattsville, Md.
Swantz, F. W., 16 S. 23 St., Belleville, Ill.
Szilasi, A., 10 Gansevoort St., Bath, N. Y.
Walchli, H. E., 144 Waddell Cir., Oak Ridge, Tenn.
Walther, A., Institut für Praktische Mathematik, Technische Hochschule, Darmstadt, Germany
White, S. D., Bell Telephone Laboratories, Inc., 463 West St., New York 14, N. Y.
Winn, D. L., 114 E. Capitol, Little Rock, Ark.

Admission to Senior Member

Ahlstedt, T. E., 3 Godfrey Ave., Roseland, N. J.
Graham, R. S., Bell Telephone Laboratories, Inc., Murray Hill, N. J.
Kelly, C. M., 754 Scotland Rd., Orange, N. J.
McConnell, K. R., 40 Lake Ave., Red Bank, N. J.
Meijer, R. R., Bendix Aviation Corp., Eatontown, N. J.
Park, C. W., 6035 Chabolyn Terr., Oakland 18, Calif.
Rigg, G. L., 15448 Stare St., Sepulveda, Calif.
Smith, P. C., Box 48, Paoli, Pa.
Stanwick, T., 4849 Brandywine St., N.W., Washington 16, D. C.
Tomota, M., Yokogawa Electric Works Ltd., 3000 Kichijoji, Musashino-shi, Tokyo, Japan
Wolfe, F. R., Jr., 1220 N. State Pkwy., Chicago 10, Ill.

Transfer to Member

Albro, P. W., 823 F St., Newport News, Va.
Carrick, D. S., 2710 San Diego Ave., S.E., Albuquerque, N. M.
Chapman, L. B., 2459 Parkview Ave., Toledo 6, Ohio
Goss, W., 5009 Cherokee Rd., N.E., Albuquerque, N. M.
Hedlund, D. A., 121 Cobleigh St., Islington, Mass.
Hitt, W. R., 2206 E. Liberty, Phoenix, Ariz.
Karp, P. W., 3826—25 St., San Francisco 14, Calif.
Leeman, A., Box 499, La Crosse, Wis.
Longo, C. V., College of Engineering, Rutgers University, New Brunswick, N. J.
Martin, D. O., 172—Seventh, N. St., Syracuse 8, N. Y.
McKey, D. B., RCA Victor Division, Bldg. 15-2, Camden 2, N. J.
Morris, W. P., Bendix Radio, Dept. 70, Baltimore 4, Md.
Raha, H., 1B Priyanath Banerji St., Calcutta, West Bengal, India
Saito, S., 3318 Jones Bridge Ct., Chevy Chase 15, Md.
Sarwate, V. V., 881 Wright Town, Jabalpur, M. P., India
Thomas, C. Y., R.D. 1, Owings Mills, Md.
Tolsch, I. H., 48 Aster Ave., N. Merrick, N. Y.

Admission to Member

Ajeman, M. S., 3367 E. Pima, Tucson, Ariz.
Allen, W., Jr., Box 505, Douglas, Ariz.

(Continued on page 102A)

Advertisement

AMPHENOL
A N CONNECTORS

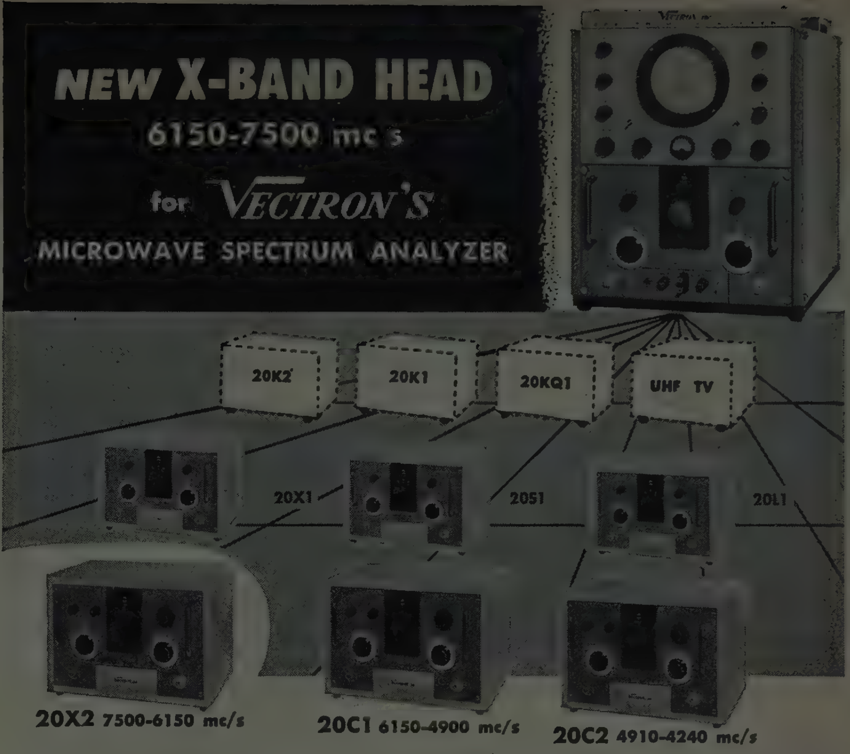
First with melamine inserts, first with the new improved dielectric material 1-501 diallyl phthalate, first with machined coupling rings, Amphenol now has made yet another improvement in A N connectors with the introduction of gold-plated contacts as standard. And, since Amphenol first began to manufacture A N connectors, the record has been one of constant improvements, leading to one result: superior efficiency in every application with the use of Amphenol A N connectors. Because of this record, Amphenol today is the leading manufacturer of approved A N connectors.

Every Amphenol A N connector is made to government specifications, but if alternate processes in manufacture are allowed, Amphenol has always adopted the highest quality interpretation. Thus, many features of Amphenol A N connectors exceed the requirements of the specifications and are unique with Amphenol. Gold-plating contacts is the newest Amphenol improvement in A N's and is representative of the plus values built into Amphenol connectors to save the user time and money and to assure the best possible performance.

For, not only in design are Amphenol A N connectors superior—but in performance, too. Highly trained personnel, modern manufacturing facilities and rigid quality control procedures combine to insure that every Amphenol A N connector will perform with precision—for years.

Amphenol A N connectors, while designed for the armed services, are ideal for commercial and industrial uses where the same dependability is mandatory. A N connectors are being widely employed in electrical and electronic industrial equipment, laboratory apparatus and therapeutic devices. Many industries—railroads, aircraft, textiles, radio and television—use types of circuits in which Amphenol A N connectors perform to great advantage.

NEW X-BAND HEAD
6150-7500 mc/s
for VECTRON'S
MICROWAVE SPECTRUM ANALYZER



THE NEW 20X2 R. F. HEAD provides band coverage from 6150 to 7500 mc/s. With the recently announced 20C2 (4240-4910 mc/s) and 20C1 (4900-6150 mc/s) Vectron's Microwave Spectrum Analyzer now provides a choice of operating frequencies from 4240 to 7500 mc/s. Additional X-band operating frequencies, 8500 to 10,250 mc/s, are covered by the 20X1 R. F. head and its variants. Other R. F. assemblies are available for L-band (20C1) and S-band (20S1).

VECTRON'S R. F. HEADS are all interchangeable and ready for immediate operation in the Display Unit SA20, without conversion or adaptation. Display Units and R. F. Heads can be purchased separately as needed without the bulk and expense of equipment covering large areas in unused bands.

Early Delivery . . . Individual R.F. Heads and SA20 Analyzers are available for early delivery. Other new Heads are well along in development and will be announced soon. Send for Bulletin SA20 (see below) and specify the frequencies you need.

For Microwave Radar and Communications Equipment The Vectron SA20 Spectrum Analyzer presents visually the frequency distribution spectrum of the power output of pulsed or CW microwave oscillators and can be used as a sensitive R. F. detector for checks and measurements in the design, production and maintenance of microwave radar and communications equipment and components.

FEATURES

Large, clear 5″ oscilloscope pattern

Standard bezel to accept camera, hood or filter

Minimum number of controls . . . maximum operating convenience

Double conversion assures I. F. alignment stability

Built in regulated supply for Klystron oscillator

Easy access for maintenance or adjustment

New Provision for D.C. Filament supply for Klystron oscillator

SPECIFICATIONS

Overall Gain — 130 decibels

Sensitivity — At least 60 dbm for 1 usec. pulse — 80 dbm for CW

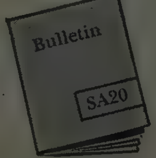
IF Bandwidth — Choice of 50 kc, recommended for CW and 0.2 to 2 usec. pulse widths, or 20 kc bandwith to 5 usec.

Sweep Frequency — 10 to 30 cps standard — available to 2 cps and with long persistence tube

Power supply 105-125V, 50-400 cycles

New Low-noise 20kc IF strip for higher useable gain.

Vectron's development program includes additional R. F. Heads to cover microwave frequencies newly opened for military and civilian use. For information on these additional R. F. Heads and for complete engineering data, send for Bulletin SA20. Write today and be sure to specify the operating frequencies you need.



VECTRON, inc. Electronic and Electro-Mechanical Equipment
402 MAIN STREET, WALTHAM 54, MASS.

Vectron invites your inquiries regarding the development and manufacture of:

Gyro-mechanisms
Gyro-stabilized Platforms
Gyros and Gyro Systems
Aircraft Instruments
Precision Mechanical Devices
Computers and Calculators
Gear Assemblies
Test Instruments
Synchros and Servomechanisms
Electronic Systems
Precision Electronic Components
Communication Networks and Filters
Microwave Equipment
Microwave Test Equipment
Radar Units and Systems
Echo Boxes

FAIRCHILD

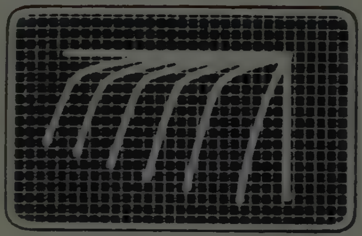
Complete—all calibrating circuits built-in. Needs only standard DC oscilloscope.

Transistor Analyzer

Developed by Fairchild in its program for transistorizing Missile Guidance Systems and other intricate electronic circuits.

Rapidly Plots Static and Dynamic Characteristics of ALL Transistors... point contact and junction. Designed on basic principles, to meet future transistor needs.

Complete Families of Curves obtainable in 10 incremental steps for each of 5 ranges. Sweeping technique shows up anomalies.



Presents on the Scope:

Alpha vs. Emitter Current

•

Collector, Emitter and Transfer Characteristics

•

Collector Characteristics in Grounded Emitter Connection

[illegible]

ENGINE AND AIRPLANE CORPORATION

FAIRCHILD

Guided Missiles Division

Wyandanch, L. I., N. Y.

Other Divisions: Aircraft Division, Hagerstown, Md. • Engine Division, Farmingdale, N. Y.

MEMBERSHIP

(Continued from page 96A)

Bailey, J. C., Hughes Research & Development Laboratories, Culver City, Calif.
Briggs, A. S., 937 Brunswick Rd., Cleveland Heights, Ohio
Chow, W. F., 477 James St., Syracuse 3, N. Y.
Chute, R. D., 800 Noe Bixby Rd., Reynoldsburg, Ohio
Corkran, D. H., 154 Lake Ave., Fair Haven, N. J.
Dover, J. J., General Delivery, Edwards AFB, Edwards, Calif.
Dunwell, S. W., 52 Mohegan Rd., Larchmont, N. Y.
Eulo, G. R., 100 Third Ave., Haddon Heights, N. J.
Faullin, R. R., c/o Dr. C. W. Vance, Livermore Rd., Owensboro, Ky.
Gapasin, F. G., CMR, Box 27, APO 994, c/o PM, San Francisco, Calif.
Goldsborough, R. R., Jr., 601 N. Bay View, Sunnyvale, Calif.
Gordon, L. L., 190 Long Branch Ave., Long Branch, N. J.
Hagen, G. D., Federal Electric Corp., 100 Kingsland Rd., Clifton, N. J.
Hardy, L. H., 124 Oxford, Eggertsville 23, N. Y.
Hill, F. E., 522 S. Law St., Aberdeen, Md.
Hoagbin, J. E., 1200 W. Cross St., Ypsilanti, Mich.
Janes, H. B., 1013 S. Tejon St., Colorado Springs, Colo.
Kirby, S. H., 4411 N. Seventh St., Phoenix, Arizona
Koval, E. R., 23 Empire St., Franklinville, N. Y.
McFadden, E. R., 87 W. Park Rd., Grand Island, N. Y.
McLaughlin, J. A., 909 E. 46 St., Long Beach 7, Calif.
Meggers, W. F., Jr., 6844 DeAnza Ave., Riverside, Calif.
Miles, A. R., 2924 Santa Clara, S. E., Albuquerque, N. M.
Nowick, C. A., 39 Fifth Ave., Pelham, N. Y.
Peters, M. W., 6040—14 St., N.W., Washington 11, D. C.
Rehm, M. P., RCA Communications, Inc., 66 Broad St., New York, N. Y.
Saltzman, H., General Precision Laboratory, Inc., Pleasantville, N. Y.
Shakir, M. M., 25 Moustafa Fahmy, Helwan, Cairo, Egypt
Sielicki, A. J., 2140 S. 81 St., West Allis 14, Wis.
Smith, R. B., 6525 N. Maplewood Ave., Chicago 10, Ill.
Smith, T. C., American Consulate, APO 206, c/o PM, New York, N. Y.
Solow, M., 418 Deerfield St., Silver Spring, Md.
Stoehr, W. F., 1514 Mardina, West Covina, Calif.
Stokely, R. G., 1033 Cathedral Way, Pomona, Calif.
Sutherland, A. D., RCA Laboratories, Princeton, N. J.
Tomey, J. G., c/o Plastoid Corp., Hamburg, N. J.
Weixler, H. J., 7984 Quinn Cir., Millington, Tenn.
Wilds, R. B., 2515 General Arnold St., N.E., Albuquerque, N. M.

The following elections to the Associate grade were approved to be effective as of September 1, 1953:

Agalsoff, J., 857 S. Fourth St., Montebello, Calif.
Ainsworth, E. F., 4524 Walsh St., Chevy Chase, Md.
Allaback, W., 118 Parkview Dr., North Canton, Ohio
Ashton, M. W. T., 2015 W. First St., Grand Island, Nebr.
Baer, E. W., III, 23 Caperton St., Newport, R. I.
Bauer, W. F., 2818 Pittsfield Blvd., Ann Arbor, Mich.
Becker, F. K., 10701 Inwood Ave., Silver Spring, Md.
Beers, W. T., 7 Sheridan St., West Newton, Mass.
Bendel, S., Jr., 1847 Linda La., Falls Church, Va.
Biss, R. E. P., 241-21—86 Ave., Bellerose 26, L. I., N. Y.

(Continued on page 106A)

Maximum Electronic Performance in any WEATHER with

LORD TEMPROOF MOUNTINGS ON COLLINS 618S-1 TRANSCEIVER~

SENSITIVE electronic equipment for airline transmitting and receiving must give continuously accurate results. For instance, note this "inside" view of the Collins Transceiver, mounted on Lord Temproof Mountings which isolate it from vibration and shock. Lord Temproof Mountings function efficiently throughout operational ranges of temperature from —80° to +250°F. The Collins Transceiver with automatically tuned elements for maximum flexibility and high power output delivers maximum performance in any weather, completely protected from vibration, shock and excessive equipment motion at resonant frequencies by Lord Temproof Mountings.

May we give you further details on this Lord application or help you solve your specific mounting requirement?

BURBANK, CALIFORNIA
233 South Third Street

DALLAS, TEXAS
413 Fidelity Union
Life Building

PHILADELPHIA 7, PENNSYLVANIA
725 Widener Building

DAYTON 2, OHIO
410 West First Street

DETROIT 2, MICHIGAN
311 Curtis Building

NEW YORK 16, NEW YORK
280 Madison Avenue

CHICAGO 11, ILLINOIS
520 N. Michigan Ave.

CLEVELAND 15, OHIO
Room 811 Hanna Building

LORD MANUFACTURING COMPANY • ERIE, PA.

LORD BONDED RUBBER

Headquarters for **VIBRATION CONTROL**

WHEN YOU NEED A

"GO-NO-GO"

GAUGE FOR ELECTRONIC COMPONENTS

The SIE

MODEL E-1 COMPARISON BRIDGE IS YOUR ANSWER!

CLOSE TOLERANCE

DIA. .1250" ± .0001"

1250 Ω ± 1 Ω

ASSURES SUPERIOR QUALITY IN ELECTRONIC EQUIPMENT AS IN PRECISION MACHINERY

And now SIE enables you to hold tolerances as close as .1% on resistors, capacitors, and inductances, at a price you can afford.

$150.00 F. O. B. HOUSTON

Send for our free brochure—

SOUTHWESTERN INDUSTRIAL ELECTRONICS COMPANY
2831 POST OAK ROAD
HOUSTON 19, TEXAS

PERFORMANCE PROVED...

JOHNSON SPECIAL SOCKETS

122-101-14

122-217-8

122-211-14

Engineered for longer life
Designed for top performance

JOHNSON electrical components include a complete line of special sockets for virtually every electronic application. Engineering skill, the result of years of specialized experience, and the most modern manufacturing facilities assure you of stock or custom-fabricated sockets that are both durable and dependable.

The special sockets shown here, variations of JOHNSON standard types, were designed to meet the punishing requirements of the 100 hour salt spray test. Construction successfully resists salt water corrosion, moisture condensation, and fungus growth; all contacts and contact springs are heavily silver plated to insure low loss and a positive electrical connection. Terminals are hot tin dipped, bases are of grade L-4 Steatite insulation with glazed top and sides. To provide added protection, all other surfaces are DC-200 impregnated.

122-101-14—Designed for Septar base tubes such as the 826, 829, 832, etc., this special socket has an anodized aluminum shell and provision for mounting mica button capacitors directly to the socket base. Five nickel plated, phosphor bronze retaining springs hold tubes securely in place and permit trouble-free operation in any position. A recessed base, solidly mounted on fungus resistant, phenolic washers, positively eliminates any contact movement.

122-217-8 thru 122-228-8—A series of ceramic wafer sockets designed to accommodate standard receiving tubes. Locating grooves speed tube insertion . . . beryllium copper retaining springs hold tubes firmly in place. Recessed phosphor bronze contacts prevent movement; countersunk rivets and boss located mounting holes permit sub-panel mounting.

122-211-14—A bayonet type socket for all tubes equipped with "50 watt" bases. Double beryllium copper filament contacts (.0005" silver plated), and hot tin dipped integral solder terminals insure positive contact with a minimum loss. Brass shell is .0003" nickel plated—ceramic base extends beyond contacts, increasing breakdown voltage rating.

JOHNSON special sockets, made to order in production quantities, meet all JAN material specification requirements. The complete JOHNSON standard socket line is listed in catalog 973, available on request.

Inquires are invited, and wherever possible we will gladly quote on "specials" to meet military requirements.

E. F. JOHNSON COMPANY

CAPACITORS, INDUCTORS, SOCKETS, INSULATORS, PLUGS, JACKS, DIALS, AND PILOT LIGHTS

204 SECOND AVENUE SOUTHWEST • WASECA, MINNESOTA

MEMBERSHIP

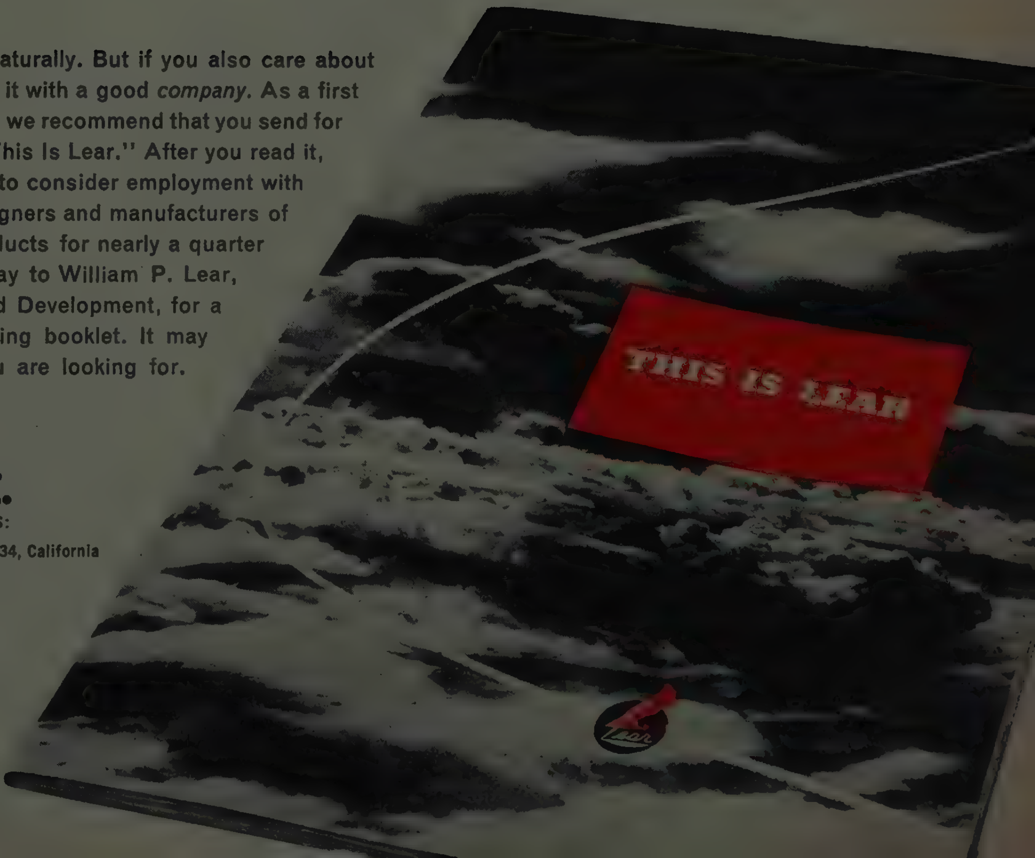
(Continued from page 102A)

Blair, C. R., 2032 Pierce Mill Rd., N.W., Washington 10, D. C.
Brown, D. E., Vitro Corporation of America, 962 Wayne Ave., Silver Spring, Md.
Brown, R. A., 4715 W. Lovers La., Dallas 9, Tex.
Bryant, C. R., 4113 Union Bay La., Seattle 5, Wash.
Budlong, W. A., Bell Telephone Laboratories, Inc., Murray Hill, N. J.
Burrell, J. E., 11602 Hartsook St., N. Hollywood, Calif.
Burridge, M. V., Special Service Division, Canadian Marconi Co., 2442 Trenton Ave., Montreal, Que., Canada
Carroll, W. P., 312 Rosewood Ave., Winnetka, Ill.
Carter, J. M., 5121 Worthington Dr., Washington 16, D. C.
Clark, W. A., Jr., 177 Spring Ave., Arlington, Mass.
Clarke, B. E., R.F.D. 11, Lincolndale Ct., Fort Wayne, Ind.
Clutterham, D. R., Aerophysics Department, Consolidated Vultee Aircraft Corp., Fort Worth, Tex.
Cobb, A. D., Box 711, Key West, Fla.
Couture, G., 358 Berkley St., St. Lambert, Que., Canada
Cowels, E. D., Detroit Edison Co., 2000 Second Ave., Detroit, Mich.
Cramer, G. F., 612 Vale St., Chevy Chase 15, Md.
Dawson, H. E., Page Engineers, APO 677, c/o Postmaster, New York, N. Y.
De Freitas, J. F., 35 Robb St., Box 463, Georgetown, British Guiana
Delaney, R. P., Raytheon Manufacturing Co., 160 N. Washington St., Boston 14, Mass.
Dickens, R. D., 1916 Westinghouse St., San Diego 11, Calif.
Dobyne, J. C., Jr., 12 N. Maple, Ferguson 21, Mo.
Eagle, G. R., 102 E. Mason Ave., Alexandria, Va.
Edelson, L. F., 1072 S. Norton, Los Angeles, Calif.
Edison, E., 329 Sycamore Rd., Santa Monica, Calif.
Eldridge, A. J., 145 Cornell Dr., Rialto, Calif.
Ermatinger, C. E., 3456 Altura Ave., La Crescenta, Calif.
Everhard, F. U., Jr., 77 Ninth St., W., Huntsville, Ala.
Ferrara, A. A., 1902 Powhatan Rd., W. Hyattsville, Md.
Freese, P. G., 1875 Grier St., Pomona, Calif.
Froggatt, J. W., Jr., Box 3342, MCLI USAFIT, Wright-Patterson AFB, Ohio
Ferguson, K. W., Box 422, Freeport, Tex.
Gale, R. J., 97 Mill River St., New Haven, Conn.
Gaskins, F. J., 172 Taylor Ave., East Meadow, L. I., N. Y.
Gastineau, L., 5745 N. Earle, San Gabriel, Calif.
Goldberg, B. A., 325 S. Clinton Ave., Oak Park, Ill.
Goodrich, P. E., 1971 Las Lunas St., Pasadena 8, Calif.
Gray, R. W., 1149 Goyeau St., Windsor, Ont., Canada
Hall, O. E., Massachusetts Institute of Technology, Instrumentation Laboratory, 68 Albany St., Cambridge 39, Mass.
Haner, L., 31-A Stephen Oval, Glen Cove, L. I., N. Y.
Heath, H. W., 2015 N.W. Flanders St., Portland, Ore.
Hepfer, J. W., Box 3197, Wright-Patterson AFB, Ohio
Hock, R. E., 4730 Wayburn, Detroit, Mich.
Hunt, C. R., 2145 Westburn Rd., E. Cleveland, Ohio
Hutt, C. E., 3310 Douglass St., El Paso, Tex.
Jackson, W. E., Electrical Engineering Department, Tufts College, Medford 55, Mass.
Jacobsohn, D. H., 5401 Ellis Ave., Chicago, Ill.
Jagadavan, S., 10 A. Vilvarayanatham, Cuddalore, N.T., Madras Presidency, South India
James, V. G., 2915 Kecoughtan Rd., Hampton, Va.
Johnson, D. S., Jr., 1320 Pearl St., Boulder, Colo.

(Continued on page 108A)

Engineers—look before you leap!

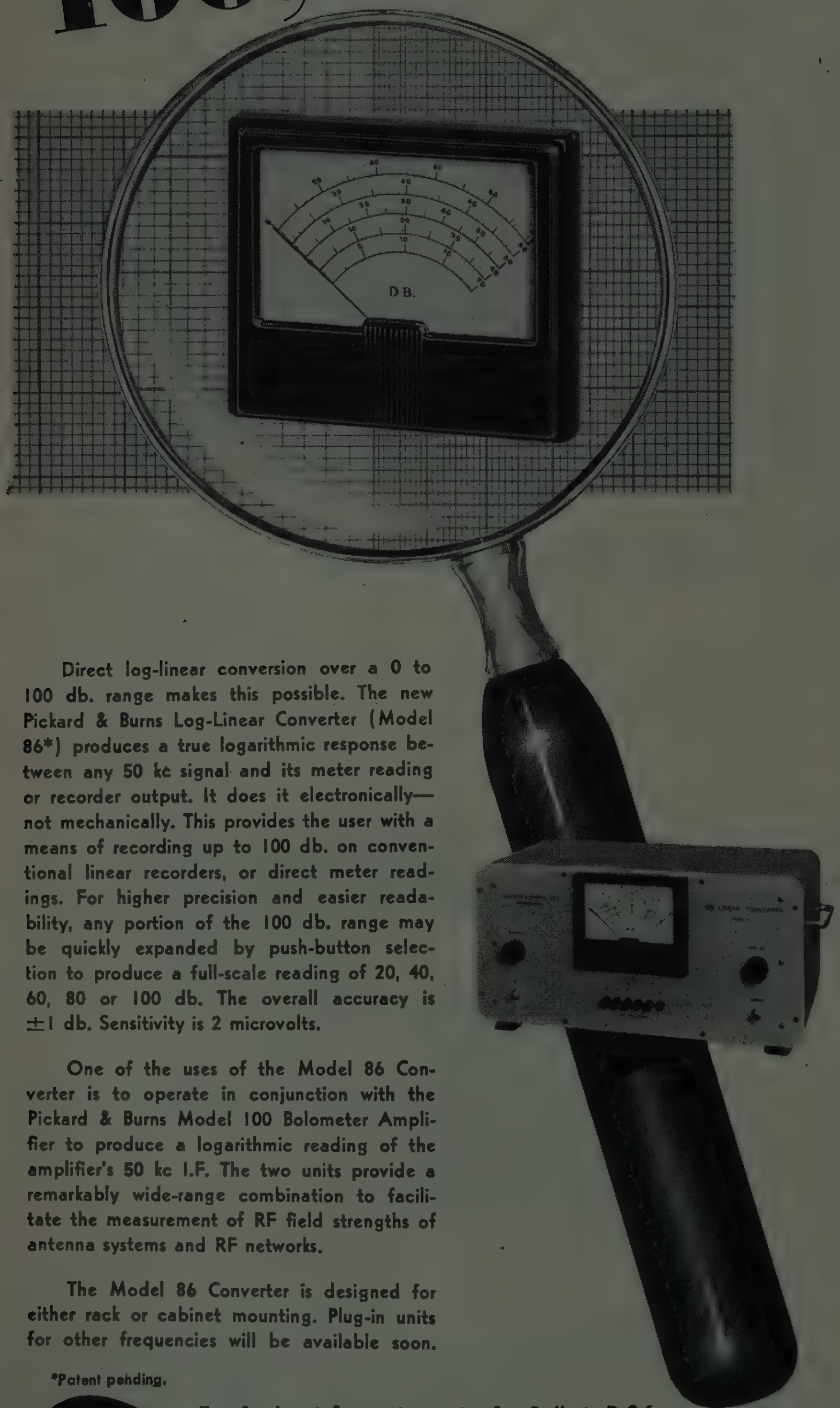
You want a good job, naturally. But if you also care about your future, you will seek it with a good *company.* As a first step in the right direction, we recommend that you send for a copy of the booklet, "This Is Lear." After you read it, we believe you will want to consider employment with Lear, Incorporated—designers and manufacturers of quality aeronautical products for nearly a quarter of a century. Write today to William P. Lear, Director of Research and Development, for a free copy of this interesting booklet. It may be just the "break" you are looking for.



LEAR, INC.
EXECUTIVE OFFICES:
3171 South Bundy Dr., Los Angeles 34, California

NOW READ VOLTAGE RATIOS OF

100,000 to 1



Direct log-linear conversion over a 0 to 100 db. range makes this possible. The new Pickard & Burns Log-Linear Converter (Model 86*) produces a true logarithmic response between any 50 kc signal and its meter reading or recorder output. It does it electronically—not mechanically. This provides the user with a means of recording up to 100 db. on conventional linear recorders, or direct meter readings. For higher precision and easier readability, any portion of the 100 db. range may be quickly expanded by push-button selection to produce a full-scale reading of 20, 40, 60, 80 or 100 db. The overall accuracy is ±1 db. Sensitivity is 2 microvolts.

One of the uses of the Model 86 Converter is to operate in conjunction with the Pickard & Burns Model 100 Bolometer Amplifier to produce a logarithmic reading of the amplifier's 50 kc I.F. The two units provide a remarkably wide-range combination to facilitate the measurement of RF field strengths of antenna systems and RF networks.

The Model 86 Converter is designed for either rack or cabinet mounting. Plug-in units for other frequencies will be available soon.

*Patent pending.

For further information write for Bulletin P-86

PB

PICKARD & BURNS
INCORPORATED
240 Highland Avenue, Needham 94, Mass.

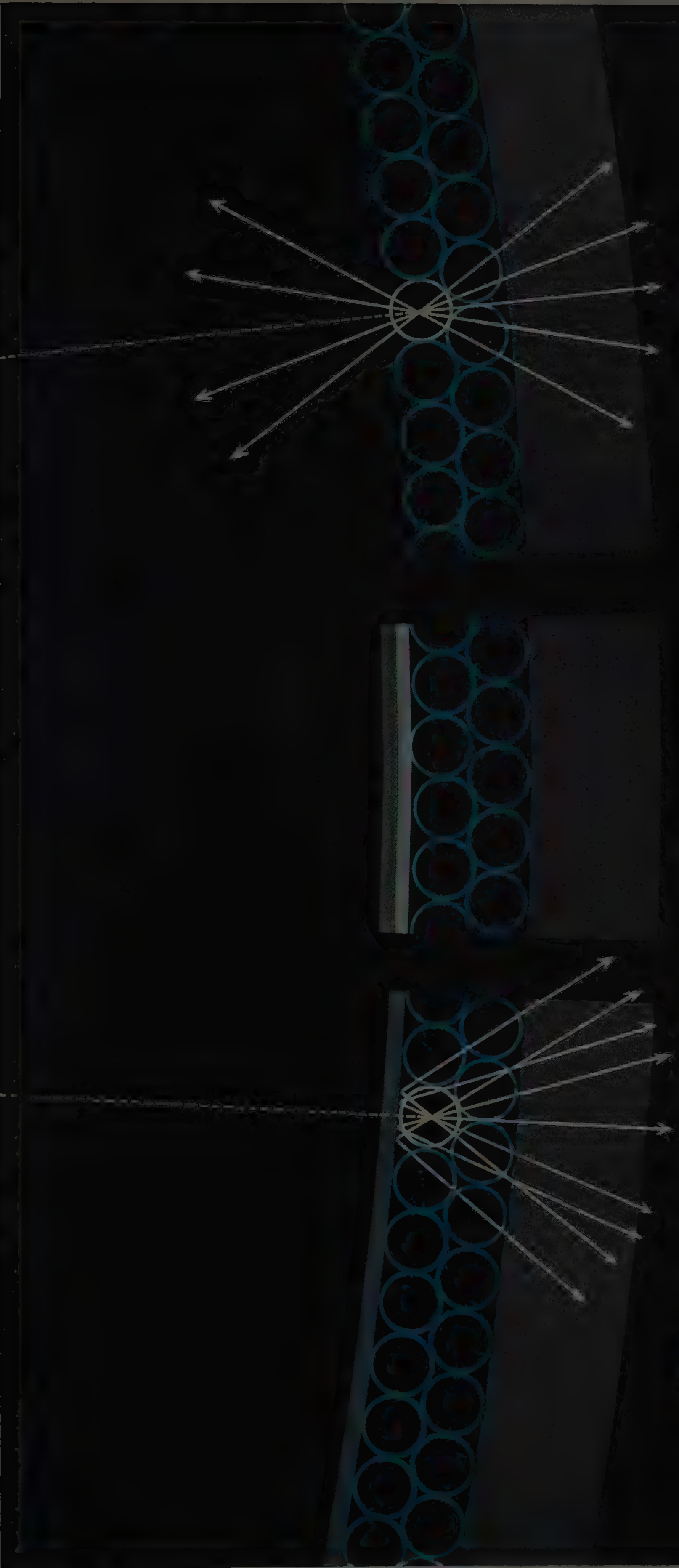
MEMBERSHIP

(Continued from page 106A)

Johnson, G. G., 308-A Entwhistle, China Lake, Calif.

Kampen, A. C., 8622 Plum St., New Orleans 18, La.
Kinnaman, R. L., 4013 E. Douglas, Wichita, Kans.
Larrimer, J. K., 2527 Wellesley Ave., Los Angeles 64, Calif.
Lacy, W. K., 135 Alice Ave., Syracuse, N. Y.
Larrowe, B. T., 1219 Share Ave., Ypsilanti, Mich.
Lee, A. E., R.F.D. 1, Clay, N. Y.
Lewis, W. H., Box 362, Lincoln Park, N. J.
Liewald, V. R., 2114 Wawona St., San Francisco, Calif.
Lindgren, H. A., Minneapolis Honeywell, 2600 Ridgeway Rd., Minneapolis, Minn.
Loughran, R. H., 912 Third Ave., Des Plaines, Ill.
Luke, J. W., International Business Machines Corp., 1022 The Alameda, San Jose 12, Calif.
MacDonald, I. T., 14892 Sutton Dr., Los Gatos, Calif.
Manner, C. E., 108 Riverthorn Rd., Baltimore 20, Md.
Marcucci, R. L., 1558 N. Marion, Tulsa, Okla.
Marti, N. F., Telecomputing Corp., Suite 206–208, 1000 Vermont Ave., N.W., Washington 5, D. C.
McCraw, L. E., 989 Echles, Memphis, Tenn.
McKenzie, A. D., Box 6004, Raleigh, N. C.
McMillan, J. D., Box 1328, Western Electric Co., Anchorage, Alaska
Melvin, R. M., 50 Halkin La., Berkeley 7, Calif.
Merish, H. J., 31 Passaic Ave., Pompton Lakes, N. J.
Meyer, D. E., Jr., 1132 Victor St., Denver 8, Colo.
Milenbach, H., 300 E. Third St., New York 9, N. Y.
Moore, J. G., Apt. 1, 2711 S. Sepulveda Blvd., Los Angeles, Calif.
Muench, W. H., c/o Falstrom Co., Falstrom Ct., Passaic, N. J.
Muoio, A. W., 139 Lawnside Ave., Collingswood, N. J.
Murdock, B. B., Prudential Insurance Co., Broad St., Newark, N. J.
Neuse, D. H., 1605 Lake Shore, Port Arthur, Tex.
Often, C. G., WDSU-TV, 520 Royal, New Orleans, La.
O'Leary, J. P., Opers. Sq. Otis AFB, Falmouth, Mass.
Olson, H. G., 45 Vivian Ct., New Orleans 14, La.
O'Neal, C. L., 7816 Santa Clare Rd., El Paso, Tex.
O'Neal, O. R., Western Electric Co., Department 851, Chatham Rd., Winston-Salem, N. C.
Pappas, J., 4311 Eastlawn Ave., Wayne, Mich.
Pechon, A. J., 820 Cadiz St., New Orleans 15, La.
Pesca, F. J., 1170—76 St., c/o Gualtieri, Brooklyn 28, N. Y.
Pivnik, S. I., 2129 E. 14 St., Brooklyn 29, N. Y.
Pourtales, J. R., 1132 N. Heliotrope Dr., Hollywood 29, Calif.
Putnam, P., 10 Amory St., Nashua, N. H.
Real, P., 1215 Woodington Rd., Baltimore 29, Md.
Reinert, D. O., 15 Mac Arthur Rd., Natick, Mass.
Revere, R. W., 64 Kane Pl., N. Babylon, L. I., N. Y.
Robbins, L. E., 10 Parmalee Ct., Huntington, L. I., N. Y.
Robert, J. M., c/o W. McLoughlin, 1114 Ardmore, Apt. 2-C, Chicago 40, Ill.
Rogers, G. J., 1811 Tucker Ave., Falls Church, Va.
Rothschild, R. S., Industrial Test Equipment Co., 55 E. 11 St., New York 3, N. Y.
Ruppenthal, W., 740 Hartford Ave., Los Angeles 17, Calif.
Sanders, W. E., Apt. 108, 6701—14 St., N.W., Washington 12, D. C.
Sanders, N. D., 17422 Lake Ave., Lakewood, Ohio
Schuster, D., 97-23—134 Rd., Ozone Park 16, L. I., N. Y.
Sellen, D. E., 611 Beloit Ave., Forest Park, Ill.

(Continued on page 110A)



what Aluminizing means

Aluminizing means the efficient use of light—light is energy—energy is the pay-off.

Aluminizing means a brighter TV picture, greater contrast, lower beam current, smaller spot size, sharper focus, reduced screen scorch—*all* from the efficient use of light.

On the inside of any TV tube face is a coating of phosphor crystals—the picture screen. As the electron beam—tracing the picture—strikes these crystals, they glow, giving off light in all directions. And there's the problem! Half the light thus generated is *inside* the tube, either lost to usefulness or lighting areas that should be dark. Both brightness and contrast suffer.

But—put a mirror behind the phosphor and "wandering" light is reflected back through the tube face. *Aluminizing creates this desired mirror!*

To aluminize a picture tube, deposit a nitrocellulose film evenly over the phosphor. Over that, deposit a film of aluminum only millionths of an inch thick—just thick enough to reflect the light and just thin enough to let the electrons pass through. Under heat, evaporate the nitrocellulose film to leave a thin smooth coating of aluminum. Result—an efficient light reflecting mirror to specifications.

Simple as it sounds, Rauland research engineers worked for three years to solve the problem and were among the first to do so.

Rauland

Perfection through Research

ZENITH Subsidiary

BRUSH
BRUSH

Meet the Redheads...
tops for tape recording

See how the latest additions to the Brush family of magnetic recording components can improve your tape recorders!

The BK-1090 record-reproduce head has the standard track width designed for dual track recording on ¼ inch tape. It provides unusually high resolution and uniformity over an extended frequency range. Cast resin construction assures dimensional stability, minimizes moisture absorption, and affords freedom from microphonics. Its balanced magnetic construction, precision lapped gap, Mu-metal housing, and single-hole mounting provide important design advantages.

The BK-1110 erase head has the same basic construction as the companion record-reproduce unit. Its outstanding feature is its efficient erasing at low power consumption—less than ½ voltampere.

Investigate these new "Redheads" for your magnetic recording. Your inquiries will receive the attention of capable engineers. Write Brush Electronics Company, Department F-10, 3405 Perkins Avenue, Cleveland 14, Ohio.

BRUSH ELECTRONICS COMPANY

INDUSTRIAL AND RESEARCH INSTRUMENTS
PIEZO-ELECTRIC MATERIALS • ACOUSTIC DEVICES
MAGNETIC RECORDING EQUIPMENT
ULTRASONIC EQUIPMENT

formerly
The Brush Development Co.
Brush Electronics Company is an operating unit of Clevite Corporation.

MEMBERSHIP

(Continued from page 108A)

Sinnette, J. T., Jr., 2251 Spaulding Pl., Altadena, Calif.
Soltero, V., Box Q, Radiation, Inc., Melbourne, Fla.
Southard, C. D., 901 Park St., Endicott, N. Y.
Spector, B., 40-B Iozia Ter., E. Patterson, N. J.
Steele, R. M., 503 St. Ann. Owensboro, Ky.
Stoneham, C. E., 49 E. Quincy St., North Adams, Mass.
Tamura, Y., 4055 N. Sacramento Ave., Chicago, Ill.
Taylor, G. J., c/o Graybar Electric Co., 210 S. Anderson St., Los Angeles 54, Calif.
Triche, A. B., 1552 Warren Dr., Huntsville, Ala.
Walther, A., Inst. Fur. Prak., Mathematik, Techniside Hochschule, 16 Darmstadt, Germany
Watkins, R. F., Jr., 4418 N. Maringo, Spokane 61, Wash.
Weidenhamer, B. C., Parkway Dr., South Park, Emporium, Pa.
Wheeler, D. E., 1833 Laurel Glen Rd., Santa Cruz, Calif.
Wickenden, R. C., 213-B Groves St., China Lake, Calif.
Williams, D. E., 114 Franklin St., Bldg. 6, Apt. A-1, Morristown, N. J.
Winkler, V. D., King's Court Hotel, Poughkeepsie, N. Y.
Wolfe, M. L., Sperry Gyroscope Co., Great Neck, L. I., N. Y.
Wood, M. R., Jr., 708 Cedar Ave., Richland, Wash.
Worsley, C. C., International Bldg., Suite 809–12, Washington 4, D. C.
Worthington, J. H., 6976 W. 85 St., Los Angeles 45, Calif.

PROFESSIONAL GROUP MEETINGS

INFORMATION THEORY

The Professional Group on Information Theory, Los Angeles Chapter, met recently at the Institute for Numerical Analysis, University of California at Los Angeles, with R. B. Conn presiding. J. T. Culbertson, Rand Corporation, presented a paper, "Sense Data in Robots and Organisms."

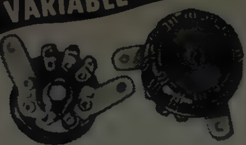
This group met again at the Institute for Numerical Analysis, under the chairmanship of R. B. Conn, to hear J. C. Fletcher, Head, Theory and Analysis Department, Hughes R and D Labs., present a paper, "Applications of Information Theory to Electronic Guidance Systems."

ELECTRONIC COMPUTERS

The Professional Groups on Electronic Computers, Los Angeles Chapter, met recently at INA-UCLA. W. F. Gunning acted as chairman for the meeting.

M. Rosenberg and S. Williams of International Telemeter Corp. and D. Buck of Massachusetts Institute of Technology presented a paper, "Magnetic Core Devices," which described the operation and present state of magnetic core memories. The fact that the cores are useful as switching elements, and that an entire computer could be made from them was also pointed out.

1 VARIABLE RESISTORS


Model 1 Radiohm® Miniature

Model 2 Radiohm

Model 2 Radiohm (including JAN types)

Model 2 EXPRESS (†) for immediate production needs

Compentrol (†) Infinitely variable loudness control

2 SWITCHES

Series 20 Miniature Phenolic or Steatite Insulation

Standard Size Phenolic or Steatite Insulation

Lever Switch

FOR SALE!

These and 100,001 other electronic components for increased performance . . . by the industry's most experienced and No. 1 electronic component source

WHETHER you buy electronic components in small lots or by the carload — here's why it's good business to concentrate your five major electronic components problems with Centralab:

- Centralab has pioneered more electronic "firsts" than any manufacturer in the field.
- Centralab Printed Electronic Circuits offer a new concept in reducing extra parts, assembly-time, errors and costs.
- Centralab ceramics are second to none—available in grade *L5 and L6 Steatite.*
- You can count on the production facilities of *seven* conveniently located plants.
- Continuous CRL product improvement.
- Unequaled engineering assistance for developing specific TV, FM, military and commercial electronic components.

Centralab electronic components are the result of more than 30 years' experience working in cooperation with manufacturers all over the world. For complete performance data and engineering specifications on products shown — check and mail the coupon.

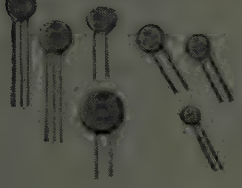
†Trademark

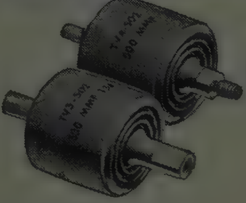
Series 30 Dual Concentric Switches and/or Controls Combinations

Tone Switch

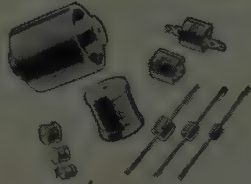
3 CAPACITORS

BC Tubular TC Tubular


BC Discs TC Discs



TV HI-VO-KAPS®

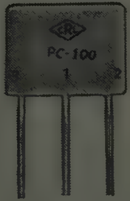

Transmitting Capacitors

Ceramic Trimmers

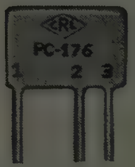
4 P.E.C.

Miniature Resistor and Resistor-Capacitor Units

CRL
PC-70
1 2 3 4
Standard Triode Couplate®

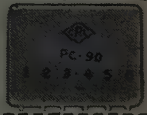


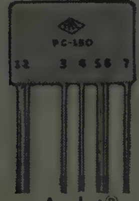
Vertical Integrator



Special Plates to suit manufacturer's requirements

CRL
PC-30
1 2 3 4





Audet® Audio-detector plate

5 CERAMICS

Custom Ceramics (Steatite, Centradite, Zirconite.)

Metalized Ceramics

Centralab

A Division of Globe-Union Inc.
920-J East Keefe Ave., Milwaukee 1, Wisconsin
In Canada, Box 208, Ajax, Canada

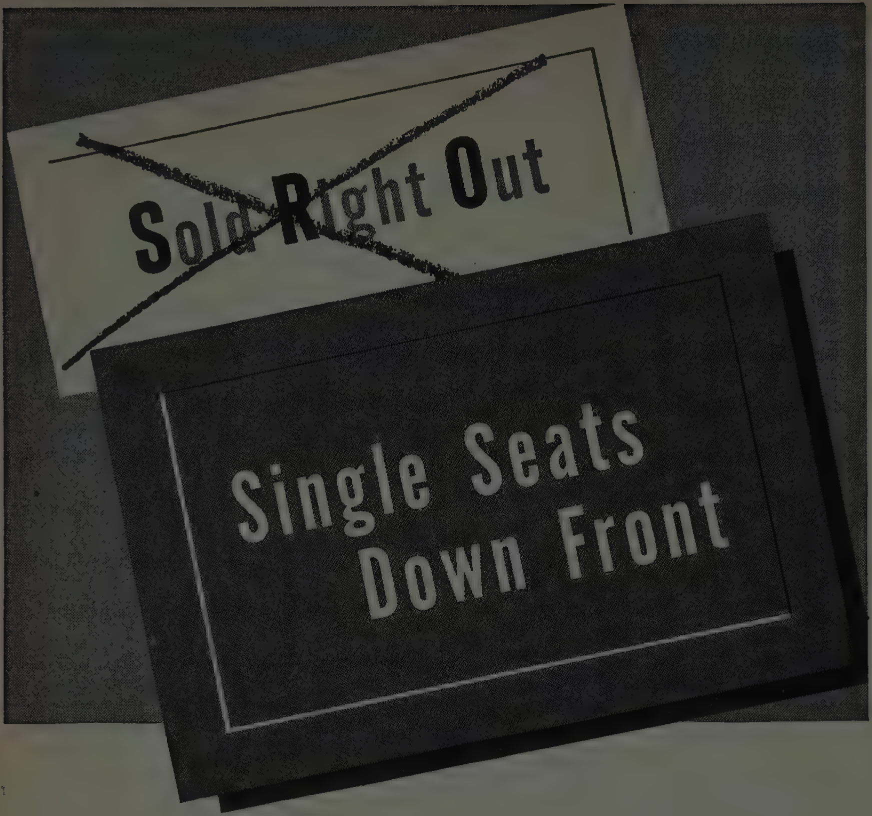
Please send me information on these Centralab products:
☐ Controls ☐ Switches ☐ Capacitors
☐ Printed Electronic Circuits ☐ Ceramics

Name............................Title............................

Company............................

Address............................

City............................Zone.........State............................



Our previous series of advertisements in this publication explained, in theatrical parlance, that our design and production facilities were pretty well "sold out" by the requirements of our present customers.

Now, we are happy to say (because we enjoy making new friends) that some of the heat has been taken off, and we are able to announce "Limited seating available"—as they say at the box office.

We shall be happy to talk with you about your present and/or future needs.

L. H. Terpening Company
DESIGN • RESEARCH • PRODUCTION
Microwave Transmission Lines and Associated Components
16 W. 61st St. • New York 23, N. Y. • Circle 6-4760

TRADE MARK

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 56A)

Coincidence-Anticoincidence Scaler

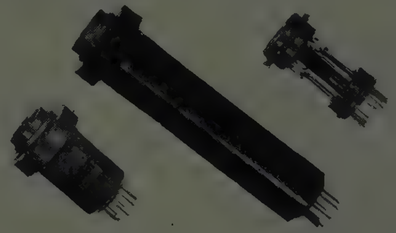
A new Model 400 Coincidence-Anticoincidence Scaler is now available from **Radiation Instrument Development Laboratory,** 2337 W. 67th St., Chicago 36, Ill. All four channels may be used for coincidence counting with the fourth channel, also designed specifically for anticoincidence counting.

The scaler is self contained, and is especially suitable for cosmic ray research as well as other coincidence-anticoincidence applications.

The input sensitivity is negative 1 volt. Dead time is less than 10 microseconds. A scale of 64 with scale selection of 4, 8, 16, 32, or 64, is provided. Counter voltage is continuously variable from 500 to 2,500 volts with electronic regulation of 0.01 per cent, per 1 per cent change in line voltage. The meter is 4½ inches and calibrated to 1 per cent of full scale.

Tube Socket Test Adapters

Vector Electronic Co., 3352 San Fernando Rd., Los Angeles 65, Calif., has developed several new tube socket test adapters used for making voltage, resistance and wave form measurements from the tube side of electronic equipment.



In testing, the adapter is inserted between the electronic tube and its socket, completing the circuit and providing convenient test tabs. Adapters are made for nine socket types. For most work the short, unshielded adapters (see left figure) are adequate, but for hard to reach locations a longer adapter with shielded leads is available (see center figure). Where there is a need to break tube circuits or alter the pin connections the "Experimenter" type is available (see right figure). This third type also provides means for adapting tubes to non-mating sockets.

(Continued on page 117A)

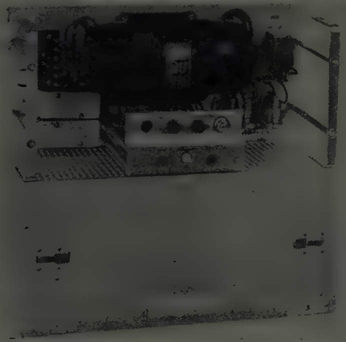
News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 114A)

Emergency AC Power Supplies

Up to 250 watts of 110 volt ac power can be obtained from 24 to 48 volt storage batteries with new Types 5060A and 5070A emergency ac power supplies, manufactured by **Lenkurt Electric Co.**, 1105 County Road, San Carlos, Calif.



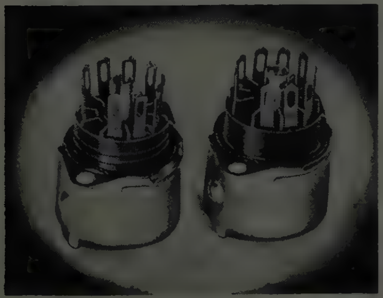
Designed to meet a wide range of applications where ac operated equipment (at attended or unattended locations) cannot be interrupted for even short intervals, these emergency power supplies are particularly suitable for use with communications equipment. The rated load capacity is ample to assure uninterrupted operation of a complete three-channel carrier terminal, a carrier repeater, a small radio station, or similar equipment.

Automatic transfer to the emergency source is completed within 0.5 seconds after failure of the normal ac power. The emergency supply is equipped so the load can be returned to the normal source either automatically or manually when power is restored.

With all control circuits and a dependable rotary converter mounted on one side of an aluminum chassis, Lenkurt emergency power supplies can be either wall mounted or installed on a standard 19 inch relay rack. A snap-on aluminum dust cover allows access to test and rest controls.

Complete specifications are listed in Lenkurt bulletin 5060A-P2.

Kel-F Tube Sockets



An increase in the performance altitude "ceiling" of an electrontube by 15 per cent resulted from extending the insulating bar-

(Continued on page 118A)

IT'S TIME FOR
TALK OF DOLLARS
AND SENSE
in

Buying Shielded Enclosures

for suppressing r-f interference

If you're thinking of buying a shielded enclosure, chances are you'll be faced with technical claims that are apt to be confusing. Worse yet, you might end up with an enclosure that does not come up to *your interpretation* of the claims, or does not maintain its initial rating. It pays to investigate.

To help you in choosing the best enclosure for your needs, Ace has just prepared a booklet which interprets the confusing nomenclature of this fast-growing industry. Written by Richard B. Schulz, Electro-Search, consulting engineer for Ace, it enables you to evaluate answers to such questions at the right . . . questions you must ask to get your money's worth. You'll quickly learn whether a manufacturer's claims are based upon guaranteed measurements or *just plain guesswork!*

Write for *Your Money's Worth in Shielded Enclosures.* IT'S FREE.

HOW TO GET WHAT YOU PAY FOR

Ask the manufacturer these questions—

1. What is the guaranteed attenuation (not insertion loss) of your shielded enclosure from ______mc to ______mc?
2. Is this guarantee based upon actual test data?
3. If so, what is your method of measurement and by whom performed?
4. Does this method measure the attenuation to (a) a plane wave, (b) an electric induction field, or (c) some combination of these?
5. Were power line filters installed at time of measurement? If so, which filters?
6. Is the guaranteed attenuation of power line filters (terminated in 50 ohms) at least as high as overall room attenuation over same frequency range?
7. What test data support this guarantee?
8. Is the enclosure bolted from the inside or the outside?
9. Are panels interchangeable? Can the door be placed in any wall position, including corners, without special adaptation?
10. Can the room be increased in width as well as in length?

Send for FREE booklet that tells you how to evaluate the answers to these important questions.

Ace Shielded Enclosures

First and Still Finest By Every Measuring Standard

The highest attenuation known to the electronic industry . . . attenuation over the widest frequency range—these are characteristic of Ace Shielded Enclosures. Years of shielding production, coupled with the knowledge of the nation's top shielding engineers give you the ultimate in shielding effectiveness.

There's no guesswork with Ace, just plain fact. And reams of guaranteed test data to back it up. Every enclosure design is thoroughly tested and approved by independent engineering laboratories to clearly prove their full value. That's why, year after year, Ace remains the country's largest shielded enclosure manufacturer . . . with more satisfactory installations than any other.

A COMPLETE LINE OF SCREEN ROOMS
FOR INDUSTRY, SCIENCE, AND MILITARY
JAN-1-225; 16E4 (ships); MIL 16910; MIL-S-4957
(Write for Engineering Bulletin No. 3)

ACE ENGINEERING & MACHINE CO., INC.
3644 N. Lawrence Street • Philadelphia 23, Pennsylvania

... Complete line of Microwave Components from magnetron to antenna...
designed and produced by experts—

WAVEGUIDE SWITCH
A complete line; compact, rugged, suitable for military usage; VSWR less than 1.10; crosstalk greater than 50 Db; operation 24 v. DC, 110 v. AC; may be specially designed to meet switching problems.

MIXER DUPLEXER
Precision-built to closest tolerances; completely tested. Designed to meet your basic requirements, or produced from your blueprints.

DUMMY LOADS
Designed for military field operation; built to meet all standard military vibrations and shock requirements. Capable of operating at extremely high average powers.

FLEXAGUIDE
Pressure-tight; rugged enough to meet roughest requirements; VSWR less than 1.10; attenuation equal to brass rigid guide.

COUPLERS
Complete series for all waveguide sizes. Flange combination, and waveguide or coaxial outputs. Designed to meet your particular problems.

For RIGID Waveguide Specify
GUIDELINE
Rigid Bends • Twists • Tapers • Crystal Mixers • Duplexers
Flanges • Magic Tees • Directional Couplers • Dummy Loads
Waveguide Switches • Coax Adaptors • Precision Castings
Waveguide Transformers • Quick Disconnect Clamps

For FLEXIBLE Waveguide Specify
FLEXAGUIDE
Army and Navy Standard Waveguides
Flexible Twists • Bends • Tapers
Straight Sections • All Lengths and Sizes

Write for Catalogs

Airtron inc
Linden, New Jersey

BRANCH OFFICES
DAYTON CHICAGO LOS ANGELES DALLAS
KANSAS CITY SEATTLE ALBUQUERQUE

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 117A)

riers on the socket base and using "Kel-F" trifluorochloroethylene polymer as the socket insulation. The high dielectric strength of "Kel-F" prevented ionization and arc-over which previously ruled out use of the tube at the higher altitude. Because of the exceptionally high mechanical strength of this fluorocarbon plastic, the barriers can be made thin and are able to stand up under heavy shock and vibration without damage.

The new miniature tube socket is injection molded by the **Elco Corp.**, Philadelphia, Pa., from "Kel-F" trifluorochloroethylene polymer, a product of the **M. W. Kellogg Co.**, P.O. Box 469, Jersey City, N. J.

Additional advantages for the new socket stem from the zero water absorption and non-wettability of the "Kel-F," precluding electrical leakage in contact with water and the formation of conductive fungus. The non-flammability and non-carbonizing characteristics of the insulation permit the use of the socket at high temperatures (up to 390°F) without damage or loss of efficiency.

For further information write to Technical Service, Chemical Manufacturing Div., The M. W. Kellogg Co.

(Continued on page 120A)

NOW Convert mechanical motion to electrical energy
with Electro Magnetic Pick-up
Model 3010-A

generates up to 28 v. without contact

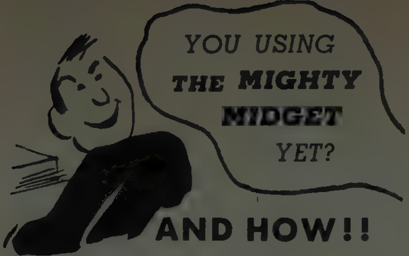
Small, compact and rugged, this Electro Magnetic Pick-up generates electrical voltages proportional to the rate of speed of any object with magnetic properties. It produces useful output voltages at frequencies up to 75,000 cps. Self-energized by built-in magnet. Low cost permits use in production machinery.

A Few of Many Applications
- Indicates rate of motion
- Acceleration and velocity studies
- For precision ignition timing
- For ballistic research

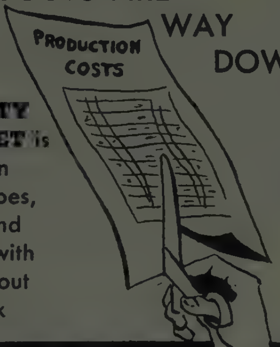
Write for Bulletin MT-592

Electro
ELECTRONIC EQUIPMENT

ELECTRO PRODUCTS LABORATORIES
4501-REu Ravenswood, Chicago 40


YOU USING THE MIGHTY MIDGET YET?

AND HOW!!
MY COSTS ARE WAY DOWN



THE MIGHTY MIDGET is made in all shapes, sizes and alloys with or without self-flux

SOFT SOLDER
PREFORMS

MADE BY **ALPHA**

SPEED AUTOMATIC SOLDERING

for flame, oven or induction heating

Increase Production • Melts Faster • Guarantee Product Precision • With Or Without Self-Flux Save Labor Costs • Designed For Your Application All Sizes, Shapes, Alloys • Stronger, Smoother Joints

Alpha's preformed solders, in any shape or size, cut many hours from your production time. You can select washers, rings, coils, cut shapes, drops, pellets, solder foil, to fit your specific needs. They save you considerable money and materials in repetitive soldering processes.

AVAILABLE IN

- **★ CEN-TRI-CORE** *ENERGIZED* **ROSIN-FILLED**
- **★ TRI-CORE** *LEAK-PRUF* **ACID-FILLED**
- **★ SINGLE-CORE**
- **★ SOLID WIRE**
- **★ SHEET SOLDER**

Please consult us on your soldering problems. Trained Field Engineers always available to assist you. Small or large quantities.

for further information

write . . .

ALPHA METALS, INC.
61 Water St., Jersey City 4, N.J.
Specialists IN SOLDER For Over 50 Years

---

teflon*

. . . and We Can Deliver!

EXTRUDED MOLDED ROD and TUBE

Small Machined Parts! Sheets!

Heavy demand has put many TEFLON fabricators in a "back ordered" condition. The effect — stymied or crippled production on your end.

At FLEXROCK we have licked this problem. New TEFLON producing equipment has been added. We have substantially increased capacity. We can't take on all things just yet. But soon we will be ready to "throw the book at you" with a complete range of TEFLON services. RIGHT NOW we are set to ship you TEFLON Rod and Tube, extruded or molded, Sheets, and small parts — no matter how intricate — machined from Rod and Tube. We can promise good delivery — yes, FAST DELIVERY . . . with closest possible tolerances on your small parts. Tell us your needs — we will be happy to quote delivery and price.

**DuPont trade-mark for tetrafluoroethylene resin*

for teflon it's
FLEXROCK
PHILADELPHIA 4, PA.

SEND US YOUR "SPECS"
LET US QUOTE

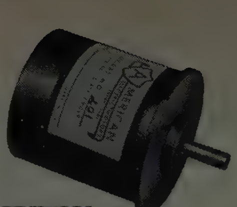
FLEXROCK COMPANY, 3608-A Filbert St., Phila. 4, Pa.

☐ *We are enclosing sample, specs, and quantity for our TEFLON requirements. Please furnish quotation.*
☐ *Please send us your TEFLON Bulletin including stock list.*

Name ....
Company ....
Address ....
City .... Zone .... State ....

AMERICAN ELECTRIC
Miniature Motors

Weigh only OUNCES yet deliver
POWER-HOUSE PERFORMANCE
Aloft or Aground!



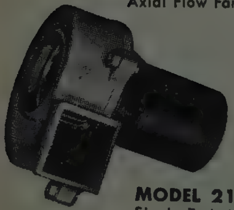
MODEL 201
Hysteresis Type
Synchronous Drive Motor

MODEL 228
Induction Drive Motor

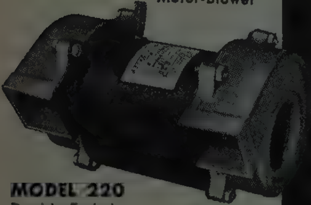
MODEL 300
Reluctance Type
Synchronous Drive Motor

MODEL 168
Propeller Fan

MODEL 182A
Axial Flow Fan



MODEL 219
Single Ended
Motor-Blower



MODEL 220
Double Ended
Motor-Blower

Need low weight for mechanization of airborne gear . . . want unusual compactness for ground equipment? AMERICAN ELECTRIC can provide the drive motor to fit your specialized requirements.

These miniatures are built as small as 1.45 inches in diameter . . . Even the "big boys" measure only 3⁵⁄₁₆ inches across! Yet with all their diminutive size and weight AMERICAN ELECTRIC Miniatures are regular "power-houses" in their field . . . *designed to utilize all magnetic materials to the ultimate, thus reducing useless, "no-pay" weight to an absolute minimum!*

No design compromises—AMERICAN ELECTRIC offers the greatest range of production and prototype models available today! Let AMERICAN ELECTRIC quote on your miniature motor requirements. Write, wire or phone today!

TWO MINIATURE DRIVE MOTOR TYPES

Induction Motors—Output torque range: ½ in. oz. to 120 in. oz.

Synchronous Motors—Output torque range: .01 in. oz. to 10 in. oz. in both Hysteresis and Reluctance types.

TWO MINIATURE COOLING TYPES

Centrifugal Blowers
Propeller Fans

Manufacturers also of HIGH FREQUENCY POWER SUPPLIES Inductor-Alternator type, 500 Watts to 75 KVA output. Portable, Semi-Portable and Stationary Types.

AMERICAN ELECTRIC MOTORS
TRADE MARK

4811 Telegraph Road,
Los Angeles 22,
California

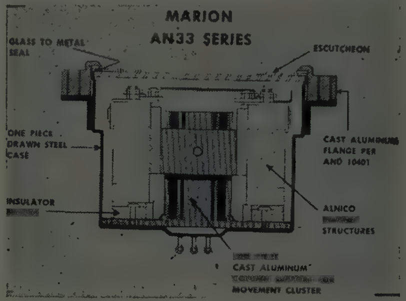
Engineering Representatives: TRAVCO ENGINEERING CO.
Silver Spring (Md.), Chicago, New York, Los Angeles

News—New Products

(Continued from page 118A)

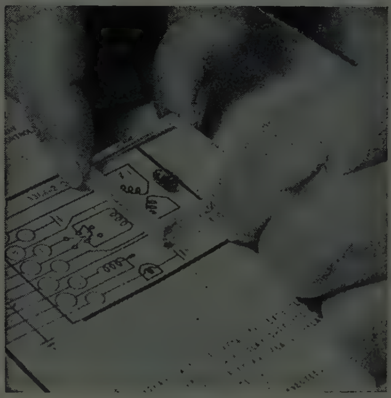
Hermetically Sealed Instruments

A series of improved multi-element aircraft instruments has been announced by **Marion Electrical Instrument Co.,** Manchester, N. H.



The series consists of single-seal glass-to-metal hermetically-sealed aircraft elements which incorporate the Marion ruggedized D'Arsonval movements and a unique columnar construction providing greater rigidity and more precise alignment. Available as two element (Model AN32E), three element (Model AN33E) and four element (Model AN34E) types. Applications include: ammeters, voltmeters, radio navigational types (such as omni-ranges and ILS), temperature indicators and others. The instruments meet AND 10401 dimensional requirements for 2¾ inch dial instruments.

(Continued on page 122A)



DON'T DRAW IT!
—PRINT IT—

- TRANSPARENT
- ASA Standard Symbols
- 27 Stamps Per Kit
- Large Selection
- Special Pads
- Opaque Ink
- Under $30.00

John Griffin Company
2157 James Avenue
St. Paul 5, Minn.

Improve Tube Performance with WESGO "AL-300" ALUMINA INSULATORS

- 97% Al_2O_3 content
- Vacuum tight—extraordinary strength
- Low loss factor — High Te value
- Non "gassing" — no poisoning of emitters
- High strength at all temperatures up to 1500°C.
- Can be supplied in most any shape to extremely close tolerances

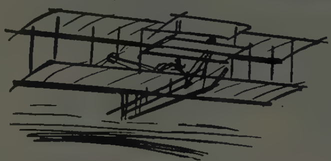
Our Engineering Department will gladly answer all inquiries relative to your particular problems

WESTERN GOLD & PLATINUM WORKS
Ceramic Division
589 BRYANT STREET
SAN FRANCISCO, CALIF.

From Kitty Hawk Through the Sound Barrier

Heiland

500B



RECORDING OSCILLOGRAPH

Since the Wright Brothers ushered in the age of flight, aviation has soared beyond the speed of sound and into the outer reaches of the earth's atmosphere. Heiland Recording Oscillographs are a vital factor in this dramatic conquest of the air. These highly sensitive, extremely accurate and dependable instruments enable testing engineers and scientists to solve the wide variety of aeronautical problems involving the measurement of physical phenomena such as strains, stresses, vibrations, pressures, temperatures, accelerations, impact, etc. This technical information, provided by Heiland Recording Oscillographs, makes possible the design and production of superior aircraft. Other industries the world over have proven these instruments to be invaluable in meeting similar demands in their applications.

FEATURES AND SPECIFICATIONS

Heiland Model 500B Portable Recording Oscillograph

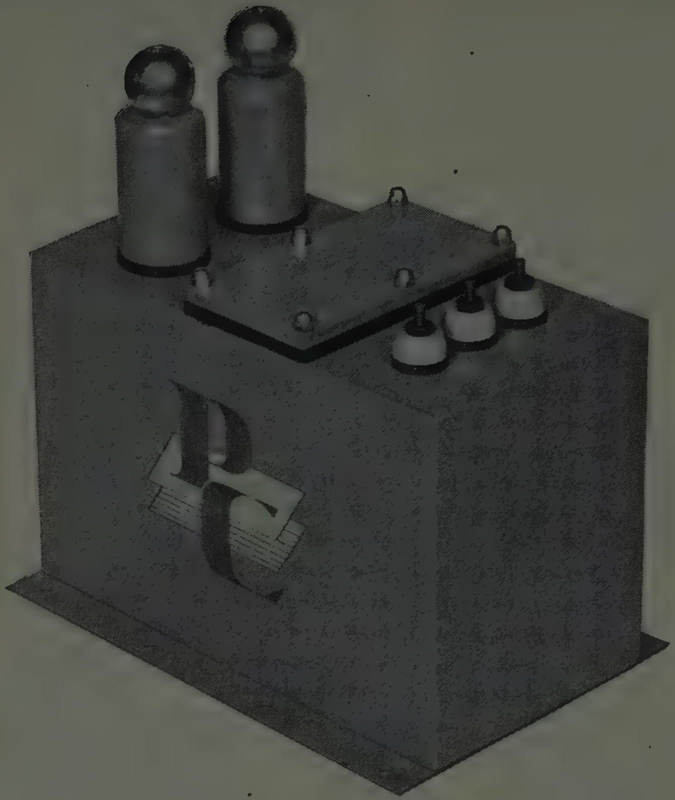
- **Compact and lightweight**
- **Provides maximum portability and versatility where desired to record up to 12 phenomena**
- **Direct monitoring while recording**
- **4 record speeds instantly selectable**

Galvanometers: Up to 12. **Record width:** 4". **Magazine capacity:** 100'. **Record speeds:** 3, 6, 12 and 24 inches per second selected by levers on control panel. Other speeds, ranging from 1/32" to 24" per second, can be obtained by changing drive sprockets and motor gear box ratios. **Drive:** Two-speed governor controlled motor. **Power supply:** 23.5 to 28.25 volts D.C. **Timer:** Chronometric timing unit projects 100 time lines per second across record width, the 1/10 second lines being heavier. 1/10 and 1 second time lines are available. **Mounts:** Detachable shock or vibration mounted base. **Case dimensions:** 6-3/4" x 9-13/16" x 12-3/4". **Weight:** 33 lbs.

Write today for free catalog of Heiland equipment including 500B and A-401 Portable Recording Oscillographs, "700" series Multi-Channel Recording Oscillographs, "82-6" Bridge Balance and Strain Indicator, Amplifier System, Galvanometers and accessories.

Heiland Research Corporation 130 East Fifth Ave., Denver, Colorado

"High Voltage POWER PACKS"



APPLICATIONS:

For the operation of display tubes of all types, insulation and breakdown testers, precipitators, Geiger counters, Alpha counters, flocking, air samplers, dust collectors and general laboratory use.

FEATURES:

- operation with line frequency input of 60 cycles
- rectifier tubes can be replaced in the field
- can be used with Variac to control output voltage from zero to maximum design voltage
- hermetically sealed

ILLUSTRATED:

Model HV 200-102; delivering 20,000 volts at 1 ma with 118V, 60 cycle input, size: 4½" W x 7¾" L x 5½" H.

STANDARD Power Packs: for sea level operation and temperature range of minus 60° C to plus 70° C, voltage ranges from 2000 to 60,000 volts, current from 1 ma to 5 ma.

SPECIAL Power Packs: designed to suit your particular electrical and mechanical requirements—for all standard frequencies to 1500 cycles.

We invite your inquiries

Ask for our complete catalog on your company letterhead

Plastic Film Capacitors • High Voltage Power Packs • Pulse Forming Networks

Plastic Capacitors, Inc.
2511 W. MOFFAT STREET, CHICAGO 47, ILLINOIS

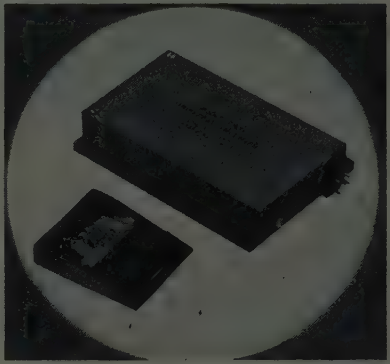
News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 120A)

New Amplifier

Endevco Corp., 689 South Fair Oaks Ave., Pasadena 2, Calif., has a new subminiature, ruggedized amplifier. Accomplished by using subminiaturized components and etched circuit wiring, the model 2607 Amplifier provides an input impedance of over 150 megohms for piezoelectric, capacitive, and other types of measuring instruments.

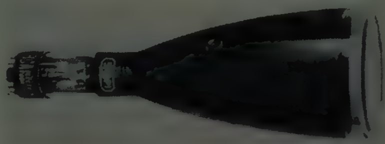


This amplifier, when combined with the Endevco "Thimble-sized" Series 2200 Accelerometers, lends itself to installation in missiles, aircraft, or ground tests where ambient conditions of temperature and vibration are severe. The selectable gain ratios of 10, 30, or 100 allow for a full 5.0 volts output from an accelerometer generating 10 mv/g when measuring 5 g's of acceleration or vibration.

Although the amplifier was designed for use with Endevco accelerometers and the telemetering of vibration and shock data from 5 cps to 20 kc, other uses in fields such as dc strain gage amplification are possible.

Oscillograph Tubes

Tube Dept., Radio Corp. of America, Harrison, N. J., recently announced the 5ABP1, 5ABP7, and 5ABP11, a new series of 5-inch, flat-face, cathode-ray tubes, utilizing electrostatic focus, electrostatic deflection, and post-deflection acceleration. The three differ only in the spectral-energy emission and persistence characteristics of their respective phosphors P1, P7, and P11.



Among the features of the 5AB types are the exceptionally high sensitivity and low capacitance of the pair of deflecting electrodes provided for vertical deflection. These characteristics make this pair of electrodes especially suited for operation from wide-band amplifiers, the high sensi-

(Continued on page 124A)

WHERE RESISTANCE TO HIGH AND LOW TEMPERATURES IS VITAL

Surflene

INSULATED HOOK-UP WIRE

Resists

- **HEAT**
- **FUNGI**
- **ABRASION**
- **CHEMICALS**

"Surflene", extruded monochlorotrifluoroethylene, has high insulation resistance, dielectric strength and outstanding resistance to heat, abrasion, most chemicals and concentrated acids, including fuming nitric acid. It is non-inflammable and inert to fungi. It is especially designed for hermetically sealed and water-proof equipment and for high temperatures encountered in power supply and continuous duty apparatus. Also available in multi-conductor cables.

"Surflene" is available in thirteen colors — red, orange, yellow, pink, light and dark green, blue, gray, tan, brown, black, white and clear.

Write our Engineering Service TODAY for technical assistance.

Surprenant MFG. CO.
199 Washington St. Boston 8, Mass. Plant—Clinton, Mass.
Engineered Wire and Cable for the Electronic and Aircraft Industries

---

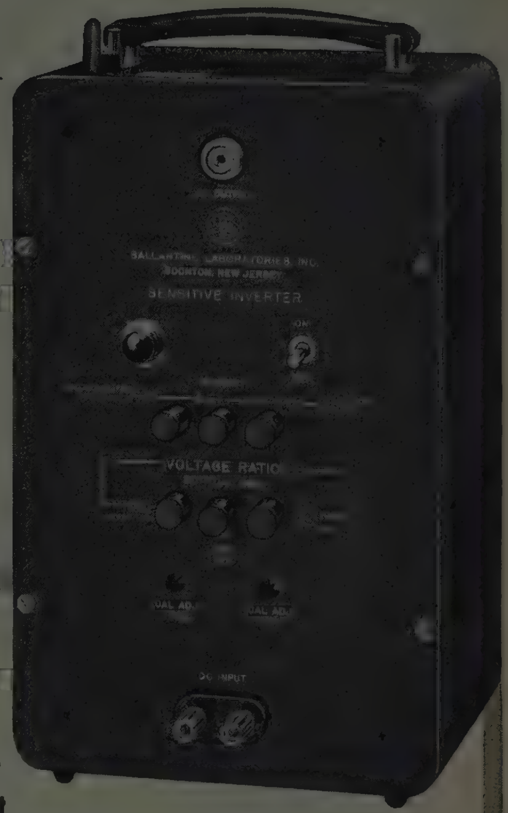
New BALLANTINE SENSITIVE INVERTER

for the precise measurement of small DC potentials

from
10µv — 100v

Threshold Sensitivity
1 µv

FOR USE WITH
Vacuum Tube Voltmeters
Oscilloscopes
Voltage Amplifiers
Multimeters
Servo-Amplifiers



MODEL 700

FEATURES

- Built-in Calibrator
- High Sensitivity
- High Input Resistance
- Distortion-free Output
- Low Noise Level
- Accurate for 50-70 cps Line Frequencies
- Polarity Sensing
- Immune to 60 cps Stray Magnetic Fields

SPECIFICATIONS—MODEL 700

INPUT VOLTAGE RANGE	10 µv—100 v DC (Sensitive to 1 µv)
VOLTAGE RATIOS (DC input to AC RMS output)	1:100 & 10:1
INVERSION STABILITY (>100 µv input)	1%
CALIBRATOR ACCURACY	0.25%
DC INPUT RESISTANCE	10 meg for 1:100; 50 meg for 10:1
AC INPUT IMPEDANCE	>200k
INPUT NOISE LEVEL	Approx. 3 µv
AC OUTPUT FREQUENCY	Line Frequency
MAX AC OUTPUT LEVEL	10 v RMS
TOTAL DISTORTION IN OUTPUT WAVE FORM	<2%
RESPONSE TIME (90% of Final Amplitude)	0.25%
POWER REQUIREMENTS	105-125 v; 50-70 cps; 15 watts

BALLANTINE LABORATORIES, INC.
102 Fanny Road, Boonton, N.J.

Increased Combat Effectiveness
and Operational Safety
SERVOMECHANISMS INC.
PACKAGED FUNCTIONAL COMPONENTS

In our front line aircraft, throughout the world, the philosophy of "packaged electronic functions" developed by Servomechanisms, Inc. to a high degree of refinement, insures:

- maximum reliability
- ease of maintenance
- complete interchangeability

A typical Servomechanisms, Inc. analog computer and companion transducer featuring plug-in components and pre-wired chassis—each electronic "building block" easily removable... simple to check and service.

For further information on specific applications write to Dept. CLO-5.

WESTBURY DIVISION .... POST AND STEWART AVES., WESTBURY, N. Y.
EL SEGUNDO DIVISION. .... 316 WASHINGTON ST., EL SEGUNDO, CALIF.

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

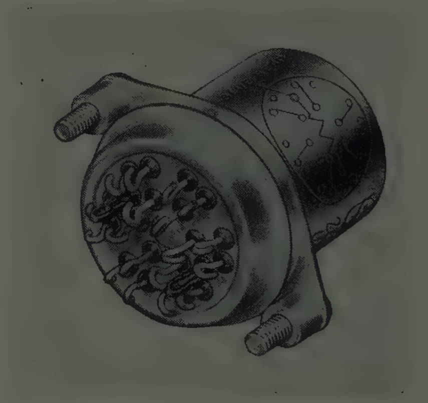
(Continued from page 122A)

tivity making up for the low-signal output of such amplifiers, and the low capacitance providing the type of load into which such amplifiers work best. Also, the pair of deflecting electrodes providing horizontal deflection has higher sensitivity than previous similar types while retaining full-screen scan.

The 5 AB-types can generally be substituted for the corresponding older 5C types to give improved performance.

Hermetically Sealed Relay

Union Switch & Signal, Div. of Westinghouse Air Brake Co., Dept. 67, 1789–1807 Braddock Ave., Pittsburgh 18, Pa., has designed and tested for meeting the requirements of Military Specifications MIL-R-5757 A and B, the "Union" Type M, 6 pdt hermetically-sealed relays, claimed to be one of the smallest and lightest in the miniature field. It weighs 3.5 ounces and has a volume of 1.5 cubic inches.



Within the requirements of the two specifications, it has the following ratings: shock resistance of 40 g's for 0.010 second under any conditions without malfunctioning; vibration range of 10 to 55 cps, 0.060 total excursion; temperature ranges of −55 to 85°C and −65 to 125°C; maximum pull-in voltage of 18 volts at maximum rated temperature; and minimum life expectancy of 1,000,000 operations.

Standard contact ratings are 2 amperes (resistive) for 100,000 operations (8 amperes overload resistive for 100 cps) at 26.5 volts dc. Coil resistances for both temperature ranges are 325 ohms.

Figures quoted above are for relays designed to meet the stated military specifications. Relays can also be obtained with contacts rated for higher voltages, both dc and ac, and with rated vibration resistances up to 1,000 cps. Contact loads of 100 ma at 400 volts dc for over 500,000 operations have been successfully handled by two contacts in series. Relays can be furnished in a variety of mountings, including plug-in.

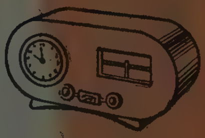
(Continued on page 126A)

Definitely Different...

AEROVOX
PRINTED WIRING

An improved method of Printed Wiring is now available. Aerovox offers a *definitely different* and improved technique. Cleaner, finer, more accurate detail; phenolic characteristics actually improved rather than impaired in processing; complete absence of corrosive agents; conductor of pure silver; conductor permanently bonded to base material without adhesives; excellent solderability. Obviously, Aerovox Printed Wiring is unique.

Meanwhile, the advantages of printed wiring are well established, notably; (1) Lower assembly costs; (2) Dip soldering eliminates individual soldering; (3) No lead dress required; (4) All circuits precisely the same — no wiring mistakes to trouble-shoot; (5) Miniaturized assemblies — greater compactness and lessened weight; (6) Markings can be incorporated, eliminating assembly errors.



CHECK LIST OF FEATURES...

- ✓ Metallic silver conductor, mechanically formed.
- ✓ Phenolic base material not subjected to acid or chemical deterioration.
- ✓ Excellent bond — silver partially imbedded in phenolic base material — not dependent on adhesive.
- ✓ Readily solderable — either dip soldering or iron soldering.
- ✓ Negligible oxidation or tarnishing under normal conditions.
- ✓ No surface plating required for most switching circuits or normal protection.
- ✓ Temperature range of —65°C to +125°C will not affect bond.
- ✓ Identically reproducible, due to precision printing technique.
- ✓ Available in production — any quantities — meeting *any* reasonable delivery schedules.

Literature, with representative sample, on request.
Let us quote on *any* wiring, switching or commutating problems; *any* quantities. Please write on your company letterhead to AEROVOX CORPORATION, Dept. P.W., New Bedford, Mass.

AEROVOX CORPORATION

NEW BEDFORD, MASS.

HI-Q® DIVISION
OLEAN, N. Y.

ACME ELECTRONICS, INC.
PASADENA 4, CALIF.

Export: 41 E. 42nd St., New York 17, N. Y. • Cable: AEROCAP, N. Y. • In Canada: AEROVOX CANADA LTD., Hamilton, Ont. JOBBER ADDRESS: 740 Belleville Ave., New Bedford, Mass.

What is your Delay or Regulating Problem?

For the most effective solution use the
SIMPLEST, MOST COMPACT
MOST ECONOMICAL
HERMETICALLY SEALED

AMPERITE
THERMOSTATIC DELAY RELAYS

Provide delays ranging from 2 to 120 seconds.

- Actuated by a heater, they operate on A.C., D.C., or Pulsating Current.
- *Hermetically sealed.* Not affected by altitude, moisture, or other climate changes.
- Circuits: *SPST only*—normally open or normally closed.

Amperite Thermostatic Delay Relays are compensated for ambient temperature changes from −55° to +70°C. Heaters consume approximately 2 W. and may be operated continuously. The units are *most compact, rugged, explosion-proof, long-lived, and—very inexpensive!*

TYPES: Standard Radio Octal, and 9-Pin Miniature.

PROBLEM? Send for Bulletin No. TR-81

BALLAST-REGULATORS

- Amperite Regulators are designed to keep the current in a circuit ***automatically regulated*** at a definite value (for example, 0.5 amp).
- For currents of 60 ma. to 5 amps. Operates on *A.C., D.C., or Pulsating Current.*
- Hermetically sealed, light, compact, and most inexpensive.

Maximum Wattage Dissipation: T6½L—5W. T9—10W.

Amperite Regulators are the simplest, most effective method for obtaining *automatic regulation* of current or voltage. ***Hermetically sealed,*** they are not affected by changes in altitude, ambient temperature (−55° to +90°C), or humidity. Rugged; no moving parts; changed as easily as a radio tube.

Write for 4-page Technical Bulletin No. AB-51

AMPERITE CO., Inc. 561 Broadway, New York 12, N. Y.
In Canada: Atlas Radio Corp., Ltd., 560 King St., W., Toronto 2B

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 124A)

Junction Transistors

The General Electric Co., Syracuse, N. Y., announced it is beginning production of new all-welded junction transitors with essentially infinite life expectancies.

The new units are evacuated, hermetically-sealed, and of all-welded metal construction. They are claimed to be the first to have all-welded construction, which eliminates the aging effects of moisture and trapped solder flux fumes.

The new construction allows power ratings up to three times those of any previously announced transistors. It has been designed to permit automatic mass production, and an automatic factory is now being developed. While some basic machines already are in use, the total mechanization of transistor production will be an evolutionary process.

Pilot production of the all-welded transistors is now under way at Electronics Park. Similar production lines are being established at the company's germanium products plant at Clyde, N. Y., with sample quantities of the new transistors scheduled for September.

The welded metal construction allows power ratings of almost one watt, with two units in a Class B push-pull circuit. They have been demonstrated to operate under water at temperatures up to 100°C.

The new transistors have been designed to meet military requirements, and the use of automatic machinery in their manufacture will assure a product uniformity never before possible.

New Brochure

A new four page brochure has been published by **Stupakoff Ceramic & Manufacturing Co.,** Latrobe, Pa., for the electronics industry. Included in the brochure are photographs and descriptive details about glass-to-metal seals, steatite and other ceramics, printed circuits and ceramic-metal assemblies. A section also is devoted to a description of the characteristics of Kovar Glass-Sealing Alloy.

Copies of this brochure, Bulletin No. 654, may be obtained by writing to Stupakoff.

(Continued on page 130A)

Type U70, 3/4″ diameter *miniaturized* variable composition resistor with special printed circuit terminals. Wattage rating: .3 watt for resistances through 10,000 ohms, .2 watt with 350 volts maximum across end terminals for resistances over 10,000 ohms.

Type U45, 15/16″ diameter, variable composition resistor with blade-type printed circuit terminals. Wattage rating: 1/2 watt for resistances through 10,000 ohms, 1/3 watt for resistances over 10,000 ohms through 100,000 ohms and 1/4 watt with 500 volts maximum across end terminals for resistances over 100,000 ohms.

Type GC-U45, 15/16″ diameter, variable composition resistor with blade-type printed circuit terminals same as U45 except with attached SPST, 3 ampere, 125 volt "GC" type switch. Also available with type "WF", DPST, 3 ampere, 125 volt switch. (Variable resistor type WF-U45.)

CTS

CHICAGO TELEPHONE SUPPLY
Corporation

ELKHART • INDIANA

REPRESENTATIVES

Henry E. Sanders, McClatchy Bldg.
69th & Market St., Upper Darby, Penna.
Phone: Flanders 2-4420

W. S. Harmon Company, 1638 So. La Cienega Blvd.
Los Angeles 35, California • Phone: Bradshaw 2-3371

John A. Green Company, 6815 Oriole Drive
Dallas 9, Texas

IN CANADA

C. C. Meredith & Co., Ltd., Streetsville, Ontario

SOUTH AMERICA

Jose Luis Pontet
Buenos Aires, Argentina • Montevideo, Uruguay
Rio de Janeiro, Brazil • Sao Paulo, Brazil

OTHER EXPORT

Sylvan Ginsbury
8 West 40th Street, New York 18, N. Y.

Specialists in Precision Mass Production of Variable Resistors

TIC-TALKS FEATURE

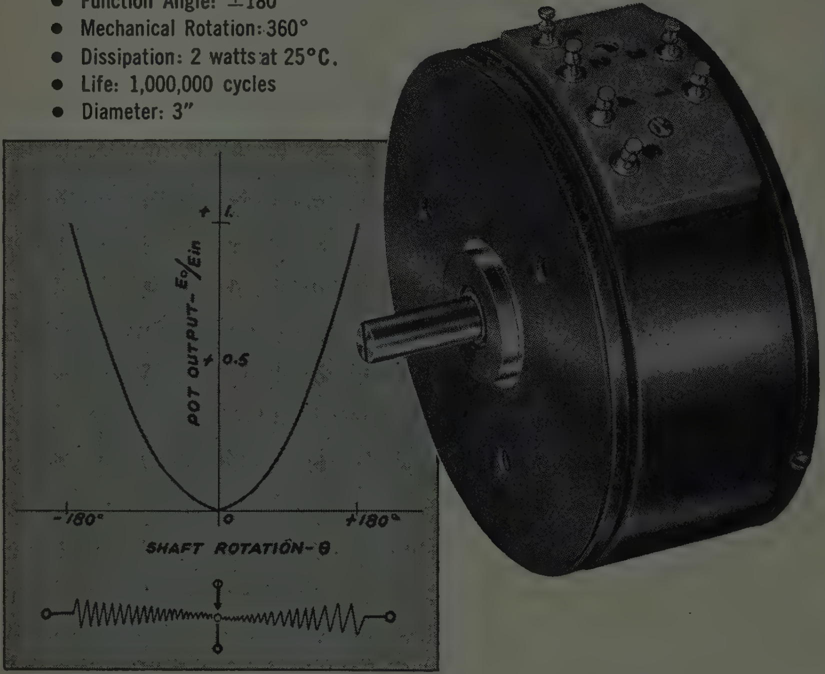
ANALOG COMPUTATION *with* TIC PRECISION POTENTIOMETERS

The type **RVP3-S121** solves the following mathematical equation:

$$\frac{Eo}{Ein} = \left(\frac{\theta}{180}\right)^2; \quad -180° \leqq \theta \leqq +180°$$

SPECIFICATIONS

- Total resistance: 2500±5%
- Conformity to function: ±0.25% Ein
- Function Angle: ±180°
- Mechanical Rotation: 360°
- Dissipation: 2 watts at 25°C.
- Life: 1,000,000 cycles
- Diameter: 3"



Your analog computations in control processes, computers, servomechanisms, and telemetering may likewise be solved by Technology Instrument Corporation precision potentiometers, with ease, economy and extreme accuracy. Precision non-linear potentiometers may be designed to meet your requirements from either implicit functions or empirical data. Submit your problem today for our analysis and recommendations.

A complete line of standard sizes is available, ranging from 7" to ½" in diameter. Greatly expanded facilities plus mass production techniques will meet your volume needs yet maintain precision tolerances in both linear and non-linear potentiometers. Write for catalog for complete information.

Engineering Representatives

Cleveland, Ohio — PRospect 1-6171
Chicago, Ill. — UPtown 8-1141
Rochester, N. Y. — Monroe 3143
Canaan, Conn. — Canaan 649
Dayton, Ohio — Michigan 8721
Baltimore, Md. — Plaza 7694

Arnprior, Ont., Can. — Arnprior 400
New York, N. Y. — MUrray Hill 8-5858
Cambridge, Mass. — ELiot 4-1751
Hollywood, Cal. — HOllywood 9-6305
Dallas, Texas — DIxon 9918
Binghamton, N.Y.—Binghamton 3-1511

TECHNOLOGY INSTRUMENT CORP.

535 Main Street, Acton, Massachusetts. Tel. ACton 3-7711

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 126A)

Attenuator Pads

Telewave Laboratories, Inc., 100 Metropolitan Ave., Brooklyn, N. Y., has recently placed a miniaturized type of microwave attenuator pad on the market. Known as Micropads, the new product is reported to be extremely compact and rugged with no fine wires or delicate elements. Ability to withstand overloads of more than 100 per cent is also claimed. Telewave's platinum film microwave resistors are employed.

Engineers of the company state that Micropads are finding increasingly widespread application wherever ultra-high precision microwave measurement is essential but space is limited.

Complete details on Micropads may be obtained by writing direct to Telewave Laboratories, Inc.

(Continued on page 132A)

A NEW UNIVERSAL KLYSTRON
POWER SUPPLY
— for
MICROWAVE OSCILLATORS

- Operates all low power commercial klystrons.
- Positive or negative grid operation.
- Widest modulation frequency range.
- Beam voltage: Regulated continuously variable over ranges of 300 to 1500 v. at 65 ma. or to 3600 v. at 25 ma.
- Repeller voltage: Direct reading continuously variable over the range of −20 to −750 volts.
- Modulation: Square wave, saw tooth, external or highly stable c-w operation.

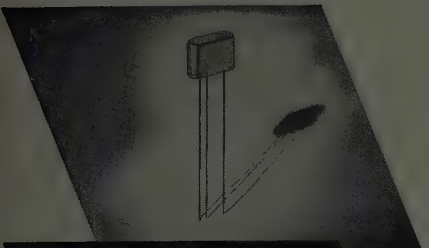
Specify the PRD Model 801-A

Polytechnic
RESEARCH & DEVELOPMENT CO., Inc.
55 JOHNSON ST., BROOKLYN 1, NEW YORK
West Coast: 741 N. Seward St., Hollywood 38, Calif.

14 Types of Germanium Transistors

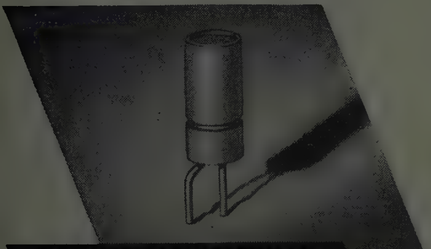
STABLE • UNIFORM • DURABLE

Hermetically Sealed



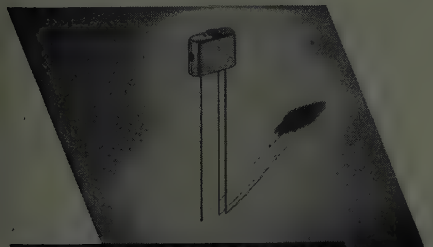
JUNCTION TRANSISTORS

Four types of these junction transistors are now available for audio or low speed switching applications where dependability, long life and minimum space requirements are important.



POINT CONTACT TRANSISTORS

Nine types of these point contact transistors are now available for applications as switches, amplifiers or oscillators. Special types made to meet your special requirements.



PN and NPN PHOTO TRANSISTORS

Type X-4 germanium PN junction photo transistor is designed for use as a light detector. Type X-25 is an NPN junction photoamplifier transistor with sufficient power output to operate a relay.

For data sheets and complete information on our transistors, diodes and transistor test set, write Dept. P10.

TRANSISTOR PRODUCTS, INC.

SNOW AND UNION STREETS, BOSTON 35, MASSACHUSETTS

AN OPERATING UNIT OF CLEVITE CORPORATION

---

to simplify data analysis...

A SPECIAL PURPOSE DEVICE... designed-developed by LIBRASCOPE for a specific computing need—the simplification of flow chart data reduction of graphic panel strip chart recorders by square root extraction and integration. The Square Root Planimeter was designed and developed by LIBRASCOPE as a special purpose device for industry. LIBRASCOPE offers this service for your application—perhaps the solution of problems confronting you in simplification of Data Analysis. For information concerning this or other special purpose devices, or assistance in solving your particular computing-controlling problems, consult LIBRASCOPE, manufacturer and designer of mechanical and electrical analog computers, digital computers, input-output devices, controls and components.

FLOW CHART TOTALIZING OF COST ACCOUNTING DATA AT THE STANDARD OIL COMPANY, EL SEGUNDO, CALIF.

THE SQUARE ROOT PLANIMETER

Flow chart totalizing of miniature panel strip chart recorders manufactured by Brown Instruments, Moore Products, The Swartwout Company, Taylor Instrument Company, and others. A true square root extraction and integration without approximation. Also available for linear integration. Accuracy comparable to stability of chart paper.

Computers and Controls

LIBRASCOPE INCORPORATED

1607 FLOWER STREET • GLENDALE, CALIFORNIA

A SUBSIDIARY OF GENERAL PRECISION EQUIPMENT CORPORATION

If you desire the challenge of advanced design fields and qualify in education and experience, write to Dick Hastings, Personnel Director.

ENGINEERS...TECHNICIANS!..here is your

New! B&W

Dip Meter

Model 600

NEW LOW PRICE

$39 75/net

B&W
Model 600 Dip Meter

VERSATILITY, COMPACTNESS, QUALITY

Few instruments will prove so handy in so many ways as this versatile B&W Model 600 Dip Meter! Ideal for lab, production, service or ham shack use, it provides a quick, accurate means for measuring resonant circuit frequencies, spurious emissions and many other tuned circuit characteristics. Shaped for easy use in today's compact electronic assemblies, highly sensitive and accurately calibrated, it incorporates many features previously found only in higher-priced instruments. You'll find dozens of uses for it as ...

A Grid Dip Oscillator for determining resonant frequencies of tank circuits, antennas, feed line systems, and parasitic circuits; aligning filters and traps; peaking coils, neutralizing and tuning transmitters before power is applied.

An Absorption Wave Meter for accurately identifying the frequency of radiated power from various transmitter stages; locating spurious emissions causing troublesome TV and radio interference, and many similar uses.

An Auxiliary Signal Generator providing a signal for tracing purposes and for preliminary alignment of receivers, converters, and I-F stages.

An R-F Signal Monitor for audible observation of hum, audio quality, and other audible characteristics of radiated power.

For Capacity, Inductance, and "Q" measurements in conjunction with other components of known value.

TECHNICAL FEATURES

- ✓ Covers 1.75 to 260 mc. in 5 bands.
- ✓ Adjustable sensitivity control.
- ✓ Size 3" x 3" x 7". Weight 2 lbs.
- ✓ Handy wedge-shape for easy access in hard-to-get-at places.
- ✓ Monitoring jack and B+ OFF switch.
- ✓ Rust-proofed chassis, aluminum case.
- ✓ Built-in power supply for 110 volts A.C.

Sold by leading distributors throughout U. S. A. and Canada
Data bulletin sent on request.

BARKER & WILLIAMSON, INC.
237 Fairfield Avenue Upper Darby, Penna.

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 130A)

Sub-Miniature High-Voltage Supply

Technical Operations Inc., 6 Schouler Court, Arlington, Mass., announces development of a sub-miniature, transistorized, high-voltage power supply, for use in high-voltage, low-current applications. Typical uses include nuclear radiation detectors, photomultiplier photometers and infra-red image converters. This new-type power supply is especially useful where small size, light weight, high dc energy conversion efficiencies and reliable operation over a long period are required. It measures $2\frac{3}{4}\times1\frac{3}{4}\times1\frac{7}{8}$ inches and weighs $7\frac{1}{2}$ ounces.

Battery operated (4 penlite cells can be used), its dc energy conversion efficiency ranges from 30 to 50 per cent depending upon the operating point and input voltage. The input can be connected to operate on voltages from 3 to 22.5 volts. Under most conditions the higher voltages give the higher efficiencies. There are no moving parts; no thermionic tubes. Hermetically sealed junction transistors are used in the conversion unit. Expected life is 50,000 hours of operation. Two models are available, with voltage regulated to ±15 volts: PS-1, at 700 volts and PS-2, at 900 volts. Both have a maximum current output of 50 microamperes.

Tantalum Capacitor

A tantalum capacitor, believed to be the smallest high capacity unit ever designed for low voltage, direct current applications, has been announced by the **General Electric Co., Capacitor Dept.**, Hudson Falls, N. Y.

The major feature of the unit is the advantage in size per volt μf over most other electrolytics. Other features include: long shelf and operating life, wide temperature range, and low leakage current. The unit is sealed against leakage or contamination and utilizes a non-acid electrolyte. Dimensions are 5/16 inch long and, $\frac{1}{8}$ inch diameter.

It is designed to operate over a temperature range of -20°C to $\times 50$°C and is suitable for storage at -65°C.

(Continued on page 134A)

SHURE

THE "Field-Proved" STANDARD IN COMMUNICATIONS . . . INTRODUCES A NEW

TELEPHONE HANDSET

...the first Handset specially engineered for two-way communications

- 2-Way Radio Communications
- Inter-Com Systems
- Airplane Announce Systems
- P. A. Systems

Specially Designed to Suit Your Specific Applications

Here is a truly modern functional handset specifically designed for 2-way communications! A product of the Shure Laboratories with many years of experience in safety mobile communications, the TH10 Handset brings you these features: . . . the field-proved *controlled reluctance* assembly as a receiver . . . high output *balanced response* carbon transmitter . . . oversize switch cavity providing flexibility in stacking of famous Shure long-life leaf blades . . . cored handle for maximum number of conductors . . . no solder connections . . . rugged shock resistant handle . . . design smart to the eye, natural in the hand. The answer to your complex circuitry!

SHURE

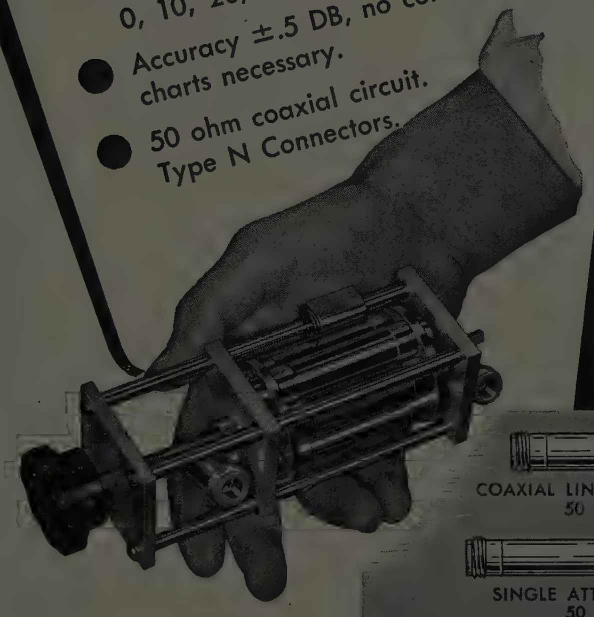
For more complete information write to SALES DIVISION

SHURE BROTHERS, Inc.
Manufacturers of Microphones & Acoustic Devices
225 W. HURON ST., CHICAGO 10, ILL.
Cable Address: SHUREMICRO

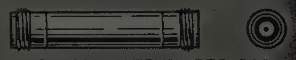
Precision

ATTENUATION to 3000 mc!

- VSWR less than 1.2 at all frequencies to **3000 mc.**
- **TURRET ATTENUATOR** featuring **"Pull - Turn - Push"** action with 0, 10, 20, 30, 40, 50 DB steps.
- Accuracy ±.5 DB, no correction charts necessary.
- 50 ohm coaxial circuit. Type N Connectors.



COAXIAL LINE TERMINATION
50 ohms



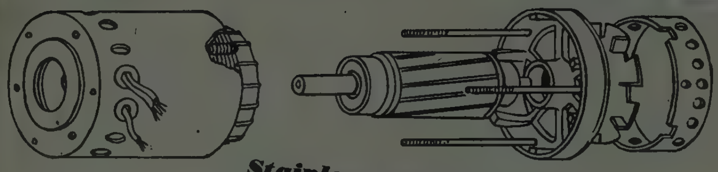
SINGLE ATTENUATOR PAD
50 ohms

VSWR ± 1.2 to 3000 mc.
One watt c.w. power dissipation

Inquiries are invited concerning single pads and turrets having other characteristics

STODDART AIRCRAFT RADIO CO., INC.
6644-C SANTA MONICA BLVD., HOLLYWOOD 38, CALIFORNIA
HOllywood 4-9294

EXTRA-RIGID CONSTRUCTION IN MINIATURE MOTORS



Stainless steel thru-bolts
Rigid die-cast aluminum housing
Riveted stator

These construction features, incorporated in *all* Air Marine sub-fractional horsepower motors, result in extra-rigid design that assures positive bearing alignment and uniform air gap. Even after repeated impact shock and vibration tests, motor performance remains unchanged. Motors are protected against humidity and fungus growth — can be mounted in any position — are equipped with ball bearings using suitable lubricants for high and low ambient temperatures—meet all AN specifications.

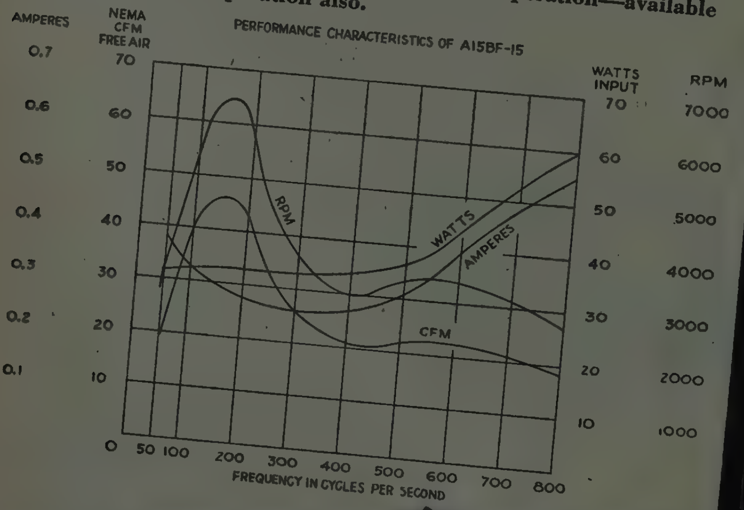
A NEW ENGINEERING DEVELOPMENT

The 50-800 cycle Type A15BF-15 Motor

Latest result of Air Marine design skill is the Type A15BF-15 motor, the first ever manufactured for operation over the entire frequency range from 50 to 800 cycles.

Motor is designed for operation on 115 volt variable frequency supply—has single winding, four leads, reversible.

Totally enclosed—available with or without fan or blower. Type A15BF-15 is designed for single phase operation—available for 2 and 3 phase operation also.



AIR MARINE MOTORS INC.
3939 MERRICK ROAD, SEAFORD, L. I., N. Y.
SUnset 5-7309

Send for Sub-Fractional Horsepower Motor and Application Folder and Engineering Assistance Form Number 1200.

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

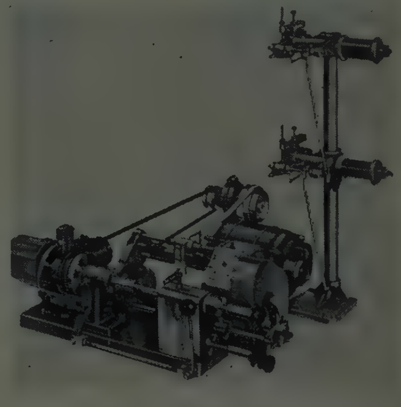
(Continued from page 132A)

The new unit is available in ratings from 2 to 16 volts, 4 to 0.7 μf respectively. Another, larger capacitor, ½ inch, with similar characteristics and the same voltage range, but with 8 to 1.5 μf, has also been announced as available.

G-E engineers said that, while temperatures below −20°C will result in further loss of capacitance, the new units will continue to be operable and will often give satisfactory values at much lower temperatures. At 10 volts or above and at −55°C, the capacitors will maintain at least 65 per cent of its 25°C value, according to advance tests. It is also possible to obtain satisfactory performance above 50°C with some life restrictions, the engineers added.

Dual Head Winder

British Industries Corp., 164 Duane St., New York 13, N. Y., has added a new AVO coil winding machine to the more than 30 models already available in the United States. The AVO "Douglas" and "Macadie" dual-head coil winder is designed for the winding of coils where the set-up time is long compared to the actual winding time. While one coil is being wound, the other can be finished and replaced by a new bobbin ready to start another coil.



This durable, high-speed production machine features a predetermined revolution counter, magnetic clutch for positive control, lead screw traverse, easily changed gears for quick set-up, micrometer traverse adjustment, foot control, and tension devices of an advanced design. There are only two controls on the machine, one of which engages the clutch while the other engages either the top or bottom spindle.

All rotating parts are fitted with ball races, and are finished with accuracy. One of the operating features of the coil winder is a rapid change of direction of the traverse at the end of each layer. This prevents any risk of the wire piling up against the cheeks of the coil.

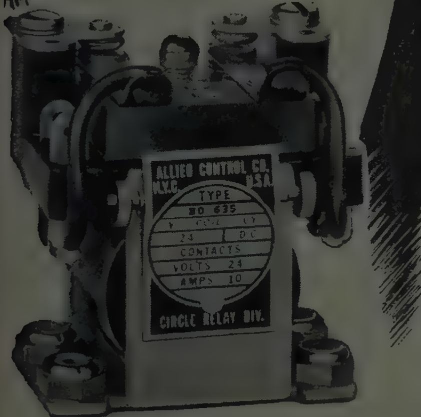
(Continued on page 136A)

24 HOUR
DELIVERY
FROM STOCK!

RELAYS

Our stock of more than a million relays—in over a thousand different types—is the world's largest. Don't delay your production for want of large or small quantities of relays of any type.

Telephone, wire or write for quotations.



NEW AND MORE COMPREHENSIVE

1953 RELAY SALES CATALOG

NOW READY

Be sure to send for your copy

Relay Sales
1953 CATALOG

Relay Sales

Telephone
SEeley 8-4146

833 W. CHICAGO AVE.
DEPT. 7, CHICAGO 22, ILL.

---

world's largest Ion Trap maker offers lowest priced Ion Trap on the market

NEW SIMPLIFIED CONSTRUCTION

MODEL T-312. The new simplified steel construction lowers manufacturing costs by fully utilizing, for the first time, the Alnico permanent magnet's maximum efficiency. This makes Model T-312 the lowest priced ion trap on the market. Installs in only 2-3 seconds—just slip on.

FEATURES OF BOTH MODELS

STAYS PUT—No wobble; no shift during shipment; no realignment necessary when your TV set is installed in the home.

EASILY ADJUSTED—Slides more uniformly over tube's neck due to metal-to-glass contact.

STABILIZED AND TESTED on special equipment designed and used only by Heppner, each individual Heppner Ion Trap is guaranteed to meet your working requirements.

UNUSUALLY FAST DELIVERY.

LIGHTWEIGHT—Snap-On Model weighs only ½ ounce; Slip-On Model only $^3/_5$ ounce. Will not harm tube's neck.

ALNICO P.M. USED—Retains magnetism indefinitely.

SNAP-ON ION TRAP

installs instantly—just snap on—stays put

MODEL E-437. Saves you expensive production manhours with EXCLUSIVE instant snap-on feature. Reduces your parts costs because priced below competition. Clamp-type construction of Hardened Spring Steel.

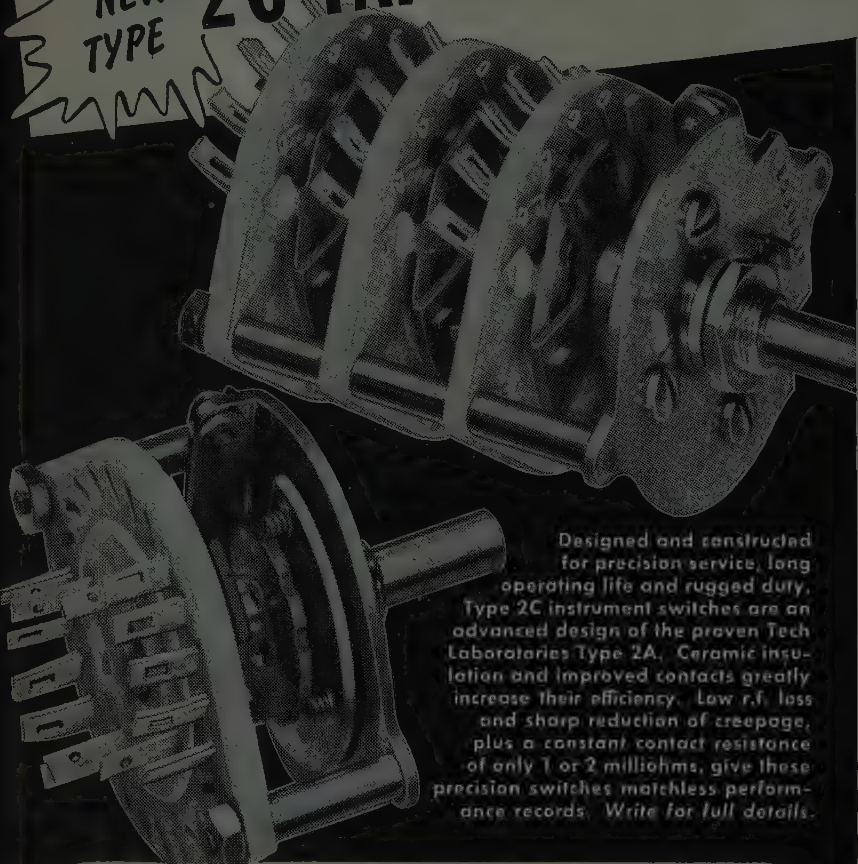
Heppner has built over 15,000,000 ion traps to date

Write today for further information on better ion traps at lower prices.

HEPPNER
MANUFACTURING COMPANY
Round Lake, Illinois (50 Miles Northwest of Chicago)
Phone: 6-2161
SPECIALISTS IN ELECTRO-MAGNETIC DEVICES

Representatives:
John J. Kopple
60 E. 42nd St., New York 17, N.Y.
James C. Muggleworth
506 Richey Ave., W., Collingswood, N. J.
Ralph Haffey
2417 Kenwood Ave., Ft. Wayne 3, Indiana
Irv. M. Cochrane Co.
408 So. Alvarado St., Los Angeles, Calif.

Ceramic Insulated for
LOW LOSS...
MINIMUM CREEPAGE
NEW TYPE 2C TAP SWITCHES



Designed and constructed for precision service, long operating life and rugged duty. Type 2C instrument switches are an advanced design of the proven Tech Laboratories Type 2A. Ceramic insulation and improved contacts greatly increase their efficiency. Low r.f. loss and sharp reduction of creepage, plus a constant contact resistance of only 1 or 2 milliohms, give these precision switches matchless performance records. Write for full details.

SPECIFICATIONS

Contact resistance: 1-2 milliohms

Contact material: Silver alloy

Contact design: Laminated wiper arm, self-cleaning, shorting or non-shorting

No. of contacts: 2 to 24 single pole, shorting or non-shorting
2 to 11 double pole, shorting or non-shorting
2 to 5 triple pole, shorting or non-shorting

Spacing: 15° or 20°, shorting or non-shorting

No. of poles per deck: 1 to 4

No. of decks: According to requirements

Life: 200,000 cycles, min.

Current carrying cap.: 3 amp.

Max. operating voltage: 120 V., a.c.

Mounting: Single hole, ⅜"-32 bushing, standard length for up to ¼" panel, special lengths to order

Size: 1¾" dia.

Detent: Ball and spring

Weight: Approx. 1 oz. per deck

TECH LABORATORIES, INC.
Manufacturers of Precision Electrical Resistance Instruments
PALISADES PARK, NEW JERSEY

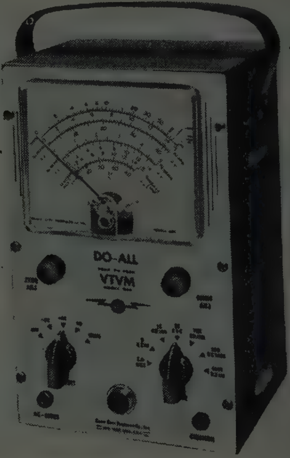
News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 134A)

Peak-to-Peak VTVM

Radio City Products Co., Inc., 152 W. 25 St., New York 1, N. Y., has announced an advanced design peak-to-peak VTVM, Model #655.



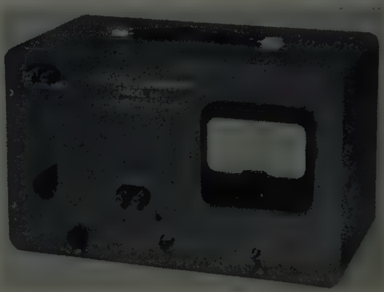
This latest addition to the RCP "Do-All" line gives a true reading measurement of complex and sinusoidal voltages with necessary peak-to-peak or RMS value read directly, for the analysis of waveforms in video, synchronous and deflection circuits.

Of high-impedance design, the RCP Model #655 "Do-All" features peak-to-peak ac measurements of 0.1 volt to 1500 volts on 7 ranges, dc measurements, of from 0.02 volts to 1500 volts on 7 ranges, and resistance measurements of from 0.2 ohms to 1,000 megohms on 7 ranges.

The measuring circuit uses a balanced-bridge type dc amplifier and sensitive meter together with a high-impedance voltage divider. A 1-megohm isolation resistor provides an input impedance of 11 megohms on dc. An additional peak-to-peak rectifier together with compensated attenuator is used for the ac measurements.

Impedance Comparator

Industrial Test Equipment Co., 55 E. 11 St., New York, N. Y., has developed a new Impedance Comparator, Model 60.



This instrument has been designed for production line testing of resistors, capacitors, and inductors. The percentage deviation of the component under test

(Continued on page 138A)

by
every
test
ATR
is BEST!
ATR VIBRATOR
524
ATR REPLACEMENT

ATR AUTO RADIO

VIBRATORS

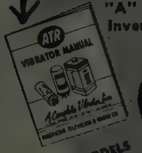
Have Ceramic Stack Spacers

A COMPLETE LINE OF VIBRATORS

Designed for Use in Standard Vibrator-Operated Auto Radio Receivers. Built with Precision Construction, featuring Ceramic Stack Spacers for Longer Lasting Life. Backed by more than 22 years of experience in Vibrator Design, Development, and Manufacturing.

Free

"A" Battery Eliminators, DC-AC Inverters, Auto Radio Vibrators



ATR

✓ NEW MODELS ✓ NEW DESIGNS ✓ NEW LITERATURE

See your jobber or write factory

AMERICAN TELEVISION & RADIO Co.
Quality Products Since 1931
SAINT PAUL 1, MINNESOTA—U. S. A.

KEARFOTT GYROS

continuous
vertical
reference

KEARFOTT vertical gyros providing continuous vertical reference within two minutes of arc under bench conditions typify the engineering know-how and production skills available to you in the field of precision gyros for airborn control applications.

Designed for particular applications with stringent performance requirements, a wide variety of free, vertical and rate gyros now in production are being used extensively in aircraft and missile control systems demanding the most precise gyro reference obtainable.

Kearfott gyros incorporate many unique features permitting operation under extreme operational or environmental conditions. A true hermetic seal in dry inert gas provides positive environmental protection. Synchro pick-offs and rigid structural elements assure performance during adverse conditions of vibration or shock.

If you require gyros with these highly desirable characteristics, we would be happy to review your application to the end that these problems may be resolved. Please write today for Bulletin #53 describing our products and facilities. Technical data on all products is available and will be sent on request.

KEARFOTT COMPONENTS INCLUDE:

Gyros, Servo Motors, Synchros, Servo and Magnetic Amplifiers, Tachometer Generators, Hermetic Rotary Seals, Aircraft Navigational Systems, and other high accuracy mechanical, electrical and electronic components.

Kearfott
SINCE 1917
CREATIVE ENGINEERING
PRODUCTION ACHIEVEMENT

KEARFOTT COMPANY, INC., 1150 McBride Ave., Little Falls, N. J.
Midwest Office: 188 W. Randolph St., Chicago 1, Illinois
West Coast Office: 253 N. Vinedo Ave., Pasadena, Calif.
A General Precision Equipment Corporation Subsidiary

Saratoga Industries

STAR PERFORMANCE AS MANUFACTURERS OF TRANSFORMERS, REACTORS, FILTERS, TOROIDAL COILS FOR THE ELECTRONICS INDUSTRY

Now in its ninth year of operation, Saratoga Industries, Inc. has built a solid reputation for the manufacture of precision windings. Approved for in-plant testing under MIL-T-27, Saratoga Industries, Inc. is also prepared to handle all types of commercial production. Saratoga engineers invite your inquiry to help solve your problems relating to reactors, transformers, filters and windings of all types.

SARATOGA INDUSTRIES, INC., SARATOGA SPRINGS, N. Y.

SQUARE PULSE GENERATOR

MODEL 300

for the

MILLIMICROSECOND to MICROSECOND RANGE

New Basic Test Instruments for NUCLEAR, RADAR, TV, UHF, and other fields in which FAST PULSE CIRCUITS are employed. Three or more pulse outputs are available in Model 300.

SPECIFICATIONS

PULSE SHAPE: square pulse
RISE TIME: .001 μsec. from 10% to 90% amplitude
PULSE WIDTH: .001 μsec to several μsec., selectable.
PULSE AMPLITUDE: From 100 volts to .006 volts in one db steps
OUTPUT IMP: Matched to any impedance for standard coax lines
POWER INPUT: 105-125 V, 60 cy.
SIZE: 17-1/2" x 19" x 10-3/16"

EPIC ELECTRICAL & PHYSICAL INSTRUMENT·CORP.
42-19 27th Street, L.I.C. 1, N. Y.
Dept. RP-10

A NEW FAST 10 mc SCALER

0.1 Microsecond Resolution

SPECIFICATIONS **Model 410**

INPUT CIRCUIT:
- **POLARITY:** Positive pulses only.
- **AMPLITUDE:** Minimum amplitude of 5 volts required at low counting rates, increasing to 10 volts minimum at the maximum counting rate.
  - **REQUIRED RATE OF RISE:** Minimum of 10 volts per μsec.
- **INPUT IMPEDANCE:** Greater than 5000 ohms.

RESOLVING TIME: 0.1 μsec.
MAXIMUM ACCEPTABLE UNIFORM RATE: 10mc or 10^7 counts/second, no lower limit on counting rate.
SCALING FACTOR: Neon light interpolation for reading residual counts.
OUTPUT:
- **POLARITY:** Positive or Negative pulse selected by front panel switch.

PULSE CHARACTERISTICS: Triangular pulse of approximately 1 μsec. rise time, 4 μsec. width and 50-60 volt amplitude.
POWER REQUIREMENTS: 105-125 volts, 50-60 cycles, approximately 175 watts.
SIZE: 10-1/2" x 19" x 13" deep

Complete literature on request

EPIC ELECTRICAL & PHYSICAL INSTRUMENT CORP.
42-19 27th Street, L.I.C. 1, N. Y
Dept. RS-10

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 136A)

from a standard component is read directly on the meter. Four ranges are provided: 1, 5, 10, and 20 per cent full scale. One linear scale serves for all ranges. No zero adjustment is required and the range calibration is readily performed by means of a built-in standard. Special design has eliminated the necessity for operating push-buttons or relays. Component impedances from 1 ohm to 5 megohms at 60 cps may be compared. Built-in regulator permits line voltage variations from 105 to 125 volts, 60 cps. Dimensions are height 9 inches, width 15 inches, depth 8 inches.

Inverters

New models of ATR Inverters for operation from 6-volt or 12-volt storage batteries have recently been announced by the **American Television & Radio Co.,** 300 E. Fourth St., St. Paul, Minn.

ATR Inverters operate from 6- to 12-volt storage batteries and provide 110-volt ac 60-cps output in various wattage capacities for the operation of dictating machines, tape recorders, wire recorders, radio sets, test equipment, and other related small electrical or electronic apparatus.

Inverter models are also available for operation from other dc input voltages ranging from 6 volts dc to 220 volts dc.

Complete literature is available directly from the factory.

Dual-Beam Cathode-Ray Voltmeter Bulletin

A bulletin on the new DuMont Type 322-A Cathode-ray Oscillograph is now available from **Technical Sales Department, Allen B. DuMont Laboratories, Inc.,** 760 Bloomfield Ave., Clifton, N. J.

The new bulletin contains complete technical specifications, description, and photo-recordings made with the new instrument. The DuMont Type 322-A is an improved redesigned counterpart of the DuMont Type 322 Dual-beam Cathode-ray Oscillograph with the added feature of built-in independent voltage calibration for both beams, and which also incorporates the new tight-tolerance Type 5AFP-cathode-ray tube.

(Continued on page 142A)

STABILITY and ACCURACY PERMEABILITY TUNED OSCILLATORS

COLLINS RADIO COMPANY
TYPE
SERIAL
CEDAR RAPIDS, IOWA, U.S.A.
WARNING
SEALED UNIT
DO NOT REMOVE
THIS COVER
V002
6BA6
V001
6BA6

Actual size

**Collins Type 70E-15 precision oscillator. 2.0 — 3.0 mc
All Collins oscillators are designed for linear dial calibration.**

NARDA
Model 802

2400 to 10,200 Mc
FREQUENCY METER

SPECIFICATIONS
- FREQUENCY RANGE: 2400 - 10,200 Megacycles
- ACCURACY: ±0.2%
- SENSITIVITY: 10 milliwatts to 5 watts
- RESONANCE INDICATOR: 50 microamp movement
- TEMPERATURE COEFFICIENT: 15 parts per million per °C.

The NARDA Line
INCLUDES:
Hi-Power Impedance meters • 12.4 to 18.0 Kmc Frequency meter • Microwave mixers, detectors, and test equipment • Waveguide Bends and Components • Pulsed R-F Signal generators • Microwave Engineering.

COVER: Unit is equipped with detachable cover—not shown.

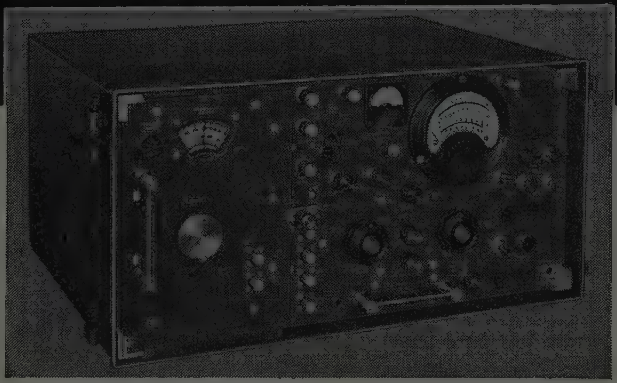
For additional information regarding this unit, send for bulletin #1053.

Custom built Microwave and Electronic Test Equipment

NARDA NASSAU RESEARCH & DEVELOPMENT ASSOCIATES INCORPORATED
66 MAIN STREET MINEOLA, NEW YORK
Subsidiary of PEERLESS INSTRUMENT CO., INC. GARDEN CITY 3-3570

NOISE and FIELD INTENSITY METER Model NF-105
(Commercial Equivalent of AN/URM-7)

CONFORMS TO
MIL-I-6181B
MIL-I-16910



ENGINEERING DATA
- Frequency range 20 MC to 1000 MC by means of three quick-change tuning heads. At least one RF amplifier with tuned input is employed for each tuning range.
- Easy frequency scanning by means of single tuning knob.
- Built-in impulse noise calibrator flat to 1000 MC (Output externally available).
- 4½" logarithmic indicating meter, reads carrier or true peak.
- Aural slideback operation.
- Input VSWR better than 1.2 to 1.
- Built-in regulated "A" and "B" supply.
- Complete line of accessories available.

Write today for additional information and our complete catalog

edp EMPIRE DEVICES PRODUCTS CORPORATION
38-15 BELL BOULEVARD • BAYSIDE 61 NEW YORK

MANUFACTURERS OF
FIELD INTENSITY METERS • DISTORTION ANALYZERS • IMPULSE GENERATORS • COAXIAL ATTENUATORS • CRYSTAL MIXERS

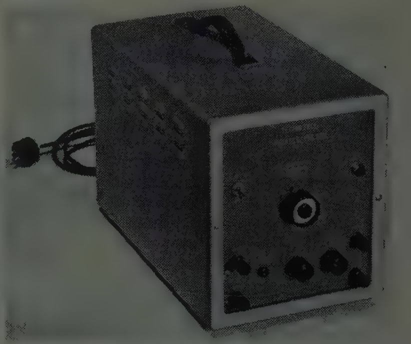
News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 142A)

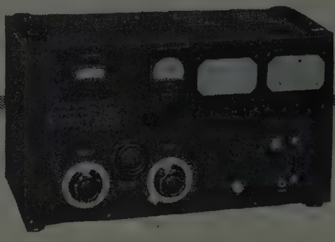
Variable Pulser

A new Variable Pulser featuring a range of pulse repetition rates from 20 cps to over 2.0 mc with high stability of pulse duration, is now available from **Technitrol Engineering Co.**, 2751 N. Fourth St., Philadelphia 33, Pa.



It is designed to convert the output of any standard oscillator with 3 volts RMS or greater, into a series of pulses, one for each oscillating cycle. These pulses exhibit rise and fall times of 0.05 μs and can be varied in width from 0.2 to 5.0 μs and amplitude from 0 to over 40 volts. In addition to the output pulse a trigger pulse preceding it in time is provided. Literature is available—send for Bulletin 186-2.

(Continued on page 172A)



Measurements Corporation
MODEL 84-TV
UHF TELEVISION
Standard Signal Generator
300–1000 Mc.

FREQUENCY RANGE: 300-1000 megacycles.
OUTPUT: .1 Microvolt to 1 Volt, across 50 Ohms.
OUTPUT IMPEDANCE: 50 Ohms coaxial.
MODULATION: Internal 400 cycle, continuously variable from 0 to 30%. Provision for external modulation of 50 to 20,000 cycles.
LEAKAGE: Negligible.
SIZE: Overall Dimensions: 11¾ inches high, 19 inches wide, 11 inches deep.
WEIGHT: Approximately 40 pounds.
POWER: 115 volts, 60 cycles, 120 watts.

MEASUREMENTS CORPORATION
BOONTON NEW JERSEY

OPTICAL SYSTEMS

INDUSTRIAL PERISCOPES

KOLLMORGEN

DESIGN

DEVELOPMENT

MANUFACTURE

For nearly half a century Kollmorgen has designed, developed and manufactured precision optics and optical systems for industry and the military.

We have the engineering "know-how", the design personnel and the manufacturing capacity to help you solve your optical problem.

KOLLMORGEN Optical CORPORATION

Plant: 347 King Street • Northampton, Mass.
New York Office
30 Church Street
New York 7, N.Y.

2 Computers? No-just One IDA!

Integro-Differential Analyzer

Leading design and research engineers have found that one IDA computer does the work of 2 ordinary computers – because of such ahead-of-the-field features as those outlined below:

Send for NEW Catalog Now!
IDA

Interchangeable Set-up Boards: permit problem change-over in minutes; thus IDA is always at work, there's no lost set-up time!

20 Uncommitted Amplifiers: perform *any* computing function; and any required scale factor may be used for any number of inputs to any amplifier.

Hold Control: usually found only in most expensive computers, permits introduction of gross non-linearities.

8 Initial Conditions: once fixed, are automatically restored after each solution.

New Extra-Convenient Compactness: with the IDA you can actually sit at your desk while you compute!

Send for complete descriptive catalog . . .

COMPUTER CORPORATION OF AMERICA
149 CHURCH STREET NEW YORK 7, NEW YORK

Design, development and manufacture of computers, laboratory instruments, regulated power supplies and specialized equipment for computers, instrumentation and control. Computing laboratory for the solution of problems in dynamics.

Burlington
D.C. MILLIAMPERES
RUGGEDIZED
HERMETICALLY SEALED
INSTRUMENTS

LABORATORY APPROVED
Under MILITARY SPECIFICATION MIL-M-10304

- Will withstand Hi-Impact Shock Tests, extensive vibration and tumbling requirements, extreme thermal shock, humidity and temperature tests.
- Glass to metal type seal with molded vulcanized rubber terminal connections capable of carrying 30 amps for self-contained units.
- Magnetically shielded.
- Black satin onodized aluminum bezel.
- D'Arsonval permanent magnet type movement—for all D.C. Ranges.
- Available in 2½" and 3½" round case types.
- Guaranteed one year against defective workmanship and materials.

BURLINGTON INSTRUMENTS ALSO AVAILABLE IN HERMETICALLY SEALED OR BAKELITE CASES IN 1½" THROUGH 4½" SIZES

BURLINGTON INSTRUMENT COMPANY
DEPT. I-103, BURLINGTON, IOWA

IF IT'S NEW . . . IF IT'S NEWS . . . IT'S FROM ELCO

Among the news-making products now being introduced by Elco Corporation, are sub-miniature sockets of tested laboratory and practical performance. Illustrated here is Elco's 5-pin sub-miniature, which offers the quality-minded user the electrical uniformity and mechanical stability resulting only from the highest manufacturing standards. And, as with all Elco products, the use of Elco sub-miniature sockets affords many advantages previously unavailable.

New contact design automatically centers the tube pins in position, eliminating strain on the tube body. Positive contact resistance assures excellent circuit performance. Insulator construction affords adaption for printed circuitry, a decided extra advantage; and provides a longer creepage path between contacts. Mounting retainer securely locks body of socket to chassis and is self-adjusting to any variation in chassis thickness from .015" to 062". The retainer is of heat-treated steel cadmium plated; the insulator of low-loss mica filled phenolic. Elco also offers many other new sub-miniature, miniature and printed circuit types. Complete details are yours upon request; as is full information about Elco's quality line of sockets, shields, and sensational new Varicon connectors.

For Catalog Sheets, Call GArfield 6-6620 or Write ELCO Corp., 190 W. Glenwood, Phila. 40, Pa.

TOP HAT FOR PLUG-IN UNITS

A widely used, dependable, improved clamp for electron tubes, relays and capacitors.

WRITE FOR 1953 CATALOG

EASY TO APPLY
INSTANTLY RELEASED
POSITIVE LOCKING ACTION

TIMES FACSIMILE CORPORATION
540 West 58 St., New York 19, N. Y.
1523 L St., N. W. Washington 5, D. C.

AN/APR-4 LABORATORY RECEIVERS

Complete with all five Tuning Units, covering the range 38 to 4,000 Mc.; wideband discone and other antennas, wavetraps, mobile accessories, 100 page technical manual, etc. Versatile, accurate, compact—the aristocrat of lab receivers in this range. Write for data sheet and quotations.

We have a large variety of other hard-to-get equipment, including microwave, aircraft, communications, radar; and laboratory electronics of all kinds. Quality standards maintained. Get our quotations!

We will buy any Electronic Material at top prices. SCHOOLS—unload your dusty surplus for cash or credit.

ENGINEERING ASSOCIATES

434 PATTERSON ROAD
DAYTON 9, OHIO

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 170A)

Wideband Directional Couplers

Four new Wideband Directional Couplers designed for power, impedance, or match measurements between 30 and 1500 mc, were announced this week by **Sierra Electronic Corp.**, 1050 Brittan Ave., San Carlos, Calif.

POWER FLOW
DIRECTIONAL COUPLER
MODEL 137
SERIAL 220
SIERRA ELECTRONIC CORP
SAN CARLOS, CALIF.
E₁
E₂

The power and frequency range of the new instruments permits use on a wide variety of laboratory measuring problems, including coefficient of reflection, or SWR power in the load, or dynamic match.

Because the couplers are small in size, inexpensive and ruggedly constructed,

(Continued on page 174A)

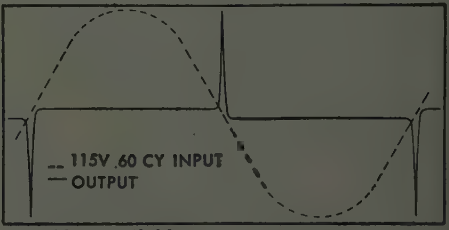
ENGINEERING SPECIALISTS

- CONTROL TRANSFORMERS
- MANUFACTURING

Engineering, designing, and currently manufacturing 400 different types of specialized industrial control transformers.

PEAKING TRANSFORMER HERMETICALLY SEALED

PERFORMANCE CURVE



Also available
220 V input, to 200 V peak
220 V input, to 100 V peak
Exclusive design, low exciting current 100 M. A. 1½ WATTS or as low as 10 M. A. 1 WATT.

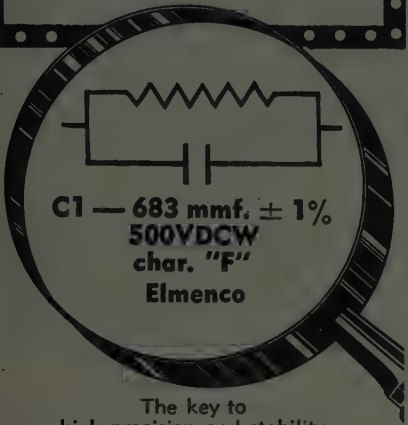
INQUIRIES INVITED

CHICAGO MAGNETIC CONTROL
1616 N. DAMEN AVE.
CHICAGO 47, ILLINOIS

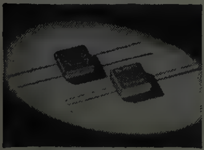
PRECISION

IS THE WATCHWORD TODAY IN ELECTRONICS

. . . as technological advancements call for circuits of increasing accuracy and dependability!

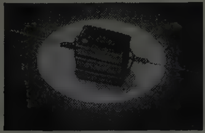


The key to high precision and stability lies in proper selection of mica capacitors, made possible through our ability to provide ANY CAPACITY at ANY TOLERANCE with the highest characteristics within the ranges specified for molded mica capacitors.



SINGLE UP TO 15000 MMF

DUAL UP TO 30000 MMF



TRIPLE UP TO 45000 MMF

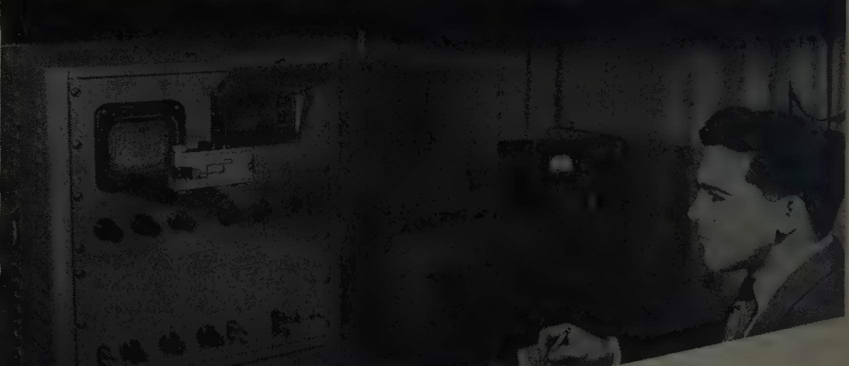
Any Capacity
Any Tolerance (to ± 0.5%)
JAN Characteristic "F" or Better for Most Capacity Values.

All capacitors are ELMENCO and are manufactured in accordance with JAN-C-5 specifications. Known the world over for their reliability under all operating conditions, ELMENCO CAPACITORS are chosen by manufacturers requiring the highest quality components for their products.

Write for our free descriptive catalog and for information regarding your special product requirements.

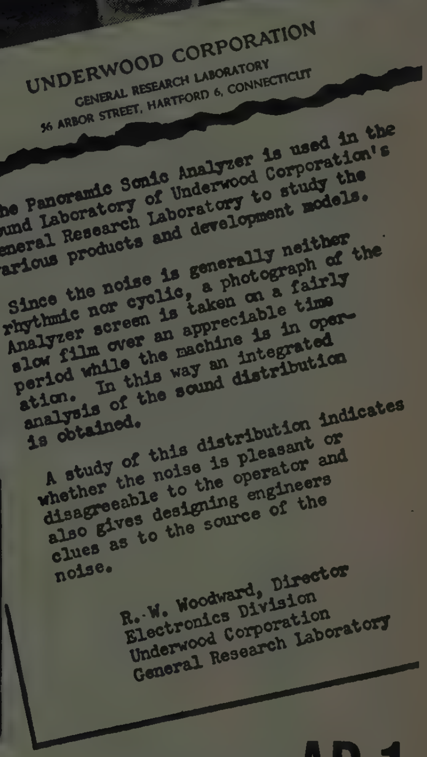
ARCO
ELECTRONICS INC.
103 LAFAYETTE ST., N. Y. 13, N. Y.

WHAT'S MAKING THAT NOISE?



PANORAMIC
RADIO PRODUCTS, INC.

finds out for
UNDERWOOD
CORPORATION



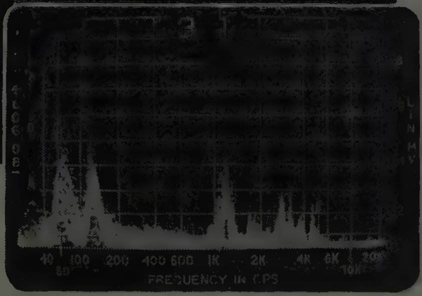
UNDERWOOD CORPORATION
GENERAL RESEARCH LABORATORY
56 ARBOR STREET, HARTFORD 6, CONNECTICUT

The Panoramic Sonic Analyzer is used in the Sound Laboratory of Underwood Corporation's General Research Laboratory to study the various products and development models.

Since the noise is generally neither rhythmic nor cyclic, a photograph of the Analyzer screen is taken on a fairly slow film over an appreciable time period while the machine is in operation. In this way an integrated analysis of the sound distribution is obtained.

A study of this distribution indicates whether the noise is pleasant or disagreeable to the operator and also gives designing engineers clues as to the source of the noise.

R. W. Woodward, Director
Electronics Division
Underwood Corporation
General Research Laboratory



Panoramic Sonic Analyzer MODEL **AP-1**
provides Sound and Vibration Analysis

for Product Development
Quality Control
Improvement

the pioneer
is the leader

PANORAMIC
RADIO PRODUCTS, INC.

The ever increasing importance and volume of work in noise and vibration analysis necessitates simple high speed analyzers to assure maximum efficiency and economy both in the laboratory and on the production lines. The Panoramic Sonic Analyzer truly meets these requirements. In a matter of seconds, the AP-1 automatically visualizes the frequency distribution and amplitude of complex waveform components between 40 and 20,000 cps. The AP-1 is a dual duty instrument. It is designed for investigations of research level yet it is so simple to operate that it is widely used by non-technical personnel for production line testing.

Let us help solve your noise and vibration problems

Write for complete details today.

12 South Second Avenue,
Mt. Vernon, New York

Try Remler for
Service-Tested
"Hard-to-Get"
Components

Custom Components

Metal-plastic components designed and manufactured to order. Write for quotations specifying electrical and mechanical characteristics. Describe application. No obligation.

FOR EFFICIENT MAINTENANCE

SPECIFY REMLER **TILT-UP**

EQUIPMENT SLIDES

Remler slide rails for rack or cabinet mounting permit complete withdrawal or inspection of top and bottom of apparatus chassis. Positive . . . self-locking. Full roller type . . . handles equipment up to 75 lbs. Stainless steel for military applications. Nickel plated brass rollers; roller studs in stainless or copper flashed cold rolled steel. . . . **$15.95 per pair.**

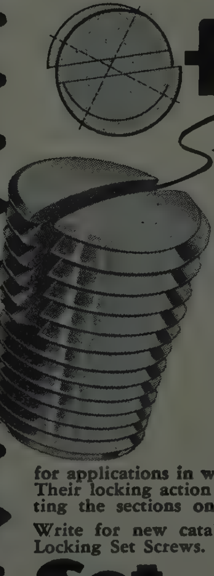
Remler Company Ltd. 2101 Bryant St. San Francisco 10, Calif.

Remler

Write for quantity prices.

Since 1918 PIONEERS IN ELECTRONICS AND PLASTICS

ANNOUNCING
that we now manufacture and sell



Offset
Self-Locking
SET SCREWS
—formerly marketed by Shakeproof Division of Illinois Tool Works

Now, more than ever, you can make Set Screw & Mfg. Co. your No. 1 source of supply for *self-locking set screws.* The recent addition of Offset Type Self-Locking Set Screws to our own widely successful ZIP-GRIP* and NU-CUP Self-Locking designs gives you a complete Self-Locking Set Screw range for solving vibration problems.

Setko Offset Self-Locking Set Screws are particularly suited for applications in which slotted screws are required. Their locking action results from springing or offsetting the sections on both sides, parallel with slot.

Write for new catalog sheet on Setko Offset Self-Locking Set Screws.

*Pat. Pending

371

Set Screw & Mfg. Co.

FOR FREE CATALOG

Simply write your name and address on margin of this page, tear out and mail today.

422 Main St., Bartlett, Ill. (Chicago suburb)

We Specialize in Solving Puzzling Set Screw Problems

These manufacturers have invited PROCEEDINGS
information. Please mention your I.R.E. affiliation.
readers to write for literature and further technical

(Continued from page 172A)

they are also practical as components in transmitters including communications, navigation, radar, television, microwave, emergency and other systems where power and match must be monitored continuously. The couplers may be used with either coaxial lines or with lumped linear passive networks.

The four models offered include Model 137, for 51.5 coaxial line, with coupling factor of 70 to 35 db and full-range directivity better than 46 db. Model 138, of similar design, is also for 51.5 ohm line, but provides a coupling factor of 59 to 24 db. Models 137A and 138A are identical with the preceding instruments, except are designed for 50 ohm cable. Bulletin 104, now available, describes the instruments and their applications.

RF Bridge

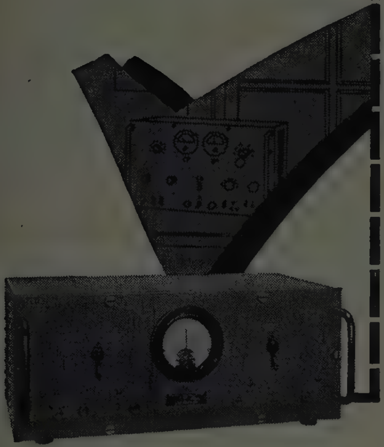
Boonton Radio Corp., Boonton, N. J., announces a new Type 250-A RX Meter, a completely self-contained RF bridge which permits the direct measurement of equivalent parallel resistance and capacitance of two terminal networks over an unusually wide frequency range. The new instrument has a frequency coverage of 500 kc to 250 mc in eight ranges; a resistance range of 15 to 100,000 ohms, and a capacitance range of $+20$ $\mu\mu$f to -100 $\mu\mu$f. Resistances from 0 to 15 ohms may be determined by indirect means; the capacitance range can be increased to 0 to 120 $\mu\mu$f by the use of auxiliary resonating coils.

The 250-A RX Meter is particularly useful for measuring the performance of resistors and transistors at elevated frequencies and also provides an extremely convenient tool for the determination of characteristic impedance, attenuation, and velocity of propagation of transmission lines.

The new 250-A RX Meter consists of ganged continuously tuned bridge and local oscillators, a modified Schering Bridge, an unbalanced or IF amplifier, and a null indicator with automatic gain control. The resistance scale covers 28 inches of scale length and requires no corrections in readings over the entire frequency range; the capacitance scale consists of a main dial calibrated in units of 10 $\mu\mu$f and a vernier dial with calibration points at intervals of 0.1 $\mu\mu$f.

(Continued on page 176A)

H-16 CHECKS the CHECKER



ARC Type H-16 STANDARD COURSE-CHECKER

For Omni Signal Generators

■ This newly developed instrument is a means for checking precisely the phase-accuracy of the modulation on VOR (Omnirange) Signal Generators. Now that the use of omnirange receivers and signal generators is so widespread, it is necessary to have a means of measuring the phase differences between the 30 cps envelope of the 9960 ± 480 cps reference modulation, and of the 30 cps variable modulation when that difference is required to be 0, 15, 180 or 195 degrees.

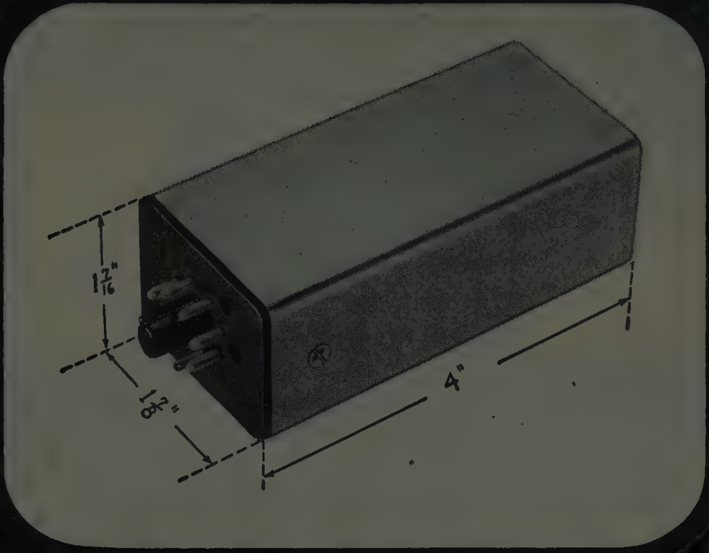
■ An important feature of the H-16 is a built-in self-checking circuit to insure .1 degree accuracy. Errors may be read directly on a 3-inch meter, calibrated to read ± 4 degrees.

Write for detailed specifications

Dependable Airborne Electronic Equipment Since 1928

Aircraft Radio Corporation
BOONTON NEW JERSEY

Precision Crystal Oven



Maintains Crystal Temperature—

to within 0.025°C at normal room temperature
—to within .15°C over outside range
from −40°F. to 150°F.

SPECIFICATIONS:

Operating temperature 75°C or 85°C

Warm up time for stable operation at −25°C — 7 minutes

Operates on 110 V, AC or DC (also in 6, 12, or 24 V models)

Mounting: standard base octal socket

Dimensions: 4″ high—1⅞″ wide —1-7/16″ deep

Crystal holder type: HC-6

Meets applicable requirements of Mil—T—945A

Withstands 10 day humidity cycle at 95% relative humidity, in accordance with SC-D-15914

Vibration test method 10 to 33 CPS at 0.06 inch excursion

Operates in horizontal or vertical position

Standard finish as per U. S. A. specs 72-53 Type 1: or any finish to meet purchaser's requirements

For further information, call or write

The Caribe Aircraft Radio Corporation's new crystal oven was engineered to military specifications for use in secondary frequency standards. Its unusual ability to maintain crystal temperatures within such precise tolerances is due to its unique low mass thermostat, large expanding element and high lever multiplication, minimizing contact wear, giving long life and freedom from drift.

Caribe
AIRCRAFT RADIO CORP.
COAMO, PUERTO RICO

Caribe Aircraft Radio Corp., Coamo, P. R. or Philip H. Harrison & Co., Matawan, N. J.

the
AUTOGRAF
Automatically plots X=(f)Y for you!

The Moseley Autograf—a precision, portable graphic recording instrument—plots transistor, diode, vacuum tube, magnetic amplifier and similar characteristics quickly, accurately, easily. The Autograf pens records on standard 8½"x11" graph paper. Scales: from 0-5 millivolts up to 0-100 volts both axes. Sensitivity—200,000 ohms per volt. Self-contained, weighs but 35 pounds.

=MOSELEY=

WRITE: F. L. MOSELEY CO., 409½N. FAIR OAKS AVE., PASADENA 3, CALIF.

Watch
TENSOLITE
for progress in
ELECTRONIC
WIRING!

For High Dielectric
Strength, specify—

TENSOLON
TEFLON-INSULATED
WIRE & CABLE

- THIN WALL
- 14 COLORS
- FREE-STRIPPING
- EXTRA FLEXIBILITY
- TOUGH TEFLON INSULATION
- TEMPERATURE RATING: —90° to +250°C

For an extra margin of dependability at maximum operating temperatures, specify these rugged Teflon insulated hook-up wires. Available in stranded sizes from 20 to 30 AWG with shields and teflon jackets or lacquered braids. Constructed to meet highest government and commercial standards, Tensolon Wires feature the new Tensulated-Teflon covering that eliminates pin holes and other imperfections.

ASSORTED TENSOLON HIGH-TEMP WIRES IN LABORATORY AND TEST QUANTITIES

An economical sample kit for designers, engineers, testing departments and development laboratories. Prices on request.

WRITE FOR CATALOG TODAY

TENSOLITE INSULATED WIRE CO., INC., TARRYTOWN, NEW YORK

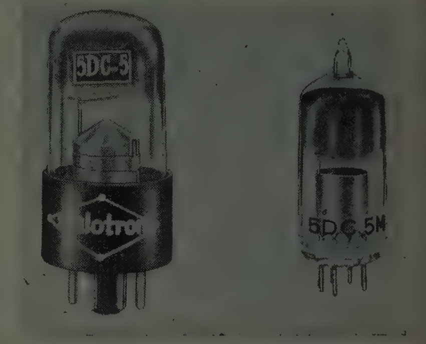
News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 174A)

Temperature Limited Diodes

Thermosen, Inc., 361 W. Main St., Stamford, Conn., manufacturers of "Kalotron" diodes, announce the addition of two new tubes to their line. Designated the 5DC-5 and the 5DC-5M, the tubes have similar electrical specifications, as follows: cathode voltage 5.6 ac/dc, cathode current 55–75 ma; plate voltage 500, plate current 0.450 to 0.575 ma. The 5DC-5 uses a T9F1 bulb and a #8537 8-pin intermediate octal base; the 5DC-5M uses a T5-1/2 bulb and a T5-1/2 7-pin miniature button base.

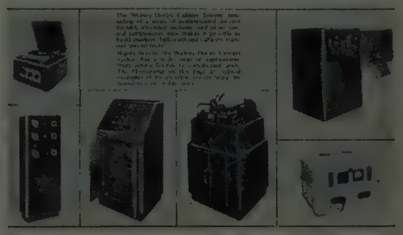


These diodes have temperature limited emission characteristics where the anode current is a direct function of filament voltage. Small changes in filament voltage result in relatively large changes in anode current. Due to the use of a pure tungsten filament, the specified ratings are maintained throughout the normal life of the tube.

Further information about these and other diodes may be obtained from the manufacturer.

Cabinet Components

British Industries Corp., 164 Duane St., New York 13, N. Y., has introduced into the United States a flexible new method of equipment cabinet construction by Widney-Dorlec. These components permit manufacturers and users of electronic equipment to build finished cabinets in their own shops without use of special tools.



Where quality and time are important, but the quantity is too small to justify the expense of full production tools, Widney-Dorlec cabinet components provide an ideal answer for manufacturers, laboratories, radio and television stations and many other users of electronic equipment.

(Continued on page 178A)

Potter & Brumfield STANDARD RELAYS

offer you **4** *important advantages*

PROVEN DESIGN
P & B's 20 years' experience in relay design is your assurance of long, trouble-free performance.

LOWER COST
These relays are already tooled. Mass production economies are passed on to you.

FAST DELIVERY
Orders for standard relays can be filled from stock or with a minimum of delay.

DISTRIBUTOR SALES
Popular types available through P & B Distributors located in all principal cities.

MORE THAN 110 P & B STANDARD RELAY STRUCTURES FOR EVERY ELECTRICAL AND ELECTRONIC APPLICATION

General Purpose	Telephone
Power	Motor Starting
Multiple Contact	Photo Flash
Multiple Leaf	Control
Latching	Sensitive
Plate Circuit	Miniature
Impulse	Shock Proof

Write for new master catalog describing our wide line of basic relay structures, housings and enclosures. Samples, quotations and recommendations promptly furnished on special problems.

POTTER & BRUMFIELD
PRINCETON, INDIANA
Export: 13 E. 40th Street, New York, New York
Sales Engineers in Principal U. S. and Canadian Cities

LFE SOLID DELAY LINES STORE INFORMATION

Offer important advantages in obtaining precise delay intervals for pulse or modulated signals:

Wide ranges of delay	Smooth pass band
Low attenuation	Wide temperature range
Low spurious response	Minimum size and weight
Wide bandwidth	Rugged construction

Available for video integration, computers, time markers, moving target indication, etc.

For complete information, write: Specialties Division

LABORATORY for ELECTRONICS, INC.
75-4 PITTS STREET • BOSTON 14, MASS.

PRECISION ELECTRONIC EQUIPMENT • OSCILLOSCOPES • MAGNETOMETERS • COMPUTERS • MICROWAVE OSCILLATORS • SOLID DELAY LINES

Specification Coils

—for every requirement—radio, FM, TV and Government Applications!

Including Universal, Bank Wound, Universal Progressive and Solenoid. All are precision-built to highest engineering standards and conform exactly to specifications. For uniform high quality, prompt delivery and economical unit costs, specify coils by Fugle-Miller. Radio, TV and JAN specifications are a specialty. Phone, wire or write for quotations.

ADDRESS INQUIRIES TO DEPT. P-10

FUGLE-MILLER LABORATORIES
MAIN STREET, METUCHEN, NEW JERSEY
Telephone Metuchen 6-2245

IT'S
HARVEY
FOR PROMPT
"OFF-THE-SHELF" DELIVERY

Whether it's equipment, components or other electronic requirements, you will always find them in Harvey's extensive stocks, ready for immediate delivery to you anywhere.

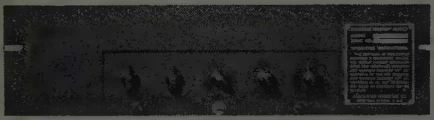
Harvey's twenty-five years of service to the industry are your assurance of understanding 'know-how' and complete dependability.

WRITE
PHONE
or WIRE

hrc

Telephone
JUdson 2-1500

HARVEY
RADIO COMPANY, INC.
103 West 43rd St., New York 36, N. Y.



RACK MOUNTING MODELS

THIS IS THE SUPPLY IN WHICH THE OUTPUT VOLTAGE VARIES TO HOLD THE LOAD CURRENT CONSTANT.

DESIGNED FOR PRODUCTION TESTING, RESEARCH, INSTRUMENTATION, AND CALIBRATING USE.

STANDARD MODELS ARE AVAILABLE TO COVER THE CURRENT RANGE OF 0.2 TO 100 M.A. IN ONE INSTRUMENT.

ELECTRONICALLY REGULATED
D.C. CONSTANT CURRENT
POWER SUPPLIES

OUTPUT CURRENT IS HELD
CONSTANT AS LOAD VARIES

OTHER MODELS AVAILABLE
WRITE DEPT. 10I FOR LITERATURE

ASSOCIATED SPECIALTIES CO.
1751 MAIN STREET
OREFIELD, PENNSYLVANIA

There is Always One Leader in Every Field
BODNAR INDUSTRIES, Inc.
leads in the field of
TRANSILLUMINATED PLASTIC LIGHTING PLATES
BECAUSE OF *Quality* • *Uniformity* • *Performance*
Design & Layout "Know-How Service"
Quantity Production Promptly
NEW YORK —19 Railroad Ave., New Rochelle (Home Office)
TEXAS —208 West Avery, P.O. Box 4116, Station A, Dallas
CALIFORNIA—4440 Lankershim Blvd., P.O. Box 264, North Hollywood
CANADA —313 Montreal Trust Bldg., 67 Yonge St., Toronto
SPECIMEN PANEL MIL-P-7788 (AN-P-89) SENT ON LETTERHEAD REQUEST

News—New Products

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 176A)

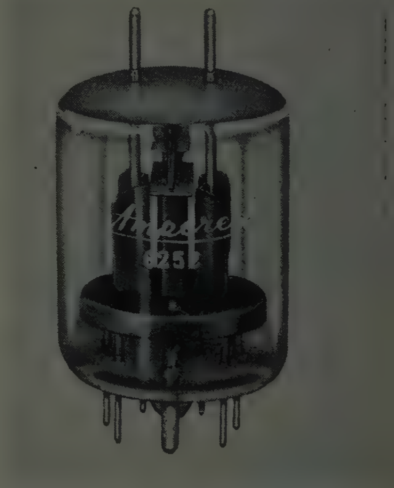
The Widney-Dorlec cabinet system consists of a series of prefabricated, die-cast corners, extruded sections, and other special parts, which fit together to form modern, full-radio used cabinets. Also available, and integrated into the system, are an extensive group of telescopic mountings and hardware.

Cabinets of any size, are easily made from the main frame sections and die-cast corners bolted together to form a substantial framework to work in which metal or plastic panels can be inserted. For large cabinets, intermediate crossbars give added strength and enable multiple units to be neatly housed. Where a square base is required, a special base section is available. Adding to the flexibility of the system are corners which allow sloping fronts of 45° to be erected.

For units that demand regular inspection or adjustment, provision is made for sliding drawer sections. Rail support brackets are made to fit internal slide rails to corner castings. When these slide rails are provided in the main cabinet, the chassis and the front panel easily slide in and out. Alternatively, the Widney-Dorlec telescopic mountings can be used.

Twin Tetrode

Amperex Electronic Corp., 230 Duffy Ave., Hicksville, L. I., N. Y., announces the addition of a new tube to their line of twin tetrode tubes, type 6252.



A lower power version of the Amperex type 5894/AX9903, the tube's maximum plate dissipation rating is 20 watts under ICAS conditions and works efficiently with a power output of 12 watts at 600 mc. It has been successfully operated as a frequency multiplier over the entire UHF television band.

Three inches in over-all height and slightly less than a 3/4 inch maximum diameter, the tube is suitable for low-drain mobile transmitters and multiplier chains.

(Continued on page 180A)

Let **WANG**

STATIC MAGNETIC DEVICES

serve you in your electronic system as:

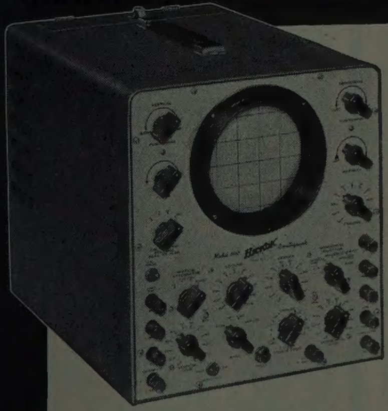
- Digital to analog converter
- Sequence pulse generator
- Pulse count converter
- Output display device
- Data manipulator
- Pulse generator
- Precision timer
- Number storage
- Shift register
- Pulse counter
- Synchronizer
- Rate meter

WANG LABORATORIES

296 Columbus Ave., Boston 16, Mass.
KEnmore 6-0624

HICKOK

Model 640



Laboratory Engineering

5″ OSCILLOSCOPE

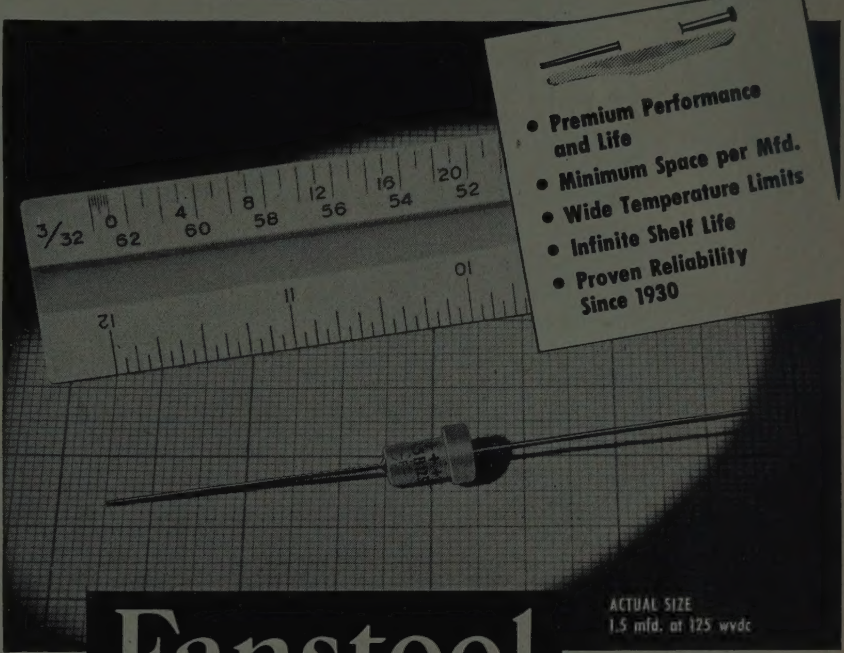
- DC amplifiers to 4.5 mc with 17 millivolt sensitivity.
- Calibrating voltages, triggered sweep, Z-axis modulation, light shield provided.
- Write for technical details . . .

THE HICKOK ELECTRICAL INSTRUMENT CO.

10551 DUPONT AVE., CLEVELAND 8, OHIO

TANTALUM CAPACITORS ARE BASIC

in current electronic trend......



- Premium Performance and Life
- Minimum Space per Mfd.
- Wide Temperature Limits
- Infinite Shelf Life
- Proven Reliability Since 1930

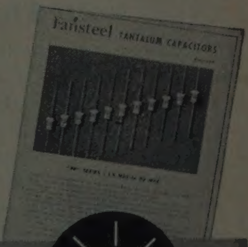
ACTUAL SIZE
1.5 mfd. at 125 wvdc

Fansteel

TANTALUM CAPACITORS

Now, through the use of tantalum, new high standards of electrolytic capacitor performance are available. The tantalum oxide film is the most stable dielectric, chemically and electrically, yet discovered. As a result, Tantalum Capacitors offer advantages not found in any other electrolytic type—long life, space saving, wide temperature range, excellent frequency characteristics, no shelf aging.

Tantalum Capacitors are made by Fansteel and other leading capacitor manufacturers. Ask for current information bulletins on Fansteel Tantalum Capacitors.



FANSTEEL METALLURGICAL CORPORATION

NORTH CHICAGO, ILLINOIS, U. S. A.

Tantalum Capacitors . . . Dependable Since 1930

32401C

Saratoga Industries

STAR PERFORMANCE AS MANUFACTURERS OF TRANSFORMERS, REACTORS, FILTERS, TOROIDAL COILS FOR THE ELECTRONICS INDUSTRY

Now in its ninth year of operation, Saratoga Industries, Inc. has built a solid reputation for the manufacture of precision windings. Approved for in-plant testing under MIL-T-27, Saratoga Industries, Inc. is also prepared to handle all types of commercial production. Saratoga engineers invite your inquiry to help solve your problems relating to reactors, transformers, filters and windings of all types.

SARATOGA INDUSTRIES, INC., SARATOGA SPRINGS, N. Y.

PPC

New and timely books—

Radio and Radar Technique
by A. T. Starr

This new book covers all the latest advances in radio and electronics with emphasis on methods and techniques. Especially stressed are: the role of noise in electronic systems; techniques in the super-high-frequency range (microwaves); the properties of systems as explicit functions of time, i.e., waveforms; and the fundamental behavior of electronic tubes.

812 pages *6¼" x 10"* *$15.00* *1953*

Television and Radar Encyclopaedia
Edited by W. MacLanachan

Comprehensive and authoritative, this new encyclopaedia provides a concise explanation of the fundamental principles of television and radar—for the layman as well as the qualified technician. Besides the 225 labeled illustrations, there are cross references following the more important topics. The inventor of television, Sir Robert Watson-Watt is among the contributors.

211 pages *5½" x 8½"* *$6.00* *1953*

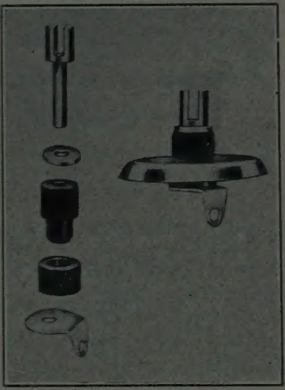
PITMAN Publishing Corporation 2 W. 45th St. New York 36

News—New Products

(Continued from page 178A)

Hermetic Seals

Stratoseal Mfg. Co., 3039 W. Fullerton Ave., Chicago 47, Ill., have a solid silicone hermetic seal which is claimed to leak less than 1 cc of air in 31 years at a pressure differential of 1 atmosphere.



The seals are available in a hollow tube type, turret stud type, or slotted stud as shown in the illustration. An 11/64 inch hole in the covers is all that is necessary prior to installation.

The slotted stud is at the top, compression member is second, top gland is third, bottom gland is fourth and the solder lug is fifth. Complete assembly is shown at right. The firm recommends that the top gland be inserted into the opening before the stud is inserted. Price $75 per M.

(Continued on page 183A)

ZOPHAR
---WAXES
---COMPOUNDS

Zophar Waxes, resins and compounds to impregnate, dip, seal, embed, or pot electronic and electrical equipment or components of all types; radio, television, etc. Cold flows from 100°F. to 285°F. Special waxes non-cracking at —76°F. Compounds meeting Government specifications plain or fungus resistant. Let us help you with your engineering problems.

107 YEARS
ZOPHAR MILLS, INC.
112-130 26th Street,
Brooklyn 32, N. Y.

These manufacturers have invited PROCEEDINGS readers to write for literature and further technical information. Please mention your I.R.E. affiliation.

(Continued from page 180A)

High Speed Alternators

High power outputs for their size and weight characterize a new line of miniaturized high-frequency alternators now being produced by **D & R, Ltd.,** 402 E. Gutierrez St., Santa Barbara, Calif.

d.r LTD.
SANTA BARBARA, CALIFORNIA
ALTERNATOR
5000~ 350 W
25,000RPM
MOD. No. A-17
SER. No. 329-1

Operating shaft speeds are from 10,000 to 50,000 rpm. The present line includes units with power output ratings from 125 to 4,000 watts at 5,000 cps.

As an example, the Model A-17 unit, illustrated herewith, $2\frac{1}{2}$ inches in diameter, weighing 22 ounces, delivers 350 watts output at 5,000 cps with a shaft speed of 25,000 rpm.

Over 85% of the torque wrenches used in industry are

STURTEVANT
TORQUE WRENCHES
Read by Sight, Sound or Feel.

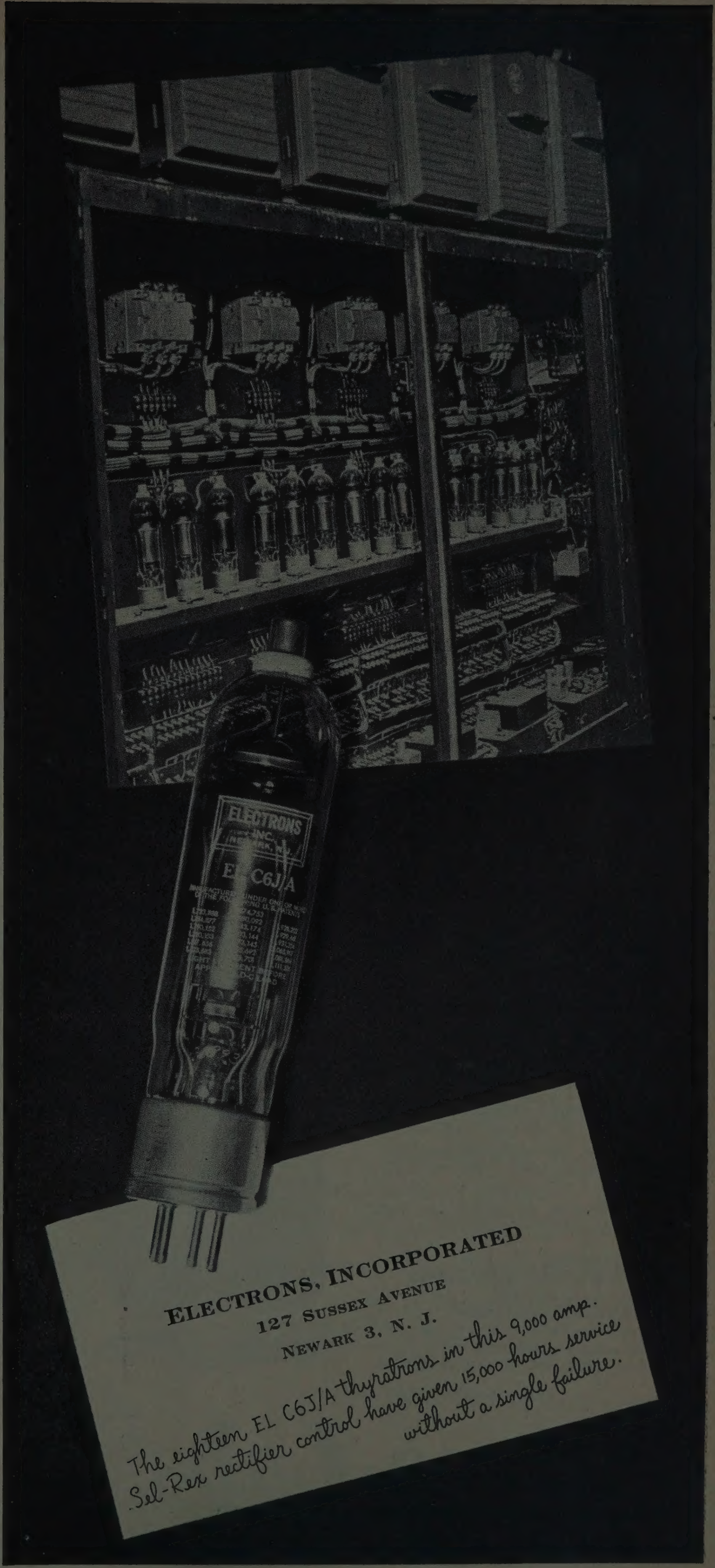
- Permanently Accurate
- Practically Indestructible
- Faster—Easier to use
- Automatic Release
- All Capacities

in inch ounces . . . inch pounds . . . foot pounds (All Sizes from 0-6000 ft. lbs.)

STURTEVANT TORQUE MANUAL

Every manufacturer, design and production man should have this valuable data. Sent upon request.

P.A. STURTEVANT CO.
ADDISON QUALITY ILLINOIS



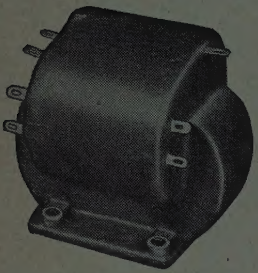
ELECTRONS, INCORPORATED
127 SUSSEX AVENUE
NEWARK 3, N. J.

The eighteen EL C6J/A thyratrons in this 9,000 amp. Sel-Rex rectifier control have given 15,000 hours service without a single failure.

FOR MILITARY

Acme ACME Electric

OR AVIATION APPLICATIONS



All the experience of 35 years of transformer building is now available to west coast buyers of electronic and MIL-T-27 transformers thru our west coast engineering laboratories. Adequate facilities for designing quality transformers are available on your requirements.

ACME ELECTRIC CORPORATION
MAIN PLANT: 4410 Water Street • Cuba, N. Y.
West Coast Engineering Laboratories: 1375 W. Jefferson Blvd. • Los Angeles, Calif.
In Canada: ACME ELECTRIC CORP. LTD. • 50 North Line Rd. • Toronto, Ont.

Acme ACME Electric
TRANSFORMERS

AN INSTRUMENT FOR ALL YOUR MAGNETIC MEASURING PROBLEMS

Dyna-Labs
D-79
GAUSSMETER

This precision built instrument measures flux density, determines direction of flow. It locates and measures stray fields and plots variations in strength and checks production lots against a standard. Simple to operate. No ballistic readings . . . no jerking or pulling. Supplied with protective carrying case.

- Other Features -
- Reads 10 to 30,000 Gauss Flux Fields
- Probe is only .025" thick
- Active area .01 square inches
- Overall size 13" x 6-3/4" x 10-1/2"
- Net weight only 10-1/2 lbs
- Power supply 105-125 volts, 50-60 cycles

Direct inquiries to Dept. IRE-10

KILOGAUSS
KILOGAUSS FULL SCALE
ON
OFF
GAUSSMETER
ZERO SET

Dyna-Labs INC.
1075 STEWART AVENUE, GARDEN CITY, L. I., N. Y. GARDEN CITY 3-2700

Professional Cards

ALFRED W. BARBER LABORATORIES
Specializing in the Communications Field and in Laboratory Equipment
Offices, Laboratory and Model Shop at:
32-44 Francis Lewis Blvd., Flushing, L.I., N.Y.
Telephone: Independence 3-3306

INTERNATIONAL RADIO CONSULTANTS
Pan American Radio Bldg., 16 Rue Delacroix
Tangier Int'l Zone Morocco
Specialized in the design, construction, installation and operation of foreign Radio, Electronic, Communications and Acoustical projects, and representing and advising governments and other agencies at meetings of the International Telecommunications Union in local, regional and world wide affairs.
Edward J. Content, P.E. and Staff

CROSBY LABORATORIES, INC.
MURRAY G. CROSBY & STAFF
RADIO-ELECTRONIC RESEARCH
DEVELOPMENT & MANUFACTURING
COMMUNICATIONS, FM & TV
ROBBINS LANE
HICKSVILLE, NEW YORK
HICKSVILLE 3-3191

INTERFERENCE MEASUREMENT SERVICES
OF
DYNAMIC ELECTRONICS—N.Y., INC.
Director—H. S. BENNETT, DR. ENG., P.E.
Specialists in determining equipment compliance with government radio interference specifications.
73-39 WOODHAVEN BLVD.
GLENDALE, L.I. IL-9-7000

ELDICO OF NEW YORK, INC.
Donald J. S. Merten and Engineering Staff
Consultants on Interference Elimination from Transmitters, Induction Heaters, Diathermy, etc.
44-31 Douglaston Parkway, Douglaston, L.I., N.Y.
Bayside 9-8686

ELECTRO-METRIC INSTRUMENT CO.
A. Newton, Director of Eng.
Circuit analysis, design and development in the fields of VHF, UHF tuners, TV receivers and accessories, laboratory and test instrumentation.
241 Centre Street, New York 13, N.Y.
Canal 6-1337

Richard B. Schulz
Electro-Search
Radio-Interference Reduction;
Development of Interference-Free Equipment,
Filters, Shielded Rooms
4337 N. 5th Street, Philadelphia 40, Pa.
GLadstone 5-5353

ELK ELECTRONIC LABORATORIES, INC.
Jack Rosenbaum
Specializing in design and development of Test Equipment for the communications, radar and allied fields
333 West 52nd St., New York 19, PL-7-0520

(Continued on page 186A)